SISPAD 2022

INTERNATIONAL CONFERENCE ON SIMULATION OF SEMICONDUCTOR PROCESSES AND DEVICES

Conference Program

International Conference on Simulation of Semiconductor Processes and Devices

September 6-8th, 2022 – Granada, Spain

The conference will be held in presence at the *Palacio de Congresos* located in *Paseo del Violón*, s/n, 18006 in Granada (https://goo.gl/maps/ptkwd6cJSXjGygfh8).

The *International Conference on Simulation of Semiconductor Processes and Devices* (SISPAD) provides an international forum for the presentation of leading-edge research and development results in the field of process and device simulation. SISPAD is one of the longest-running conferences devoted to technology computer-aided design (TCAD) and advanced modeling of novel semiconductor devices and nano-electronic structures.

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The local organizing committee also received financial support from the UGR Research and Knowledge Transfer Fund (PPIT).

Welcome to SISPAD 2022

Dear Colleague,

On behalf of the University of Granada and the Organizing Committee, I warmly welcome you to the 27th International Conference on Simulations of Semiconductor Processes and Devices.

It has been a difficult period with the worldwide pandemic. The last two editions were very complicated, and I would like to publicly recognize the efforts and generosity of the Organizing Committees of SISPAD-2020 (Osaka, Japan) and SISPAD-2021 (Dallas, TX, USA) for keeping the conference even in so difficult circumstances. We're all in debt to them. Thank you!!

We would also like to make a special mention to the Steering Committee of SISPAD and its President Prof. Juergen Lorentz, for their support, professionality, and their valuable advice during the organization of the conference.

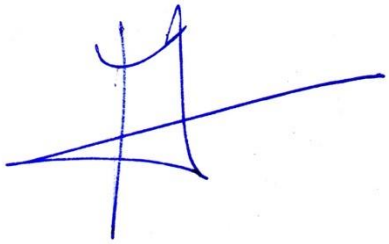
I am very grateful that so many of you have been able to overcome the difficulties and make it to Granada. This run of SISPAD 2022 has once again attracted an extremely high standard of participants and I am sure that this will be an extraordinary meeting. Our delegate list includes contributions from twenty-two countries, from many leading companies, Universities and Research Labs. So I anticipate plenty of stimulating discussions. I also hope that SISPAD 2022 will promote new collaborations between industry and academia which will further advance the science of Semiconductor simulations.

The success of a meeting like SISPAD depends, of course, on the quality of the presentations but even more important is the active participation of the other assembled experts. So, I encourage everyone to take part in the discussions and debates that go on both during the scientific sessions and during the breaks. We have tried to put all the ingredients so the conference becomes a familiar and comfortable event, and you feel at home.

We have not spared any efforts to allow the SISPAD conference to recover the excellence that it used to have in the events previous to the pandemic, not only in the scientific sphere but also in the social one. And, here we have counted with the inestimable help of the city of Granada. Granada has an incomparable historical, cultural and social heritage. For thousands of years, Granada has served as a place of convivence for millenary civilizations, Jews, Christians and Muslims. Granada and its Alhambra represent an incomparable frame of mixing of cultures, and peaceful coexistence. And all these have deeply marked the actual life and spirit of an old but at the same time modern city and its open-mind population.

Granada is also the seat of one of the older Universities in Spain and Europe. Founded by Emperor Charles V in 1531, the University of Granada with almost 500 years of history, is today one of the more active Universities in Spain (in the top 3) and it is ranked in the top 200 of all Universities Worldwide.

I would like to thank you all – presenters, audience, exhibitors, organizers and the SISPAD committees (Steering Committee and Technical Program Committee) - for your participation in this conference. I hope you have an interesting, informative, enjoyable, and overall, unforgettable stay at Granada.



F. Gamiz
SISPAD 2022 Conference Chair

Invited Speakers

Prof. Siegfried Selberherr

About Electron Transport and Spin Control in Semiconductor Devices

As the scaling of CMOS-based technology displays signs of an imminent saturation, an introduction of novel non-conventional computational degrees of freedom to sustain the path of energy efficient computing at reduced costs becomes paramount. Employing the second intrinsic electron characteristics – the electron spin – offers additional functionality to electron devices. Apart from forming a qubit, the electron spin is promising for digital applications. We discuss recent advances in spin-based switches: SpinFETs and SpinMOSFETs, as well as nonvolatile CMOS-compatible spin-transfer torque and the spin-orbit torque magnetoresistive random access memories. A modeling approach based on an appropriate extension of the spin and charge transport equations to complex layered structures including tunnel barriers is introduced. As an example, the magnetization dynamics in ultra-scaled MRAM cells is evaluated.

Professor Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of Diplomingenieur in electrical engineering and the doctoral degree in technical sciences from the Technische Universität Wien in 1978 and 1981, respectively. Dr. Selberherr has been holding the venia docendi on computer-aided design since 1984. Since 1988, he has been the Chair Professor of the Institut für Mikroelektronik. From 1998 to 2005, he served as Dean of the Fakultät für Elektrotechnik und Informationstechnik. Prof. Selberherr published more than 400 papers in journals and books. He and his research teams achieved more than 1200 articles in conference proceedings of which more than 200 have been with an invited talk. Prof. Selberherr authored three books and co-edited more than 45 volumes, and he supervised, so far, more than 100 dissertations. His current research interests are modeling and simulation of problems for microelectronics engineering. Prof. Selberherr is a Fellow of the IEEE (1993), a Fellow of the European Academy of Sciences and Arts (2004), a Fellow of the Academia Europaea (2013), and a Fellow of the Asia-Pacific Artificial Intelligence Association (2021).

Dr. Farzan Gity

Mono-material TMD-based heterostructures for nanoelectronics applications

Transition metal dichalcogenide (TMD) based heterostructures can be formed by interfacing two different TMDs through vertical stacking in which these TMDs are interacting through weak van der Waals (vdW) forces, to circumvent the conventional lattice-mismatch problem. Heterostructures of two dissimilar TMDs can be used in device structures with atomically sharp and clean interfaces. TMD-based heterostructures allow for exploring new physics and device architectures by utilising different strategies, such as combining different TMDs, various crystallographic alignment and stacking sequence. Combining monolayers of different TMDs in vertical and lateral geometry allows for manipulating the electrical and optical properties of the heterostructure-based devices.

Molybdenum disulfide (MoS2) is the most studied TMD with a wide variety of applications such as field-effect transistors (FETs), light harvesting devices, chemical sensors, photocatalysts, and flexible electronics. Bulk MoS2 is semiconducting with an indirect bandgap of 1.2 eV, whereas monolayer MoS2 is a direct gap material with a bandgap of 1.8 eV, where the conduction band minimum and the valence band maximum are located at the K-point. Tungsten disulfide (WS2) possesses similar crystal structure as of MoS2 where monolayer WS2 is also direct semiconductor with bandgap of 1.97 eV. Both electron and hole effective masses of WS2 are smaller than that of MoS2. AA' stacking of monolayer MoS2 and WS2 creates an indirect bandgap material with larger contribution of WS2 valance and MoS2 conduction states (Fig. 1). This is consistent with the scanning tunnelling spectroscopy (STS) measurements of MoS2/WS2 heterostructures.

Dr Farzan Gity is a Principal Investigator (PI) and a senior staff researcher at Tyndall National Institute, University College Cork (UCC). In addition to Irish Research Council fellowship, he was the PI of the EU-H2020 SaSHa project at Tyndall. Dr Gity has also received the Science Foundation Ireland Technology Innovation and Development Award for integrating dissimilar materials for advanced nanoelectronic applications. He is the PI of the EU FET-OPEN INTERFAST project at Tyndall on developing novel spin-based devices. In 2019, Dr Gity has been awarded UCC's Early Stage Researcher of the Year Award.

Dr Gity's activities involve Emerging Materials and Devices for future nanoelectronics and spintronics applications, including nanofabrication, characterisation and simulations of materials and devices based on two-dimensional materials. He has more than 6 years of collaborative research projects with major semiconductor industries such as Intel.

Dr. Gerhard Klimeck

Semiconductor workforce development through immersive simulations on nanoHUB.org

Over 160,000 nanoHUB users have run over 7 million simulations in Apps mostly focused on semiconductor devices and materials modeling. nanoHUB created nano-Apps before Apple created Apps for the iPhone and made scientific codes usable for a much larger user group. Most scientific tools strive to be comprehensive in solving "any" simulation problem in a specific problem range. That comprehensiveness limits the use to experts, who require extensive training. nanoHUB has instead focused on delivering a spectrum of Apps (over 700 now) that individually have a limited capability focused on a PN-junction, MOSFET, or nanowire while the underlying tool could of course solve a much wider set of problems. We assembled some of these Apps that are essential for specific courses into small sets such as ABACUS (crystals, bandstructure, drift-diffusion, pn-junctions, BJTs, MOScaps, MOSFETs). The usability results are stunning. Our user analytics prove that over half of the simulation users participate in structured education through homework/project assignments. We can identify classroom sizes and detailed tool usage. We can begin to build mind-maps of design explorations and assess depth of explorations for individuals and classes. While parts of academia struggled to innovate curricula, we have measured the median first-time App insertion into a class to be less than six months. Over 180 institutions have utilized nanoHUB in their curriculum innovation in over 3,600 classes. 2 million nanoHUB visitors explore lectures and tutorials annually. With such a community presence we believe nanoHUB is the platform of choice to deliver online modeling, simulation, virtual environments, and lectures for the US initiative on workforce development. This presentation will overview some of the nanoHUB impact metrics and turn towards a tool recitation session. In the recitation a brief overview of ABACUS will be given and the audience may request other tool demonstrations or exploration.

Dr. Gerhard Klimeck is a Professor of Electrical and Computer Engineering at Purdue University; Director of the Network for Computational Nanotechnology; Reilly Director of the Center for Predictive Materials and Devices. He helped to create nanoHUB.org, the largest virtual nanotechnology user facility serving over 2.0 million global users, annually. Dr. Klimeck is a fellow of the Institute of Physics (IOP), the American Physical Society (APS), the Institute of Electrical and Electronics Engineers (IEEE), the American Association for the Advancement of Science (AAAS), and the German Humboldt Foundation. He has published over 525 printed scientific articles; he has been recognized for his co-invention of a single-atom transistor, quantum mechanical modeling theory, and simulation tools. His NEMO5 software has been used since 2015 at Intel to design nano-scaled design transistors. The nanoHUB team was recently recognized by a top 100 by R&D award - Making simulation and data pervasive.

Dr. Raphaël J. Prentki

Tunneling leakage in ultrashort-channel MOSFETs—From atomistics to continuum modeling

The channel lengths of some transistors are now nearing the nanometer, making these devices prone to direct source-to-drain tunneling (DSDT), a leakage mechanism commonly considered to set the end of Moore's law. In a MOSFET, the probability for a charge carrier to undergo DSDT decays exponentially with channel length, source depletion length, and drain depletion length. Bound-charge engineering (BCE) is a recently introduced scheme where the depletion lengths of transistors can be controlled through effective doping by surface bound charges residing on the interface between a semiconductor and an adjacent oxide. In this work, BCE is applied to reduce DSDT leakage current down to acceptable levels in MOSFETs with channels as short as 1.5 nm; the higher the oxide permittivity, the lower the DSDT leakage. As vehicles for this study, we consider n-type gate-all-around MOSFETs with (A) a 2-nm-wide silicon nanowire (NW) channel and (B) a silicon nanosheet (NS) channel. The silicon NW devices are modeled via state-of-the-art atomistic quantum transport simulations based on the nonequilibrium Green's function (NEGF) formalism and the tight-binding (TB) model, a simulation paradigm currently under development within our first-principles quantum transport software NanoDCAL+ which properly accounts for the atomistic effects, quantum confinement, and nonequilibrium quantum transport phenomena relevant in ultrascaled devices. On the other hand, the silicon NS devices, which are physically larger, are simulated within continuum models after calibration against NEGF–TB data. Specifically, we use the new NEGF–k·p feature under development within the QTCAD software suite (Quantum-Technology Computer-Aided Design), our finite-element-based quantum hardware modelling tool. It is found that short-channel device with high-permittivity oxides exhibit temperature-dependent DSDT, thereby maintaining their subthreshold swing at a value close to the thermal limit of 60 mV/dec at room temperature. BCE may thus pave a way toward ultrascaled MOSFETs. This work highlights the need for simulation platforms combining ab initio simulation tools, which can account for atomistic and quantum effects, with continuum models describing quantum transport at a mesoscopic scale, at which devices are too large to be described purely from first principles but small enough for tunneling to be significant.

Raphaël J. Prentki obtained his Ph.D. in Physics from McGill University in 2021. His doctoral research focused on charge transport in low-power nanoelectronic devices, notably tunnel field-effect transistors (FETs), negative-capacitance FETs, and cold-source FETs. He studied these emerging systems using both analytical and computational methods of condensed matter and statistical physics, such as the effective mass approximation, the Landauer–Büttiker formalism, the tight-binding model, density functional theory, and the nonequilibrium Green's function formalism. He joined Nanoacademic Technologies in 2022; he is currently a research scientist and software developer for QTCAD, Nanoacademic Technologies' newest modeling tool for quantum technologies.

Program at a Glance

Monday, September 5th – Workshop day – Room: Andalucia 2

Morning workshop: MONTE CARLO SIMULATION: BEYOND MOORE'S LAW

Time	Title
9:00 – 11:10	First session (4 talks)
11:10 – 11:40	Coffee break
11:40 – 13:40	Second session (4 talks)
13:40 – 15:00	Lunch

Afternoon workshop: MODELING AND CHARACTERIZATION OF 2D MATERIALS FOR MORE THAN MOORE APPLICATIONS

Time	Title
13:40 – 15:00	Lunch
15:00 – 16:30	First session (3 talks)
16:30 – 17:00	Coffee break
17:00 – 18:30	Second session (3 talks)

Monday, September 5th – Conference program

08:15 – 19:00	Registration
19:00 - 20:00	Bus departure and transfer to welcome cocktail
20:00 – 22:00	Welcome cocktail at *Carmen de los Mártires*
22:00 – 22:30	End of the soirée and bus transfer

Tuesday, September 6th

08:15	Registration Opening	
08:50 - 09:15	Conference Opening: Prof. Pilar Aranda Ramírez Rector of the University of Granada	
09:15 – 10:00	Invited talk: Siegfried Selberherr, TU Wien	
10:00 – 10:20	Coffee Break	
10:20 – 11:40	S1A - Magnetism	S1B – Power Electronics
11:50 – 13:10	S2A – Tunneling and Steep Slope Devices	
13:10 – 14:30	Lunch	
14:30 – 16:10	S3A – Process Simulation	S3B – Machine Learning I
16:10 – 16:30	Coffee Break	
16:30 – 17:50	S4A – TCAD Models	S4B – Machine Learning II
18:00 – 19:00	Get-together cocktail	
19:00 – 19:20	Bus departure for private Alhambra guided tour	
19:30 – 22:00	Exclusive visit to Alhambra and Palace of the Emperor Charles V	

Wednesday, September 7th

08:15	Registration Opening	
09:00 - 09:15	SISPAD 2023 Presentation – Satofumi Souma, Kobe University	
09:15 – 10:00	Invited talk: Farzan Gity, Tyndall National Institute	
10:00 – 10:20	Coffee Break	
10:20 – 11:40	S5A – Two-Dimensional Materials	S5B – High-Frequency Devices
11:50 – 13:10	S6A – Atomistic and Ab-initio Modeling	S6B – Circuit Simulation and Compact Modeling
13:10 – 14:30	Lunch	
14:30 – 15:15	Invited talk: Gerhard Klimeck, Purdue University	
15:15 – 17:15	Coffee Break + Poster Session	
18:30 – 19:00	Bus departure and transfer to Albaycín	
19:00 – 20:30	Guided visit across the Albaycín	
20:30 – 22:30	Gala dinner at *Palacio de los Córdova*	

Thursday, September 8th

08:15	Registration Opening	
09:15 – 10:00	Invited talk: Raphaël J. Prentki, Nanoacademic Technologies Inc.	
10:00 – 10:20	Coffee Break	
10:20 – 11:40	S7A - Qubits	S7B – Reliability I
11:50 – 13:10	S8A – Memories	S8B - Reliability II
13:10 – 14:30	Lunch	
14:30 – 16:10	S9A – Advanced Methods for Numerical Calculations	S9B – Nanodevices and Interconnects
16:10 – 16:30	Coffee Break	
16:30 – 17:50	S10A – Sensors and Optoelectronics	S10B – Interfaces, Traps and Defects
17:50 – 18:00	Conference Closing	

Sessions A will take place in **Rooms Andalucía 1+2**
Sessions B will take place in **Room Andalucía 3**

https://congresos.ugr.es/sispad2022/program/

General Information

TRAVEL INFORMATION AS FOR JULY 12TH (Periodically Check this website)

PASSENGERS FROM COUNTRIES THAT BELONG TO THE EUROPEAN UNION OR SCHENGEN ASSOCIATED COUNTRIES

Passengers arriving in Spain by AIR OR SEA from these countries will NOT be required to present the SpTH health control form or a COVID-19 certificate.

PASSENGERS FROM COUNTRIES THAT DO NOT BELONG TO THE EUROPEAN UNION OR ARE NOT CONSIDERED AS ASSOCIATED COUNTRIES SCHENGEN

Passengers arriving in Spain by AIR (except children under the age of 12 and passengers in international transit) from countries that DO NOT belong to the European Union or are NOT considered Schengen associated countries, must have one of these documents:

DIGITAL COVID CERTIFICATE OR EU EQUIVALENT vaccination against COVID-19 or a negative certificate of an active infection diagnostic test or a certificate of recovery after passing the disease. You can check if your certificate is valid on the website https://www.spth.gob.es/ or in the Spain Travel Health app -SpTH- (Android, iOS, Huawei).

Upon arrival at the airport follow the signals indicating the **ORANGE WAY**.

QR SPTH. If you do not have the EU Digital COVID Certificate or EU equivalent, you must fill in the SPTH Health Control Form manually entering the details of your vaccination, recovery or diagnostic test certificate through the website https://www.spth.gob.es/ Will open in a new window or the Spain Travel Health application -SpTH- (Android, iOS, Huawei). The system will send you a QR code that you will have to present both prior boarding, and upon your arrival in Spain. In the health control, you may be required to present this document certifying vaccination, diagnostic test or recovery.

Upon arrival at the airport follow the signals indicating the **BLUE WAY**.

Please consider checking periodically the ongoing travel limitations as restrictions might change at any time.

SAFE EVENT

All organized events must comply with the ongoing anti-contagion safety protocol imposed by the Spanish government. SISPAD 2022 is no exception and, although the restrictions are currently soft, be aware that heavier limitations might be imposed such as mandatory face mask to access the conference.

GRANADA

Granada has been the crucible of cultures and civilizations where, during the centuries, Christians, Muslims, and Jews lived all together. Nowadays, Granada is a modern city that has an uncommon scientific and cultural background, along with the University and the institutes of the Spanish National Research Council (CSIC), and an architectural, natural, and historic

patrimony like no other. Likewise, it owns a grown and active corporate environment made up of companies based on knowledge, standing out those related to the health campus and new technologies. To all these values, we should add an extensive cultural activity and the well-known hospitality of the people from Andalucía which brings a warm welcome to their guests.

Granada welcomes every year more than 2,5 million tourists both nationally and internationally driven here for the excellent touristic offers, the location, and the weather, with the Alhambra as the most emblematic monument, being the most visited monument in all of Spain.

CONFERENCE VENUE

The congress venue will be the Granada Conference Center (*"Palacio de congresos"*): for its design, size, and features, it is considered one of the main Conference Centers in Spain. It can be found at *Paseo del Violón S/N*, 18006 Granada.

LODGING INFORMATION

Close to the Conference Venue, the SISPAD attendees can find a varied offer of hotels. Some of them have been selected according to their proximity:

- Hotel Saray. (* * * * 0.2 km)
- Senator Granada Spa. (* * * * 0.3 km)
- Macià Monasterio de los Basilios. (* * * 0.4 km)
- Andalucía Center Granada. (* * * * 0.7km)
- Occidental Granada. (* * * * 0.8 km)
- Abades Recogidas. (* * * * 1.1 km)
- Barceló Granada Congress. (* * * * * 1.2 km)

HOW TO REACH GRANADA

Direct flights to Granada

International connections exist to Granada (airport code GRX) from London Gatwick and Paris Orly operated by Vueling Airlines. However, given that the number of flights from these cities is quite limited, the best option for reaching Granada by plane is to take an international flight to Madrid or Barcelona and then a domestic flight to Granada.

The airport is located 17 km from the city center. Upon arrival, the connection to the city can be done by taxi (around 30 Eur) or by bus. The bus transfer is cheaper (3 Eur) and has one of the stops at the Conference Venue (7 stops from the airport). The bus departure schedule is synchronized with the flight's arrival and typically takes place around 30 minutes after landing. The bus stop is to the right of the building as you leave the airport.

Direct flights to Málaga

Málaga is the closest international airport to Granada (125 km). International direct flights land at the Málaga airport coming from the main cities of Europe.

Once arrived at Málaga Airport, the possibilities of reaching Granada by public transport are the following:

- Direct bus from the airport to the Granada bus station (12.21 Eur and around 2 h). This is the easiest transfer possibility. There are around 10 departs per day. To check if the timetables fit your flight schedule you can take a look here.
- If the direct bus connection is not an option for you, then the most convenient solution is to take a train to Málaga Central Station (María Zambrano Station). From there, you can take a direct bus to Granada (the Central Train Station is in front of the Málaga Bus Station) almost every hour.

TOURIST INFO

Granada is famous because of its large amount of tourist possibilities, amongst you can find such magical places such as la Alhambra (an ancient Andalusian city-castle, which was built in the XI century), the main cathedral (catholic temple, great work of the Spanish Renaissance), the city's old historic center and the wonderful borough of Albayzin.

CONFERENCE WIFI CONNECTION

The conference room is equipped with a WiFi connection with the following parameters:

SSID: SISPAD
Password: SISPAD22

Social Events

Since this year's edition of SISPAD represents the recovery of the greatly missed on-site conference format, it has been the will of the Local Organization Committee to regale the attendees of SISPAD 2022 and their registered companions with a varied, enriching, and intense social program.

The city of Granada, custodian, and inheritor of the mixture of cultures that left their indelible legacy across the centuries offers an incomparable landscape for brightening up the SISPAD Conference again.

SEPTEMBER 5TH (MONDAY)

The social activities will start the day before with a warm welcome soirée. Attendees and registered companions are expected to arrive at the Conference Venue according to the following schedule:

- 19.00 – 19.30 Reception at the Conference Palace of Granada (Venue of SISPAD 2022).

The Conference Palace of Granada will be the meeting point for SISPAD 2022 participants and companions to organize the bus transfer to the premises where the welcome cocktail will take place.

- 19.30 – 20.00 Bus transfer.
- 20.00 – 22.00 Welcome cocktail.

The welcome cocktail will take place at the *Carmen de los Mártires*, a small palace surrounded by beautiful gardens next to the forest of the Alhambra.

- 22.00 – 22.30 End of the soirée and bus transfer to city center.

SEPTEMBER 6TH (TUESDAY)

Once the afternoon session of the Conference is over, the social activities of the evening will be the following:

- 18.00 – 19.00 Get-together cocktail.

It will consist of an informal cocktail served at the Conference Venue as an opener for the cultural soirée of the day.

- 19.00 – 19.20 Departure of buses from the Conference Venue and transfer to the Alhambra.

Guides will welcome the SISPAD participants and their companions at the Conference Venue and accompany them in the buses to the Alhambra.

- 19.20 – 19.40 Organization and distribution of the groups for the visit.

Several groups, headed each one by a guide, will be formed to respect the strict limitation of 30 persons/group imposed by the Alhambra.

- 19.30 – 22.00 Exclusive visit to the Alhambra and Palace of Emperor Charles V.

The *Palace of the Alhambra* and the *Palace of Emperor Charles V* will be closed to the general public and tourists so that they will be exclusively open for the SISPAD participants offering them the possibility of quiet and private enjoyment of these monuments.

- 22.00 End of the guided visit and soirée.

The guides will conduct the participants through the forest of the Alhambra accompanying them to Plaza Nueva where the visit and the social program of the day will conclude. The place is surrounded by a vast number of bars where the participants will have the opportunity, if they wish, of continuing their soirée by enjoying some drinks before coming back to their hotels.

SEPTEMBER 7TH (WEDNESDAY)

The last evening with programmed social events will be structured as follows:

- 18.30 – 19.00 Departure of buses from the Conference Venue and transfer to the Albaycin.

Buses will head to the Mirador (viewpoint) de San Cristóbal, located on the upper side of the Albaycín, the ancient Arab neighborhood located on the hill in front of the Alhambra.

- 19.00 – 20.30 Guided visit across the Albaycín.

From the Mirador de San Cristóbal, the guides will accompany the SISPAD participants in their immersive journey across the labyrinthine Arabic streets and alleys of the Albaycín (estimated length of 3-4 km). The route will end in the magnificent *Palacio de los Córdova*, built in the XVI century where the Gala Dinner will take place.

- 20.30 – 22.30 Gala Dinner.

SISPAD participants will enjoy the Gala Dinner in the gardens of the Palace with unique views of the Alhambra during the twilight and the beginning of the night.

- 22.30 End of the soirée and return to hotels.

Due to the location of the Palace and the traffic restrictions of the environment, the return to the hotels cannot be done by bus. Participants are invited to enjoy the walk through the incomparable Paseo de los Tristes and Carrera del Darro one of the most beautiful streets in the world that connects the Arabic world of the Alhambra and Albaycin to the Baroque and Renaissance parts of the city, leading them to Plaza Nueva (where the visit of the previous day ended). Once there, those who wish it will be able to decide whether they want to take a taxi for reaching their hotels or continue on foot.

Satellite Conference Workshops (Monday, September 5th)

WORKSHOP WS1 – MONTE CARLO SIMULATION: BEYOND MOORE'S LAW

The Monte Carlo simulation approach is widely conceived as a powerful solution in comparison to other semiconductor simulation tools. Some distinctive characteristics are:

- It provides manageable simulation times compared to entirely quantum solvers.
- It allows a more accurate description of physical processes compared to classical simulators.
- Contrary to TCAD tools, it offers the possibility of including appropriate corrections for the study of quantum effects of nanoscale transistors.
- It helps unveil physical insight into what is happening inside the device, providing valuable information for defining optimization strategies.

The presentations included in the workshop will provide an overview of the Monte Carlo technique for the simulation of nanodevices going from general strategies, through the description of specific processes (like scattering mechanisms or tunneling phenomena), and reaching more complex approaches (such as Kinetic Monte Carlo or Wigner Monte Carlo).

The workshop is organized by C. Medina-Bailon and C. Sampedro (University of Granada). Financial support for the workshop organization has been obtained by C. Medina-Bailon (Univ. of Granada) from the Juan de la Cierva Incorporación Fellowship Program under grant agreement No. IJC2019-040003-I (MICINN/AEI).

Invited speakers cover the industrial and academic domain of research according to the following program:

Time	Speaker	Title
9:00	**C. Medina-Bailón** (Univ. of Granada, Spain)	General Welcome
9:10	**A. Asenov** (Univ. of Glasgow, Scotland)	The role of transport Monte Carlo simulations in Advanced CMOS TCAD
9:40	**H. Kosina** (TU Wien, Austria)	Recent Developments in Semiclassical Transport: Backward Monte Carlo and Electron-Electron Scattering
10:10	**C. Sampedro** (Univ. of Granada, Spain)	Quantum corrections in EMC: From Multisubband to quantum transport
10:40	**Craig Alexander** (Synopsys, UK)	Monte Carlo Transport Simulation – High Performance Logic and Beyond
11:10	**Coffee break**	
11:40	**V. Georgiev** (Univ. of Glasgow, Scotland)	Multi-scale simulations of novels electronic devices with KMC methods
12:10	**M. Ballicchia** (TU Wien, Austria)	Monte Carlo approach for solving integral equations: From classical-Boltzmann to quantum-Wigner particles
12:40	**L. Filipovic** (TU Wien, Austria)	ViennaEMC: A Broadly-Applicable Ensemble Monte Carlo Framework
13:10	**M. V. Fischetti** (Univ. of Texas at Dallas, USA)	Electronic transport in supported and gated two-dimensional materials: An ab initio Monte Carlo study
13:40	**Lunch**	

WORKSHOP WS2 – MODELING AND CHARACTERIZATION OF 2D MATERIALS FOR MORE THAN MOORE APPLICATIONS

Since the discovery and isolation of graphene were awarded The Nobel Prize in Physics, Two-dimensional (2D) materials have received outstanding attention for electronic, optics, and photonic applications. Incorporating 2D materials has demonstrated an optimal electrostatic control of the channel thanks to their reduced thickness. Moreover, promising levels of immunity to short channel effects, high ON/OFF ratios, reduced power consumption, low current leakage, and short switching delay are expected according to the International Roadmap for Devices and Systems (IRDS) guideline. However, to explore metal chalcogenide mixes and evaluate the potential properties and applications, solid and reliable models are required. "Modeling and characterization of 2D materials for More than Moore applications" presentations from industry and research centers will highlight the most important challenges and will provide insight into the capabilities of existing simulation modules for modeling novel 2D materials and devices.

The workshop is organized by C. Marquez and C. Navarro (University of Granada) in cooperation with the H2020 project TRAPS-2D No 895322 and Spanish Program PID2022-119668GB-I00.

The workshop will comprise presentations from industry and research:

Time	Speaker	Title
13:40	Lunch	
15:00	**Carlos Marquez** (Univ. of Granada, Spain)	Opening talk- 2D materials Roadmap
15:30	**Tue Gunst** (Synopsys Denmark)	Multiscale Atomistic to TCAD Workflow for 2D-FET Engineering
16:00	**Theresia Knobloch** (IuE, TU Wien, Austria)	Enhancing the Reliability of 2D Nanoelectronics Guided by Physical Modeling
16:30	Coffee break	
17:00	**Lida Ansari** (Tyndall National Institute, Ireland)	Semimetal-based TMDs for beyond CMOS
17:30	**François Triozon** (LETI, France)	Simulation of electron transport in 2D layers and through metal/2D/metal stacks
18:00	**Francisco Gámiz** (Univ. of Granada, Spain)	More-than-Moore applications of 2D materials

Detailed Conference Program

Monday, September 5th

19:00 - 19:30	**Reception at the Conference Palace of Granada**
19:30 - 19:30	**Bus transfer**
20:00 – 22:00	**Welcome cocktail**
22:00 – 22:30	**End of the soirée and bus transfer**

Tuesday, September 6th

08:50 - 09:15	**Conference Opening:** **Prof. Pilar Aranda Ramírez, Rector of the University of Granada**
09:15 – 10:00	**About Electron Transport and Spin Control in Semiconductor Devices** S. Selberherr, TU Wien (Austria)
10:00 – 10:20	**Coffee break**
	Session 1A: Magnetism (Rooms Andalucía 1+2) Chairperson: S. Selberherr (TU Wien, Austria) and F. Gámiz (Univ. of Granada, Spain)
10:20 - 10:40	**A novel ferroelectric nanopillar multi-level cell memory** Hyeongu Lee and Mincheol Shin School of Electrical Engineering, Korea Advanced Institute of Science and Technology (Republic of Korea)
10:40 - 11:00	**Semi-empirical and VerilogA compatible compact model for ferroelectric hysteresis behavior** M. Lederer[1], R. Olivo[1], N. Yadav[1], S. De[1], K. Seidel[1], L. M. Eng[2] and T. Kämpfe[1] [1]Fraunhofer IPMS, CNT (Germany) [2]TU Dresden (Germany)
11:00 - 11:20	**New Insights into the Effect of Spatially Distributed Polarization in Ferroelectric FET on Content Addressable Memory Operation for Machine Learning Applications** Chang Su[1], Weikai Xu[1], Qianqian Huang[1,2], Lining Zhang[3] and Ru Huang[1,2] [1]School of Integrated Circuits, Peking University (China) [2]National Key Laboratory of Science and Technology on Micro/Nano Fabrication (China) [3]School of Electronic and Computer Engineering, Peking University (China)
11:20 – 11:40	**Comprehensive Evaluation of Torques in Ultra Scaled MRAM Devices** Simone Fiorentini[1,2], Johannes Ender[1,2], Roberto L. de Orio[2], Siegfried Selberherr[2], Wolfgang Goes[3] and Viktor Sverdlov[1,2] [1]Christian Doppler Laboratory for Nonvolatile Magnetoresistive Memory and Logic at the [2]Institute for Microelectronics, TU Wien (Austria) [3]Silvaco Europe Ltd., Cambridge (United Kingdom)
	Session 2A: Tunneling and Steep Slope Devices (Rooms Andalucía 1+2) Chairperson: N. Seoane (Univ. Of Santiago de Compostela, Spain)
11:50 – 12:10	**Assessment of Lateral and Vertical Tunneling FETs Based on 2D Material for Ultra-Low Power Logic Applications** Yuanchen Chu[1,3], Shang-Chun Lu[2,3], Michael Povolotskyi[1], Gerhard Klimeck[1], Umberto Ravaioli[2], Tomás Palacios[3] and Mohamed Mohamed[4]

	[1]School of Electrical and Computer Engineering, Purdue University (USA) [2]Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign (USA) [3]Microsystems Technology Laboratories, MIT (USA) [4]MIT Lincoln Laboratory (USA)
12:10 – 12:30	**Full Quantum Simulation of Shockley-Read-Hall Recombination in p-i-n and Tunnel Diodes** A. Pilotto, P. Dollfus, J. Saint-Martin and M. Pala Université Paris-Saclay, CNRS (France)
12:30 – 12:50	**On the Feasibility of DoS-Engineering for Achieving Sub-60 mV Subthreshold Slope in MOSFETs** J.M. Gonzalez-Medina[1], Z. Stanojevic[1], Z. Hou[2], Q. Zhang[2], W. Li[2], J. Xu[2] and M. Karner[1] [1]Global TCAD Solutions (Austria) [2]HiSilicon Technologies (China)
12:50 – 13:10	**Theoretically probing the relationship between barrier length and resistance in Al/AlOx/Al tunnel Junctions** Paul Lapham and Vihar Georgiev Device Modelling Group, James Watt School of Engineering, University of Glasgow (Scotland, United Kingdom)
	Session 1B: Power Electronics (Room Andalucía 3) Chairperson: S.J. Cooke (Electronics Science and Technology Division, Naval Research Laboratory Washington, USA) and F. Triozon (CEA-LETI, France)
10:30 – 11:00	**Analysis of Uniaxial Stress Impact on Drift Velocity of 4H-SiC by Full Band Monte Carlo Simulation** T. Nishimura, K. Eikyu, K. Sonoda and T. Ogata Renesas Electronics Corporation (Japan)
11:00-11:30	**Calculation of the mobility in Al2O3/GaN electron channel: Effect of p-doping and comparison with experiments** B. Rrustemi[1,2], F. Triozon[1], M.-A. Jaud[1], W. Vandendaele[1] and G. Ghibaudo[2] [1]Univ. Grenoble Alpes, CEA, LETI (France) [2]Univ. Grenoble Alpes, IMEP-LAHC MINATEC (France)
11:30-12:00	**TCAD-based design and verification of the components of a 200 V GaN-IC platform** P. Vudumula[1], T. Cosnier[2], O. Syshchyk[2], B. Bakeroot[3] and S. Decoutere[2] [1]Department of Electrical Engineering, KU Leuven (Belgium) [2]IMEC (Belgium) [3]Center for Microsystems Technology, IMEC and Ghent University (Belgium)
12:00 – 12:30	**Development of an Ensemble Monte Carlo Simulator for High-Power Semiconductor Devices with Self-Consistent Electromagnetism and GPU Implementation** S.J. Cooke[1] and M.G. Ancona[1,2] [1]Electronics Science and Technology Division, Naval Research Laboratory Washington (USA) [2]Department of Electrical and Computer Engineering, Florida State University (USA)
12:30 – 13:00	**Investigation of effects of lateral boundary conditions on current filament movements in Trench-Gate IGBTs**

	Takeshi Suwa Toshiba Electronic Devices & Storage Corporation (Japan)
13:10 – 14:30	**Lunch**
	Session 3A: Process Simulation (Rooms Andalucía 1+2) Chairperson: T. Herrmann (Global Foundries, Germany)
14:30 – 14:50	**3D Feature-Scale Modeling of Highly Selective Fluorocarbon Plasma Etching** Frâncio Rodrigues[1], Luiz Felipe Aguinsky[1], Andreas Hössinger[2] and Josef Weinbub[1] [1]Christian Doppler Laboratory for High Performance TCAD at the Institute for Microelectronics, TU Wien (Austria) [2]Silvaco Europe Ltd. (United Kingdom)
14:50 – 15:10	**DTCO Flow for Air Spacer Generation and its Impact on Power and Performance at N7** L. Filipovic[1], O. Baumgartner[2], J. Piso[1], J. Bobinac[1], T. Reiter[1], G. Strof[2], G. Rzepa[2], Z. Stanojevic[2] and M. Karner[2] [1]Institute for Microelectronics, TU Wien (Austria) [2]Global TCAD Solutions GmbH. (Austria)
15:10 – 15:30	**GPGPU MCII for high-energy implantation** Fumie Machida[1], Hiroo Koshimoto[1], Yasuyuki Kayama[1], Alexander Schmidt[2], Inkook Jang[2], Satoru Yamada[1] and Dae Sin Kim[2] [1]DS2 Lab, DS center, Samsung R&D Institute Japan (Japan) [2]CSE Team, Innovation Center, Samsung Electronics Co., Ltd. (Korea)
15:30 – 15:50	**Modeling Electrical Resistivity of CrSi Thin Films** K. Sonoda[1], N. Shiraishi[2], K. Maekawa[1], N. Ito[1], E. Hasegawa[2] and T. Ogata[1] [1]Renesas Electronics Corporation, Ibaraki (Japan) [2]Renesas Electronics Corporation, Kumamoto (Japan)
15:50 – 16:10	**Modeling Non-Ideal Conformality during Atomic Layer Deposition in High Aspect Ratio Structures** Luiz Felipe Aguinsky[1], Frâncio Rodrigues[1], Xaver Klemenschits[2], Lado Filipovic[2], Andreas Hössinger[3] and Josef Weinbub[1] [1]Christian Doppler Laboratory for High Performance TCAD at the [2]Institute for Microelectronics, TU Wien (Austria) [3]Silvaco Europe Ltd. (United Kingdom)
	Session 3B: Machine Learning I (Room Andalucía 3) Chairperson: V. Georgiev (Univ. Of Glasgow, UK)
14:30 – 14:50	**A Novel Methodology for Neural Compact Modeling Based on Knowledge Transfer** Ye Sle Cha, Junghwan Park, Chanwoo Park, Soogine Chong, Chul-Heung Kim, Chang-Sub Lee, Intae Jeong and Hyunbo Cho Research & Development Center, Alsemy Inc. (Korea)
14:50 – 15:10	**Graph-based Compact Modeling of CMOS Transistors for Efficient Parameter Extraction: A Machine Learning Approach** Amol D. Gaidhane, Ziyao Yang and Yu Cao School of ECEE, Arizona State University (USA)
15:10 – 15:30	**Hierarchical Mixture-of-Experts Approach for Neural Compact Modeling of MOSFETs** Chanwoo Park, Premkumar Vincent, Soogine Chong, Junghwan Park, Ye Sle Cha and Hyunbo Cho

	Research & Development Center, Alsemy Inc. (Korea)
15:30 – 15:50	**Quantum Element Method for Multi-Dimensional Nanostructures Enabled by a Projection-based Learning Algorithm** Martin Veresko and Ming-C. Cheng Dept. of ECE, Clarkson University (USA)
15:50 – 16:10	**Vertical GaN Diode BV Maximization through Rapid TCAD Simulation and ML-enabled Surrogate Model** Albert Lu[1], Jordan Marshall[1], Yifan Wang[2], Ming Xiao[2], Yuhao Zhang[2] and Hiu Yung Wong[1] [1]Electrical Engineering, San Jose State University (USA) [2]Center for Power Electronics Systems, Virginia Polytechnic Institute and State University (USA)
16:10 – 16:30	**Coffee break**
	Session 4A: TCAD Models (Rooms Andalucía 1+2) Chairperson: S. Martinie (CEA-LETI, France)
16:30 – 16:50	**Hierarchical Modeling for TCAD Simulation of Short-Channel 2D Material-Based FETs** Luca Silvestri[1], Mattias Palsgaard[2], Reto Rhyner[1], Martin Frey[1], Jess Wellendorff[2], Søren Smidstrup[2], Ronald Gull[1] and Karim El Sayed[3] [1]Synopsys Switzerland LLC (Switzerland) [2]Synopsys Denmark ApS (Denmark) [3]Synopsys Inc. (USA)
16:50 – 17:10	**Modeling of SiC Transistor with Counter-doped Channel** Pratik B. Vyas, Ashish Pal, Stephen Weeks, Joshua Holt, Aseem K. Srivastava, Ludovico Megalini, Siddarth Krishnan, Michael Chudzik, El Mehdi Bazizi, and Buvna Ayyagari-Sangamalli Applied Materials (USA)
17:10 – 17:30	**Towards a DFT-based layered model for TCAD simulations of MoS_2** L. Donetti, C. Marquez, C. Navarro, C. Medina-Bailon, J. L. Padilla, C. Sampedro and F. Gamiz Departamento de Electrónica and CITIC, Universidad de Granada (Spain)
	Session 4B: Machine Learning II (Room Andalucía 3) Chairperson: G. Klimeck (Purdue University, USA)
16:30 – 16:50	**A Simulation Physics-Guided Neural Network for Predicting Semiconductor Structure with Few Experimental Data** QHwan Kim[1], Sunghee Lee[1], Ami Ma[1], Jaeyoon Kim[1], Hyeon-Kyun Noh[1], Kyu Baik Chang[1], Wooyoung Cheon[1], Shinwook Yi[1], Jaehoon Jeong[1], BongSeok Kim[2], Young-Seok Kim[2] and Dae Sin Kim[1] 1Computational Science and Engineering Team (Korea) 2Memory Metrology and Inspection Technology Team, Samsung Electronics Co. (Korea)
16:50 – 17:10	**Building Robust Machine Learning Force Fields by Composite Gaussian Approximation Potentials** Diego Milardovich, Dominic Waldhoer, Markus Jech, Al-Moatasem Bellah El-Sayed and Tibor Grasser Institute for Microelectronics, Technische Universität Wien (Austria)
17:10 – 17:30	**Surrogate models for device design using sample efficient Deep Learning** Rutu Patel, Nihar R. Mohapatra and Ravi S. Hegde

	Indian Institute of Technology Gandhinagar (India)
17:30 – 17:50	**TCAD Augmented Generative Adversarial Network for Optimizing a Chip-level Size Mask Layout Design in the HARC Etching Process** Hyoungcheol Kwon[1,3], Hwiwon Seo[3], Hyunsuk Huh[2], Felipe Iza[1], Dongyean Oh[3], Sung Kye Park[3] and Seonyong Cha[3] [1]The Wolfson School of Mechanical, Electrical and Manufacturing Engineering, Loughborough University (United Kingdom) [2]Department of Mechanical Engineering, POSTECH (Republic of Korea) [3]R&D Devision, SK Hynix Inc. (Republic of Korea)
18:00 – 19:00	**Get-together cocktail**
19:00 – 19:20	**Bus departure for private Alhambra guided tour**
19:30 – 22:00	**Exclusive visit to Alhambra and Palace of the Emperor Charles V**

Wednesday, September 7th

09:00 - 09:15	**SISPAD 2023 Presentation – Satofumi Souma, Kobe University**
09:15 – 10:00	**Mono-material TMD-based heterostructures for nanoelectronics applications** F. Gity, Tyndall National Institute (Ireland)
10:00 – 10:20	**Coffee break**
	Session 5A: Two-Dimensional Materials (Rooms Andalucía 1+2) Chairperson: F. Gity (Tyndall National Institute, Ireland)
10:20 - 10:40	**Electron-phonon calculations using a Wannier-based supercell approach: applications to the monolayer MoS_2 mobility** Jonathan Backman, Youseung Lee and Mathieu Luisier Integrated Systems Laboratory, ETH Zürich (Switzerland)
10:40 - 11:00	**Image-Force Barrier Lowering in Top- and Side-contacted Two-Dimensional Materials** Emeric Deylgat[1,2,3], Edward Chen[4], Massimo V. Fischetti[1], Bart Sorée[3,5,6] and William G. Vandenberghe[1] [1]Department of Materials Science and Engineering, The University of Texas at Dallas (USA) [2]Department Physics, KU Leuven (Belgium) [3]Imec (Belgium) [4]Corporate Research, TSMC Ltd. (Taiwan) [5]Department of Electrical Engineering, KU Leuven (Belgium) [6]Department of Physics, Universiteit Antwerpen (Belgium)
11:00 - 11:20	**The impact of electron phonon scattering on transport properties of topological insulators: a first principles quantum transport study** Elaheh Akhoundi[1,2], Michel Houssa[1,2] and Aryan Afzalian[1] [1]Imec (Belgium) [2]Dept. of Physics and Astronomy, KU Leuven (Belgium)
11:20 – 11:40	**Theoretical Study of Carrier Transport in Two-dimensional Transition Metal Dichalcogenides for Field-Effect Transistor Applications** Sanjay Gopalan, Maarten L. Van de Put and Massimo V. Fischetti Department of Materials Science and Engineering, The University of Texas at Dallas (USA)

	Session 5B: High-Frequency Devices (Room Andalucía 3) Chairperson: K. Sonoda (Renesas Electronics, Japan)
10:20 - 10:40	**Massively Parallel FDTD Full-Band Monte Carlo Simulations of Electromagnetic THz pulses in p-doped Silicon at Cryogenic Temperatures** C. Jungemann[1], F. Meng[2], M. D. Thomson[2] and H. G. Roskos[2] [1]Chair of Electromagnetic Theory, RWTH Aachen University (Germany) [2]Physikalisches Institut, Goethe-Universität Frankfurt (Germany)
10:40 - 11:00	**TCAD simulation of microwave circuits: the Doherty amplifier** S. Donati Guerrieri, E. Catoggio and F. Bonani Dipartimento di Elettronica e Telecomunicazioni, Politecnico di Torino (Italy)
11:00 - 11:20	**TCAD-Based RF Performance Prediction and Process Optimization of 3D Monolithically Stacked Complementary FET** Shu-Wei Chang[1], Jia-Hon Chou[2], Wen-Hsi Lee[1], Yao-Jen Lee[3] and Darsen D. Lu[4] [1]Department of Electrical Engineering, National Cheng Kung University (Taiwan) [2]M.S. Degree Program on Nano-IC Engineering, Department of Electrical Engineering, National Cheng Kung University (Taiwan) [3]Department of Electrical Engineering, National University of Kaohsiung (Taiwan) [4]Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University (Taiwan)
11:20 – 11:40	**THz Gain Compression in Nanoscale FinFETs** Mathias Pech and Dirk Schulz Chair for High Frequency Techniques TU Dortmund (Germany)
	Session 6A: Atomistic and Ab-initio Modeling (Rooms Andalucía 1+2) Chairperson: J. Cao (ETH Zürich, Switzerland)
11:50 – 12:10	**Ab initio study of electron mobility in V2O5 via polaron hopping** R. Defrance[1,2], B. Sklénard[1], M. Guillaumont[2], J. Li[1] and M. Freyss[3] [1]Univ. Grenoble Alpes, CEA, Leti (France) [2]LYNRED, 364 Avenue de Valence, (France) [3]CEA, DES, IRESNE, DEC (France)
12:10 – 12:30	**Efficient Atomistic Simulations of Lateral Heterostructure Devices with Metal Contacts** Mincheol Shin and Kanghyun Joo School of Electrical Engineering, Korea Advanced Institute of Science and Technology (Rep. of Korea)
12:30 – 12:50	**Impact of random alloy fluctuations on carrier transport in (In,Ga)N quantum well systems: Linking atomistic tight-binding models to drift-diffusion** M. O'Donovan[1,2], P. Farrell[3], T. Streckenbach[3], T. Koprucki[3] and S. Schulz[2,1] [1]Tyndall National Institute, University College Cork (Ireland) [2]Department of Physics, University College Cork (Ireland) [3]Weierstrass Institute (WIAS) (Germany)
12:50 – 13:10	**Robust Cryogenic Ab-initio Quantum Transport Simulation for L_G=10nm Nanowire** Tom Jiao and Hiu Yung Wong Electrical Engineering, San Jose State University (USA)

	Session 6B: Circuit Simulation and Compact Modeling (Room Andalucía 3) Chairperson: E. Guichard (Silvaco, USA)
11:50 – 12:10	**A compact physical expression for the static drain current in heterojunction barrier CNTFETs** Manojkumar Annamalai and Michael Schröter Chair for Electron Devices and Integrated Circuits, Technische Universität Dresden (Germany)
12:10 – 12:30	**Enabling medium thick gate oxide devices in 22FDX(r) technology for switch and high-performance amplifier application** Tom Herrmann[1], Alban Zaka[1], Zhixing Zhao[1], Binit Syamal[1], Wafa Arfaoui[1], Ruchil Jain[1], Ming-Cheng Chang[1], Sameer Jain[2] and Shih Ni Ong[3] [1]GlobalFoundries Dresden (Germany) [2]GlobalFoundries Malta (Malta) [3]GlobalFoundries Singapore (Singapore)
12:30 – 12:50	**Non-Quasi-Static Modeling and Methodology in Fully Depleted SOI MOSFET for L-UTSOI model** S. Martinie[1], O. Rozeau[1], HyoEun Park[2], Sungjoon Park[2], P. Scheer[3], S.El Ghouli[3], A. Juge[3], H. Lee[2] and T. Poiroux[1] [1]Univ. Grenoble Alpes, CEA, LETI (France) [2]Samsung (South Korea) [3]STMicroelectronics (France)
12:50 – 13:10	**String-level Compact Modeling Based on Channel Electrostatic Potential for Dynamic Operation of 3D Charge Trapping Flash Memories** Sunghwan Cho[1] and Byoungdeog Choi[2] [1]Department of Semiconductor and Display Engineering, Sungkyunkwan University (Republic of Korea) [2]Department of Electrical and Computer Engineering, Sungkyunkwan University (Republic of Korea)
13:10 – 14:30	**Lunch**
14:30 – 15:15	**Semiconductor workforce development through immersive simulations on nanoHUB.org** Gerhard Klimeck, Purdue University (USA)
15:15 – 17:15	**Coffee Break + Poster Session (Hall)** **P1: 1D Drift-Diffusion transport in 2D-material based FETs with vertical contacts** A. Toral-Lopez, E.G. Marin, F. Pasadas, M.C. Pardo, J. Cuesta, F.G. Ruiz and A. Godoy PEARL Laboratory, Dpto. de Electrónica y Tecnología de Computadores, Universidad de Granada (Spain) **P2: A generalizable, uncertainty-aware neural network potential for GeSbTe with Monte Carlo dropout** Sung-Ho Lee[1], Valerio Olevano[2] and Benoît Sklénard[1,3] [1]Univ. Grenoble Alpes, CEA, Leti (France) [2]Université Grenoble Alpes (France) [3]CNRS, Institut Néel (France)

	P3: A Machine-learning-based Multi-Objective Optimization of Stacked Nanosheet Transistors for sub-3nm technology node Haoqing Xu[1,2], Weizhuo Gan[1,2], Lei Cao[1,2], Huaxiang Yin[1,2] and Zhenhua Wu[1,2] [1]Institute of Microelectronics, Chinese Academy of Sciences (China) [2]School of Integrated Circuits, University of Chinese Academy of Sciences (China) **P4: Ab Initio Quantum Transport Simulations of Monolayer GeS Nanoribbons** Mislav Matić and Mirko Poljak Computational Nanoelectronics Group, Faculty of Electrical Engineering and Computing, University of Zagreb (Croatia) **P5: Acceleration of Semiconductor Device Simulation Using Compact Charge Model** Kwang-Woon Lee and Sung-Min Hong School of Electrical Engineering and Computer Science, Gwangju Institute of Science and Technology (Republic of Korea) **P6: Atomic-scale study of silane and hydrogen adsorptions competition during Si epitaxy** Laureline Treps, Jing Li and Benoît Sklénard Univ. Grenoble Alpes, CEA, Leti (France)
15:15 – 17:15	**P7: Automatic Grid Refinement for Thin Material Layer Etching in Process TCAD Simulations** Christoph Lenz[1], Paul Manstetten[2], Andreas Hössinger[3] and Josef Weinbub[1] [1]Christian Doppler Laboratory for High Performance TCAD at the [2]Institute for Microelectronics, TU Wien (Austria) [3]Silvaco Europe Ltd. (United Kingdom) **P8: Comparative Analysis of NBTI Modeling Frameworks - BAT and Comphy** Aseer Israr Ansari, Nilotpal Choudhury, Narendra Parihar and Souvik Mahapatra Department of Electrical Engineering, Indian Institute of Technology Bombay (India) **P9: Disorders in delta-layer tunnel junctions** Juan P. Mendez and Denis Mamaluy Sandia National Laboratories (USA) **P10: Ferroelectric FDSOI FET Modeling for Memory and Logic Applications** Swetaki Chatterjee[1], Shubham Kumar[2], Amol Gaidhane[3], Chetan Kumar Dabhi[4], Yogesh S. Chauhan[2] and Hussam Amrouch[1] [1]Chair of Semiconductor Test and Reliability, University of Stuttgart (Germany) [2]Indian Institute of Technology (India) [3]Arizona State University (USA) [4]University of California (USA)

15:15 – 17:15	**P11: Hierarchical Simulation of Nanosheet Field Effect Transistor: NESS Flow** D. Nagy[1,2], A. Rezaei[1], N. Xeni[1], T. Dutta[1], F. Adamu-Lema[1,2], I. Topaloglu[1], V. P. Georgiev[1] and A. Asenov[1,2] [1]Device Modelling Group, School of Engineering, University of Glasgow (Scotland, UK) [2]Semiwise Ltd. (Scotland, UK) **P12: Improvement of On-cell Metrology Using Spectral Imaging with TCAD Modeling** Byungseong Ahn[1], Kwangseok Lee[1], Jaehun Yang[1], Jiseong Doh[1], Jaehoon Jeong[1], Minseok Kim[2], Yeonjeong Kim[2], Jongchul Kim[2], Hyung Keun Yoo[2] and Dae Sin Kim[1] [1]Computational Science and Engineering Team, [2]Foundry Metrology & Inspection Team / Device Solution Business Samsung Electronics Co., Ltd. (Republic of Korea) **P13: Modeling Optical Second Harmonic Generation for Oxide Semiconductor Interface Characterization** Binit Mallick[1], Dipankar Saha[1], Anindya Dutta[2] and Swaroop Ganguly[1] [1]Department of Electrical Engineering, Indian Institute of Technology (India) [2]Department of Chemistry, Indian Institute of Technology (India) **P14: Modeling Thermal Effects in STT-MRAM** Tomáš Hadámek[1], Wolfgang Goes[2], Siegfried Selberherr[3] and Viktor Sverdlov[3] [1]Christian Doppler Laboratory for Nonvolatile Magnetoresistive Memory and Logic at the [3]Institute for Microelectronics, TU Wien (Austria) [2]Silvaco Europe Ltd. (United Kingdom) **P15: Monolithic TCAD Simulation of Phase-Change (PCM/PRAM) + Ovonic Threshold Switch (OTS) Selector Device** M. Thesberg[1], Z. Stanojevic[1], O. Baumgartner[1], C. Kernstock[1], D. Leonelli[2], M. Barci[2], X. Wang[3], X. Zhou[3], H. Jiao[3], G. L. Donadio[4], D. Garbin[4], T. Witters[4], S. Kundu[4], H. Hody[4], R. Delhougne[4], G. S. Kar[4] and M. Karner[1] [1]Global TCAD Solutions (Austria) [2]Huawei Technologies R&D Belgium N.V. (Belgium) [3]HiSilicon Technologies (China) [4]Imec (Belgium) **P16: Performance of Vertical Gate-All-Around Nanowire p-MOS Transistors Determined by Boron Depletion during Oxidation** Chiara Rossi[1], Alexander Burenkov[1], Peter Pichler[1], Eberhard Bär[1], Paweł Piotr Michałowski[2], Jonas Müller[3] and Guilhem Larrieu[3] [1]Fraunhofer Institute for Integrated Systems and Device Technology (IISB) (Germany) [2]Łukasiewicz Research Network – Institute of Microelectronics and Photonics (Poland) [3]LAAS-CNRS, Université de Toulouse (France)

15:15 – 17:15	**P17: Polarization Switching Characteristics in AFE/FE Double-Layer Devices** Mengqi Fan and Fei Liu and Xiaoyan Liu School of Integrated Circuits, Peking University (China) **P18: Scattering matrix-based low computational cost model for the device and circuit co-simulation of phosphorene tunnel field-effect transistors** Kosuke Yamaguchi and Satofumi Souma Department of Electrical and Electronic Engineering, Kobe University (Japan) **P19: Sensitivity enhancement in OCD metrology by optimizing azimuth angle based on the RCWA simulation** Hyunsuk Choi[1], Kwangseok Lee[1], Jiseong Doh[1], Jaehoon Jeong[1], Minseok Kim[2], Yeonjeong Kim[2], Jongchul Kim[2], Hyung Keun Yoo[2] and Dae Sin Kim[1] [1]Computationl Science and Engineering Team [2]Foundry Metrology & Inspection Technology Team Samsung Electronics Co., Ltd. (Republic of Korea) **P20: Strong quantization of current-carrying electron states in δ-layer systems** Denis Mamaluy and Juan P. Mendez Sandia National Laboratories (USA) **P21: Non-local Transport Effects in Semiconductors Under Low-Field Conditions** M.G. Ancona[1,2] and S.J. Cooke[2] [1]Department of Electrical and Computer Engineering, Florida State University (USA) [2]Electronics Science and Technology Division, Naval Research Laboratory Washington (USA)
18:30 – 19:00	**Bus departure and transfer to Albaycín**
19:00 – 20:30	**Guided visit across the Albaycín**
20:30 – 22:30	**Gala dinner at *Palacio de los Córdova***

Thursday, September 8th

09:15 – 10:00	**Tunneling leakage in ultrashort-channel MOSFETs—From atomistics to continuum modeling** Raphaël J. Prentki, Nanoacademic Technologies Inc. (Canada)
10:00 – 10:20	**Coffee break**
	Session 7A: Qubits (Rooms Andalucía 1+2) Chairperson: S. Souma (Kobe University, Japan)

10:20 - 10:40	**A Generalizable TCAD Framework for Silicon FinFET Spin Qubit Devices with Electrical Control** Qian Ding[1], Andreas V. Kuhlmann[2], Andreas Fuhrer[3] and Andreas Schenk[1] [1]Integrated Systems Lab, ETH Zurich (Switzerland) [2]Department of Physics,University of Basel (Switzerland) [3]Quantum Technology & Computing IBM Research Europe – Zurich (Switzerland)
10:40 - 11:00	**A Simulation Methodology for Superconducting Qubit Readout Fidelity** Hiu Yung Wong[1], Yaniv Jacob Rosen[2], Kristin Beck[2], Prabjot Dhillon[1] and Jonathan L Dubois[2] [1]Electrical Engineering, San Jose State University (USA) [2]Lawrence Livermore National Laboratory (USA)
11:00 - 11:20	**On the noise-sensitivity of 2-qubit entangling gates implemented with a silicon quantum dot system** Hoon Ryu Korea Institute of Science and Technology Information (Republic of Korea)
11:20 – 11:40	**RF simulation platform of qubit control using FDSOI technology for quantum computing** H. Jacquinot[1], R. Maurand[2], G. Troncoso Fernandez Bada[2], B. Bertrand[1], M. Cassé[1], Y. M. Niquet[2], S. de Franceschi[2], T. Meunier[3] and M. Vinet[1] [1]Univ. Grenoble Alpes, CEA, LETI (France) [2]Univ. Grenoble Alpes, CEA, IRIG/DEPHY (France) [3]CNRS Institut Néel (France)
	Session 7B: Reliability I (Room Andalucía 3) Chairperson: W. Vandenberghe (University of Texas at Dallas, USA)
10:20 - 10:40	**A Physics-based TCAD Framework for NBTI** Ravi Tiwari[1], Meng Duan[2], Mohit Bajaj[3], Denis Dolgos[4], Lee Smith[5], Hiu Yung Wong[6] and Souvik Mahapatra[1] [1]Department of Electrical Engineering, Indian Institute of Technology Bombay (India) [2]Synopsys Northern Europe Ltd. (UK) [3]Synopsys India Private Limited (India) [4]Synopsys Switzerland LLC (Switzerland) [5]Synopsys Inc. (USA) [6]San Jose State University (USA)
10:40 - 11:00	**A Stochastic Simulation Framework for TDDB in MOS Gate Insulator Stacks** Satyam Kumar, Tarun Samadder, Dimple Kochar and Souvik Mahapatra Department of Electrical Engineering, Indian Institute of Technology Bombay (India)
11:00 - 11:20	**CARAT - A Reliability Analysis Framework for BTI-HCD Aging in Circuits** Prasad Gholve[1], Payel Chatterjee[1], Chaitanya Pasupuleti[1], Hussam Amrouch[2], Narendra Gangwar[1], Shouvik Das[1], Uma Sharma[1], Victor M van Santen[2] and Souvik Mahapatra[1] [1]Department of Electrical Engineering, Indian Institute of Technology Bombay (India) [2]Institute of Computer Architecture and Computer Engineering, University of Stuttgart (Germany)
11:20 – 11:40	**Trap and Self-Heating Effect Based Reliability Analysis to Reveal Early Aging Effect in Nanosheet FET**

	Sunil Rathore, Rajeewa Kumar Jaisawal, P. N. Kondekar, and Navjeet Bagga VLSI Design and Nano-scale Computational Lab, Electronics and Communication Engineering Department, PDPM-IIITDM (India)
	Session 8A: Memories (Rooms Andalucía 1+2) Chairperson: Dong-Yean Oh (SK Hynix, Republic of Korea)
11:50 – 12:10	**A Physical Model for Long Term Data Retention Characteristics in 3D NAND Flash Memory** Rashmi Saikia and Souvik Mahapatra Department of Electrical Engineering, Indian Institute of Technology Bombay (India)
12:10 – 12:30	**An Atomistic Modelling Framework for Valence Change Memory Cells** M. Kaniselvan, M. Luisier and M. Mladenovic Integrated Systems Laboratory, ETH Zurich (Switzerland)
12:30 – 12:50	**An inner gate as enabler for vertical pitch scaling in macaroni channel gate-all-around 3-D NAND flash memory** D. Verreck, A. Arreghini, G. Van den Bosch and M. Rosmeulen Imec (Belgium)
12:50 – 13:10	**Insights into Few-Atom Conductive Bridging Random Access Memory Cells with a Combined Force-Field / ab initio Scheme** J. Aeschlimann, M. H. Bani-Hashemian, F. Ducry, A. Emboras and M. Luisier Integrated Systems Laboratory, ETH Zürich (Switzerland)
	Session 8B: Reliability II (Room Andalucía 3) Chairperson: Carlos Márquez (University of Granada, Spain)
11:50 – 12:10	**A Dynamic Current Hysteresis Model for Thin-Film Transistors** Yu Li[1], Xiaoqing Huang[1], Congwei Liao[1], Runsheng Wang[2], Shengdong Zhang[1], Lining Zhang[1] and Ru Huang[2] [1]School of ECE, Peking University (China) [2]School of Integrated Circuits Peking University (China)
12:10 – 12:30	**Analysis of 1/f and G-R Noise in Phosphorene FETs** Adhithan Pon and Avirup Dasgupta DiRac Lab, Department of ECE, Indian Institute of Technology (India)
12:30 – 12:50	**Microstructural Impact on Electromigration Reliability of Gold Interconnects** H. Ceric, R. L. de Orio and S. Selberherr Institute for Microelectronics, TU Wien (Austria)
12:50 – 13:10	**Reliability of TCAD Study for HfO_2-doped Negative Capacitance FinFET with Different Material Specific Dopants** Rajeewa Kumar Jaisawal, Sunil Rathore, P.N. Kondekar and Navjeet Bagga VLSI Design and Nano-scale Computational Lab, Electronics and Communication Engineering Department, PDPM-IIITDM (India)
13:10 – 14:30	**Lunch**
	Session 9A: Advanced Methods for Numerical Calculations (Rooms Andalucía 1+2) Chairperson: J. Lorenz (Fraunhofer IISB, Germany)
14:30 – 14:50	**A proposal of quantum computing algorithm to solve Poisson equation for nanoscale devices under Neumann boundary condition** Shingo Matsuo and Satofumi Souma

	Department of Electrical and Electronic Engineering, Kobe University (Japan)
14:50 – 15:10	**Approximate H-Transformation for Numerical Stabilization of a Deterministic Boltzmann Transport Equation Solver Based on a Spherical Harmonics Expansion** Suhyeong Cha and Sung-Min Hong School of Electrical Engineering and Computer Science, Gwangju Institute of Science and Technology (Republic of Korea)
15:10 – 15:30	**Coupling a phase field model with an electro-thermal solver to simulate PCM intermediate resistance states for neuromorphic computing** O. Cueto, A. Trabelsi, C.Cagli and M.C Cyrille Univ. Grenoble Alpes, CEA, LETI, DCOS, LSM (France)
15:30 – 15:50	**Discontinuous Galerkin Concept for Quantum-Liouville Type Equations** Valmir Ganiu and Dirk Schulz Chair for High Frequency Technique TU Dortmund (Germany)
15:50 – 16:10	**Hybrid 2D/3D Mesh for Efficient Device Simulation of a Locally Tilted Vertical NAND String** Geon-Tae Jang and Sung-Min Hong School of Electrical Engineering and Computer Science, Gwangju Institute of Science and Technology (Republic of Korea)
	Session 9B: Nanodevices and Interconnects (Room Andalucía 3) Chairperson: L. Filipovic (TU Wien, Austria)
14:30 – 14:50	**Stacking devices in a vertical nanowire, a feasible option to implement smaller ICs** E. Amat, A. del Moral, J. Bausells and F. Perez-Murano Institute of Microelectronics of Barcelona (IMB-CNM, CSIC) (Spain)
14:50 – 15:10	**A comprehensive on-current variability Pelgrom-based model for FinFET, NWFET and NSFET transistors** Julian G. Fernandez, Natalia Seoane, Enrique Comesaña and Antonio García-Loureiro CiTIUS, University of Santiago de Compostela (Spain)
15:10 – 15:30	**Forked Contact and Dynamically-Doped Nanosheets to Enhance Si and 2D Materials Device at the limit of Scaling** Aryan Afzalian, Zubair Ahmed and Julien Ryckaert Imec (Belgium)
15:30 – 15:50	**On the Switching Limits of Top-Gated Carbon Nanotube Field-Effect Transistors** A. Sanchez-Soares[1], C. Gilardi[2], Q. Lin[2], T. Kelly[1], S.-K. Su[3], G. Fagas[4], J.C. Greer[5], G. Pitner[6] and E. Chen[3] [1]EOLAS Designs, Grenagh, Co. (Republic of Ireland) [2]Stanford University (USA) [3]Corporate Research, TSMC (Taiwan). [4]Tyndall National Institute, University College Cork (Ireland) [5]University of Nottingham Ningbo China (China) [6]Corporate Research, TSMC (USA)
15:50 – 16:10	**28nm FDSOI MEOL Parasitic Capacitance Segmentation using Electrical Testing and Semiconductor Process Modeling** B. Vianne[1], B. Guillo-Lohan[1], V. Quenette[1], B. Legoix[1] and B. Vincent[2] [1]STMicroelectronics (France) [2]Coventor, a Lam Research Company (France)

16:10 – 16:30	**Coffee break**
	Session 10A: Sensors and Optoelectronics (Rooms Andalucía 1+2) Chairperson: S. Donati (Politecnico di Torino, Italy)
16:30 – 16:50	**Simulation-based study on characteristics of dual vertical transfer gates in sub-micron pixels for CMOS image sensors** Wook Lee[1], Seonghoon Ko[1], Uihui Kwon[1], HyunChul Kim[2] and Dae Sin Kim[1] [1]Computational Science and Engineering Team, Innovation Center [2]Semiconductor R&D Center Device Solution Business, Samsung Electronics Co. (Republic of Korea)
16:50 – 17:10	**Compact Model of a Metal Oxide Molecule Sensor for Self-Heating Control** Yohsuke Shiiki[1], Shintaro Nagata[2], Tsunaki Takahashi[2], Takeshi Yanagida[2] and Hiroki Ishikuro[1] [1]Electronics and Electrical Engineering, Keio University (Japan) [2]Department of Applied Chemistry, The University of Tokyo (Japan)
17:10 – 17:30	**Deriving a novel methodology for Nano-BioFETs and analyzing the effect of high-k oxides on the amino-acids sensing application** Rakshita Dhar[1], Naveen Kumar[1], Cesar Pascual Garcia[2] and Vihar Georgiev[1] [1]Device Modelling Group, James Watt School of Engineering, University of Glasgow (Scotland, UK) [2]Nano-Enabled Medicine and Cosmetics group, Materials Research and Technology Department, Luxembourg Institute of Science and Technology (LIST) (Luxembourg)
17:30 – 17:50	**Ab initio modeling of photodetectors based on van der Waals heterostructures** Jiang Cao, Sara Fiore, Cedric Klinkert and Mathieu Luisier Integrated Systems Laboratory, ETH Zürich (Switzerland)
	Session 10B: Interfaces, Traps and Defects (Room Andalucía 3) Chairperson: C. Jungemann (RWTH Aachen, Germany)
16:30 – 16:50	**Characterization and Modeling of Drain Lag using a Modified RC Network in the ASM-HEMT Framework** Mohammad Sajid Nazir[1], Ahtisham Pampori[1], Raghvendra Dangi[1], Pragya Kushwaha[2], Ekta Yadav[2], Santanu Sinha[2] and Yogesh Singh Chauhan[1] [1]Department of Electrical Engineering, Indian Institute of Technology Kanpur (India) [2]Micro Electronics Group, Space Applications Centre, Indian Space Research Organisation (India)
16:50 – 17:10	**Efficient and accurate defect level modelling in monolayer MoS_2 via GW+DFT with open boundary conditions** Guido Gandus[1,2], Youseung Lee[1], Leonard Deuschle[1], Daniele Passerone[2] and Mathieu Luisier[1] [1]Integrated Systems Laboratory, ETH Zürich (Switzerland) [2]nanotech@surfaces, EMPA (Switzerland)
17:10 – 17:30	**Prediction of the evolution of defects induced by the heated implantation process: Contribution of kinetic Monte Carlo in a multi-scale modeling framework** P.L. Julliard[1,2], A. Johnsson[3], R. Demoulin[2], R. Monflier[2], A. Jay[2], D. Rideau[1], P. Pichler[3], A. Hémeryck[2] and F. Cristiano[2] [1]STMicroelectronics (France)

	[2]LAAS-CNRS, Université de Toulouse, CNRS (France) [3]Fraunhofer Institute for Integrated Systems and Device Technology (IISB) (Germany)
17:30 – 17:50	**Surface scattering impact on Si/TiSi2 contact resistance** Kantawong Vuttivorakulchai, Mohammad Ali Pourghaderi, Yoon-Suk Kim, Uihui Kwon and Dae Sin Kim Computational Science and Engineering Team, Innovation Center, Device Solution Business, Samsung Electronics Co. (Republic of Korea)
17:50 – 18:00	**Conference Closing**