SISPAD 2019

Wednesday-Friday, 4-6 September

Palazzo di Toppo Wassermann
Università degli Studi di Udine
Udine, Italy

Conference Program

International Conference on Simulation of Semiconductor Processes and Devices

Technical Sponsor

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IEEE

Electron Devices Society

Special Thanks to Our Sponsors:

Welcome

We would like to welcome you to the 2019 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2019), to Udine and to Palazzo di Toppo Wassermann, a premises of the Università degli Studi di Udine.

The Università degli Studi di Udine is proud to host the 24th edition of SISPAD, whose longevity stems from its ability to stay at the forefront of the hot topics in the field of simulation of semiconductor processes and devices. This is the reason why, for almost a quarter of a century, leading scientists, researchers, and students have chosen the SISPAD as the forum where to share the latest developments in advanced modelling of novel semiconductor devices, processes and equipment for integrated circuits and nanoelectronics.

This year's conference program consists of 3 plenary invited presentations, 3 invited talks, 64 contributed papers and 26 posters, that were selected out of 136 submitted abstracts. These presentations have been arranged in 13 sessions and one poster session, and the conference program covers two and a half days, namely from the opening on Wednesday September 4th to the closing right after lunch on Friday September 6th.

The program of the conference is augmented and complemented by a tutorial entitled " Atomistic simulations for nanoelectronic and optoelectronic devices" and a workshop entitled "Leti seminar on Simulation and Modeling for Emerging Non-Volatile Memories", both held on Tuesday September 3rd in the afternoon.

This conference has been made possible thanks to the support, expertise and work of many people.

We are very thankful to the members of the Steering Committee for their support and useful suggestions, to the members of the Technical Program Committee for their commitment and expertise to critically analyse many submitted abstracts and then select those that now form the technical program of this conference. We are particularly thankful to the Chairman of the previous European SISPAD edition, Jürgen Lorenz, and to the Chairman of last year edition, Leonard Franklin Register, for sharing their expertise in the conference organization and for many useful words of advice. We would like to thank our invited speakers for sharing their renowned expertise with the attendees of the conference.

We are also thankful to the Università degli Studi di Udine, that is hosting the conference in Palazzo di Toppo Wassermann, to the Conference Secretariat (Centro Congressi Internazionale, Torino) and particularly to Giulia Datta and Rosaria Petrolo for their professionalism and tireless commitment, to the offices and people of the IEEE Electron Devices Society and IEEE Meetings, Conferences & Events Department, who helped us in several respects in the organization of the conference.

We extend our sincere thanks to our sponsors for their generous contributions.

We are finally deeply thankful to all authors and presenters for having chosen SISPAD to share their scientific work, and to each and every attendee of the conference, who literally made this conference possible.

David Esseni
Conference Chair

Pierpaolo Palestri and Denis Rideau
Technical Program Co-Chairs

Francesco Driussi
Publication Chair

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Jeff Wu, TSMC, Taiwan

Tutorial on Atomistic simulations for nanoelectronic and optoelectronic devices

Advances in fabrication of materials enabled the development of new nano-materials, nano-structures and nano-devices, thus opening the way to the “nano-era”. In this framework, dependable simulation approaches at the atomic scale, able to handle new nano-materials (e.g. 2D materials), interfaces and quantum effects are a fundamental tool in the engineering of these new structures/devices.

This tutorial will introduce to first-principle atomistic simulations based on Density Functional Theory (DFT), with special emphasis on applications to materials for nano/opto electronics. The tutorial will explore the potentialities of DFT techniques in characterizing new materials and structures, including defects and their electrical and optical properties, and will show how to bridge the results of simulations with experiments and spectroscopic signatures.

Program

14.00-15.00 “Reproducing, understanding, predicting: first-principle simulations meet TCAD”
Layla Martin-Samos, CNR-IOM

15.00-16.00 “Basic of DFT simulations: opportunities and limits”
Prof. Paolo Giannozzi, Università degli Studi di Udine

16.00-16.30 Coffee break

16.30-17.30 “Linking excited states to spectroscopic signatures with many-body perturbation theory”
Prof. Paolo Umari, Università degli Studi di Padova

Leti seminar on Simulation and Modeling for Emerging Non-Volatile Memories

Leti is a technology research institute at CEA Tech located in Grenoble (France) and a recognized global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions. Committed to innovation, its teams create differentiating solutions for Leti’s industrial partners.

Leti has invested heavily and for many years in its place as a premier research institute worldwide. It is now home to hi-tech microelectronics cleanrooms, a range of advanced characterization tools that are unique in the world. As a world leader in innovation, Leti develops new non-volatile memory solutions, for which simulation and modeling are essential activities to support technology developments and device behavior understanding.

Leti invite you to attend its ‘Advanced Simulations for Emerging Non-Volatile Memory Technologies’ seminar as an official satellite event of the 2019 IEEE SISPAD conference. This event will be held on Friday, September 3rd from 5:00 PM to 7:30 PM, Palazzo di Toppo Wassermann.

Program

17.00 Welcome and Introduction – T. Poiroux (CEA-Leti)

17.05 Innovative non-volatile memory technologies: a revolution for the storage towards a memory that thinks – G. Navarro (CEA-Leti)

17.20 Electro-thermal and material simulations for PCM – O. Cueto (CEA-Leti)

17.35 Multiphase field method for the simulation of the complex phase changes in PCM
R. Bayle (ST Micro)

17.50 Invited talk: Self-consistent TCAD simulation of chemical reactions within electronic devices. Application to CBRAM and OxRAM – (Silvaco, speaker to be defined)

18.10 Questions/Answers

18.30 Networking cocktail

Wednesday September 4th, 2019

09.00-09.10	Conference Opening	
09.10-10.00	Plenary invited: Neuro-Inspired Computing with Nanoelectronic Devices: Experimental Progresses and Modeling Opportunities, Shimeng Yu *Room T9*	
10.00-10.20	Coffee break	
10.20-12.20	S1: Reliability of devices and interconnects *Room T9*	S2: Advanced methods for numerical calculations *Room T4*
12.20-13.30	Lunch	
13.30-15.40	S3: Memories *Room T9*	S4: Quantum transport in nanoscale devices *Room T4*
15.40-16.10	Coffee break	
16.15-18.00	Poster session *Velario*	
18.00-19.00	Cocktail reception – Palazzo di Toppo Wassermann	

Thursday September 5th, 2019

09.00-09.10	Presentation of SISPAD 2020	
09.10-10.00	Plenary invited: Modeling Silicon CMOS devices for quantum computing, Yann-Michel Niquet *Room T9*	
10.00-10.20	Coffee break	
10.20-12.20	S5: Atomistic and ab-initio modeling *Room T9*	S6: Compact and circuit oriented modelling S7: Temperature related effects *Room T4*
12.20-13.30	Lunch	
13.30-15.40	S8: Power devices and wide band-gap semiconductors *Room T9*	S9: Technology Optimization *Room T4*
15.40-16.00	Coffee break	
16.00-17.40	S10: Beyond CMOS materials and devices *Room T9*	S11: Interfaces, traps and defects *Room T4*
19.30-22.30	Gala Dinner - Palazzo Kechler	

Friday September 6th, 2019

09.10-10.00	Plenary invited: Compact Modeling Perspective – Bridge to Industrial Applications Mitiko Miura-Mattausch *Room T9*	
10.00-10.20	Coffee break	
10.20-12.30	S12: Process modelling *Room T9*	S13: Sensors and optoeletronic devices *Room T4*
12.30-13.30	Lunch	

Wednesday September 4

09.00-09.10 **Conference opening**

09.10-10.00 **Plenary invited**
Room T9 Neuro-Inspired Computing with Nanoelectronic Devices: Experimental Progresses and Modeling Opportunities
Shimeng Yu,
Georgia Institute of Technology

10.00-10.20 **Coffee break**

Room T9 **Session 1**
Reliability of devices and interconnects
Chairpersons: L. Filipovic, Technische Universität Wien, Austria,
F. Driussi, University of Udine

10.20-10.40 1.1 - 3D Kinetic Monte Carlo Simulation of Electromigration in Multi-layer Interconnects
Linlin Cai, Wangyong Chen, Xing Zhang, Yudi Zhao, and Xiaoyan Liu
Institute of Microelectronics, Peking University, Beijing, China

10.40-11.00 1.2 - Metallic ions drift in hybrid bonding integration modeling, towards the evolution of failure criterion
MANZANAREZ Hervé, MOREAU Stéphane, CUETO Olga
Univ. Grenoble Alpes, CEA, LETI, Grenoble France.

11.00-11.20 1.3 - TCAD Framework to Estimate the NBTI Degradation in FinFET and GAA NSFET Under Mechanical Strain
Ravi Tiwari[1], Narendra Parihar[1], Karansingh Thakor[1], Hiu-Yung Wong[2], and Souvik Mahapatra[1]
[1]Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai, India
[2]San Jose State University, San Jose, CA, USA

11.20-11.40 1.4 - A Stochastic Hole Trapping-Detrapping Framework for NBTI, TDDS and RTN
Sharang Bhagdikar and Souvik Mahapatra
Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai, India

11.40-12.00 1.5 - TCAD-Enabled Machine Learning Defect Prediction to Accelerate Advanced Semiconductor Device Failure Analysis
Chea-Wei Teo[1] [2], Kain Lu Low[1], Vinod Narang[2], and Aaron Voon-Yew Thean[1],
[1]Department of Electrical and Computer Engineering, National University of Singapore, Singapore
[2]Device Analysis Lab, Advanced Micro Devices Pte Ltd, Singapore

12.00-12.20 1.6 - TCAD Augmented Machine Learning for Semiconductor Device Failure Trouble shooting and Reverse Engineering
Y. S. Bankapalli and H. Y. Wong
Electrical Engineering, San Jose State University, San Jose, CA, USA

Room T4 **Session 2**
Advanced methods for numerical calculations
Chairpersons: A. Godoy, University of Granada, Spain, D. Connelly, Atomera, USA

10.20-10.40 2.1 - On the Simulation of Plasma Waves in HEMTs and the Dyakonov-Shur Instability
1st Christoph Jungemann, 2nd Tobias Linn, 3rd Zeinab Kargar
Chair of Electromagnetic Theory, RWTH Aachen University, Aachen, Germany

10.40-11.00 2.2 - Exact Correction of the Self-Force Problem in Monte Carlo Device Simulation
Andrea Ghetti
Technology Development, Micron Technology Inc., Vimercate, Italy

11.00-11.20 2.3 - A Robust Simulation Method for Breakdown with Voltage Boundary Condition Utilizing Negative Time Constant Information
Shigetaka Kumashiro, Tatsuya Kamei, Akira Hiroki, Kazutosi Kobayashi
Kyoto Institute of Technology, Matsugasaki, Sakyo-ku, Kyoto, Japan

11.20-11.40 2.4 - Extending the Numerov Process to the Semiconductor Transport Equations
Nicolò Speciale[1], Rossella Brunetti[2], Massimo Rudan[1]
[1]"E. De Castro" Advanced Research Center on Electronic Systems (ARCES) and Department DEI, University of Bologna,
[2]FIM Department, University of Modena and Reggio Emilia, Modena

11.40-12.00 2.5 - Implementation of Automatic Differentiation to Python-based Semiconductor Device Simulator
Tsutomu Ikegami, Koichi Fukuda, Junichi Hattori
National Institute of Advanced Industrial, Science and Technology (AIST), Tsukuba, Japan

12.00-12.20 2.6 - Deep Neural Network for Generation of the Initial Electrostatic Potential Profile
Seung-Cheol Han and Sung-Min Hong
School of Electrical Engineering and Computer Science, Gwangju Institute of Science and Technology, Gwangju, Republic of Korea

12.20-13.30 **Lunch**

Room T9 **Session 3**
Memories
Chairperson: Seong-dong Kim, SK Hynix, South Korea

13.30-14.00 Invited presentation
The evolution of TCAD as virtual design solutions: Fully atomistic TCAD, TCAD assi sted AI, TCAD mediated DTCO and real-time TCAD
Dae Sin Kim
Samsung Electronics, Hwasung-si, Republic of Korea

14.00-14.20 3.1 - Multiscale Modeling of Charge Trapping in Molecule Based Flash Memories
Oves Badami[1], Toufik Sadi[2], Vihar Georgiev[1], Fikru Adamu-Lema[1], Vasanthan Thiruna vukkarasu[1], Jie Ding[3], Asen Asenov[1]
[1]School of Engineering, University of Glasgow, Glasgow, United Kingdom
[2]School of Science, Aalto University, Aalto, Finland
[3]College of Electrical and Power Engineering, Taiyuan University of Technology, China

14.20-14.40 3.2 - TCAD Model for Ag-$GeSe_3$-Ni CBRAM Devices
Kiraneswar Muthuseenu[1], E. Carl Hylin[2], Hugh J. Barnaby[1], Priyanka Apsangi[1], Michael N. Kozicki[1], Garrett Schlenvogt[2], Mark Townsend[2]
[1]School of Electrical, Computer and Energy, Engineering, Arizona State University, Tempe, AZ, USA
[2]Silvaco Inc., North Chelmsford, MA, USA

14.40-15.00 3.3 - Comprehensive Comparison of Switching Models for Perpendicular Spin-Transfer Torque MRAM Cells
Simone Fiorentini[1], Roberto Orio[1], Wolfgang Goes[2], Johannes Ender[1], Viktor Sverdlov[1]
[1]Christian Doppler Laboratory for Magnetoresistive Nonvolatile Memory and Logic Institute for Microelectronics, TU Wien Vienna, Austria
[2]Silvaco Europe Ltd Cambridge, United Kingdom

15.00-15.20 3.4 - 3D TCAD Model for Poly-Si Channel Current and Variability in Vertical NAND Flash Memory
D. Verreck[1], A. Arreghini[1], F. Schanovsky[2], Z. Stanojevic[2], K. Steiner[2], F. Mitterbauer[2], M. Karner[2], G. Van den bosch[1], A. Furn´emont[1],
[1]imec, Leuven, Belgium,
[2]Global TCAD Solutions GmbH., Vienna, Austria

15.20-15.40 3.5 - Optimization of select gate transistor in advanced 3D NAND memory cell
Jin Cho, Derek Kimpton, Eric Guichard
Silvaco, Inc, Santa Clara, CA, USA

Room T4 **Session 4**
Quantum transport in nanoscale devices
Chairperson: W.Vandenberghe, University of Texas at Dallas, USA

13.40-14.00 4.1 - A Hybrid Mode-Space/Real-Space Scheme for DFT+NEGF Device Simulations
F. Ducry, M. H. Bani-Hashemian, and M. Luisier
Integrated Systems Laboratory (ETH Zurich)

14.00-14.20 4.2 - Full band quantum transport modelling with EP and NEGF methods: application to nanowire transistors
M. Pala[1], D. Esseni[2]
[1]C2N, Universit´e Paris-Saclay, Palaiseau, France
[2]DPIA, University of Udine, Udine, Italy

14.20-14.40 4.3 - A Quantum Element Reduced Order Model
Ming-C. Cheng
Dept. of ECE, Clarkson University, Potsdam, NY, USA

14.40-15.00 4.4 - Quantum Mechanical Simulations of the Impact of Surface Roughness on Nanowire TFET performance
Yunhe Guan[1], ZunChao Li[1], Hamilton Carrillo-Nuñez[2], Vihar P. Georgiev[2], Asen Asenov[2]
[1]School of Microelectronics, Xi'an Jiaotong University, Xi'an, China
[2]School of Engineering, University of Glasgow, Glasgow, United Kingdom

15.00-15.20 4.5 - Efficient Coupled-mode space based Non-Equilibrium Green's Function Approach for Modeling Quantum Transport and Variability in Vertically Stacked SiNW FETs
V. Thirunavukkarasu[1], H. Carrillo-Nunez[1], F. D. Alema[1], S. Berrada[1], O. Badami[1], C. Medina-Bailón[1], T. Datta[1], J. Lee[1], Y. Guen[2], V. Georgiev[1] and A. Asenov[1]
[1]School of Engineering, University of Glasgow, Glasgow, Scotland, UK.
[2]Department of Electrical Engineering, Xian Chiao Tung University, People Republic of China.

15.20-15.40 4.6 - Surface Roughness Scattering in NEGF using self-energy formulation
Oves Badami, Salim Berrada, Hamilton Carrillo-Nunez, Cristina Medina-Bailon, Vihar Georgiev, Asen Asenov
School of Engineering, University of Glasgow, Glasgow, United Kingdom

15.40-16.00 **Coffee break**

16.00-17.30 **Poster Session**
Velario

P01 - Impact of BEOL Design on Self-heating and Reliability in Highly-scaled FinFETs
Jaehee Choi, Udit Monga, Yonghee Park, Hyewon Shim[1], Uihui Kwon, Sangwoo Pae[1], Dae Sin Kim
Semiconductor R&D Center, [1]Foundry Business, Samsung Electronics Co., Ltd., Hwa sung-si, Gyeonggi-do, Korea

P02 - Modeling 1/f and Lorenzian noise in III-V MOSFETs
E. Caruso[1], F. Bettetti[2], L. Del Linz[2], D. Pin[2], M. Segatto[2], P. Palestri[2]
[1]Tyndall National Institute, University College Cork, Cork, Ireland
[2] DPIA, University of Udine, Italy.

P03 - Investigation of TCAD Calibration for Saturation and Tail Current of 6.5kV IGBTs
Takeshi Suwa and Shigeaki Hayase
Toshiba Electronic Devices & Storage Corporation, Kawasaki, Japan

P04 - Simulation of Statistical NBTI Degradation in 10nm Doped Channel pFinFETs
F, Adamu-Lema, V. Georgiev, Member, IEEE, and A. Asenov, Fellow, IEEE
Device Modeling Group, University of Glasgow, Glasgow, UK

P05 - A SPICE Compatible Compact Model for Process and Bias Dependence of HCD in HKMG FDSOI MOSFETs
Uma Sharma and Souvik Mahapatra
Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai, India

P06 - Quantum Transport Simulations of the Zero Temperature Coefficient in Gate-all-around Nanowire pFETs
Hyeongu Lee, Junbeom Seo, Mincheol Shin
School of Electrical Engineering Korea Advanced Institute of Science and Technology Daejeon, Republic of Korea

P07 - Electro-Thermal Analysis and Edge Termination Techniques of High Current β-Ga2O3 Schottky Rectifiers
Ribhu Sharma[1], Erin Patrick[2], Jiancheng Yang[3], Fan Ren[3], Mark Law[2], Stephen Pearton[1]
[1]Material Science and Engineering, University of Florida, Gainesville, Fl, USA
[2]Electrical and Computer Engineering, University of Florida, Gainesville, Fl, USA
[3]Chemical Engineering) University of Florida, Gainesville, Fl, USA

P08 - Thermal Conductivity of Silicon Nanowire Using Landauer Approach for Thermoe lectric Applications
Ming-Yi Lee[1], Min-Hui Chuang[1], Yiming Li[1] [3], Seiji Samukawa[2] [3]
[1]Institute of Communications Engineering, National Chiao Tung University, Hsinchu, Taiwan
[2]Institute of Fluid Science and WPI-AIMR, Tohoku University,Aoba-ku, Sendai, Japan
[3]Center for mmWave Smart RadarSystems and Technologies, National Chiao Tung University, His

P09 - Simulation of Chemically Reacting Flow in Plasma Native Oxide Cleaning Process
Seung-Min Ryu[1], Yunho Kim[1], Dylan Pederson[1], Jonghyun Lee[2], Youngkwon Kim[2], Laxminarayan L. Raja[1], Jiho Uh[2], Sang-Jin Choi[2]
[1]Dept. of Aerospace Engineering and Engineering Mechanics The University of Texas at Austin Austin, U.S.
[2]Memory Technology Innovation Team Samsung Electronics Hwaseong-si, South Korea

P10 - Simulation of deep level transient spectroscopy using circuit simulator with deep level trap model implemented by Verilog-A language
Koichi Fukuda[1], Junichi Hattori[1], Hidehiro Asai[1], Mitsuaki Shimizu[1], Tamotsu Hashizume[2]
[1]National Institute Of Adivanced Industrial Science and Technology (AIST), Tsukuba, Japan
[2]Research Center for Integrated, Quantum Electronics (RCIQE), Hokkaido University, Hokkaido, Japan

P11 - A New Computer-Aided Calibration Technique of Physics Based IGBT & Power-Diode Compact Models with Verilog-A Implementation
Arnab Biswas, Daniel Ludwig, Maria Cotorogea
Infineon Technologies AG, Neubiberg, Germany

P12 - First-principles investigation of paramagnetic centers in P2O5 based glasses
Luigi Giacomazzi[1], Layla Martin-Samos[2], Nicolas Richard[3], Matjaz Valant[1], Nadege Ollier[4]
[1]Materials Research Laboratory, (University of Nova Gorica), Nova Gorica, Slovenia
[2]CNR-IOM Democritos, Trieste, Italy
[3]DAM-DIF CEA, Arpajon, France
[4]LSI-IRAMIS, CEA, Palaiseau, France

P13 - Theoretical Study of the Edge Effect of Dumbbellshape Graphene Nanoribbon with a Dual Electronic Properties by First-principle Calculations
Qinqiang Zhang[1], Takuya Kudo[2], Jowesh Gounder[2], Ying Chen[3], Ken Suzuki[3], Hideo Miura[3]
[1]Dept. of Finemechanics, Tohoku University, Sendai, Japan
[2]Dept. of Finemechanics, Graduate School of Engineering, Sendai, Japan
[3]Fracture and Reliability Research Institute, Tohoku University, Sendai, Japan

P14 - A new wet etching method for black phosphorus layer number engineering: experiment, modeling and DFT simulations
Teren Liu[1], Tao Fang[1 2 3], Karen Kavanagh[4], Hongyu Yu5, Guangrui (Maggie) Xia[1]
[1]Department of Materials Engineering, University of British Columbia, Vancouver, Canada
[2]Department of Physics and Astronomy, University of British Columbia, Vancouver, Canada
[3]Stewart Blusson Quantum Matter Institute, University of British Columbia, Vancouver, Canada
[4]Department of Physics, Simon Fraser University, Vancouver, Canada
[5]School of Microelectronics, line 3: Southern University of Science of Technology, Shenzhen, China

P15 - OFF Current Suppression by Gate-gontrolled Strain in The N-type GaAs Piezoelectric FinFETs
Yuxiong Long[1], Jun Z. Huang[2], Zhongming Wei[1], Jun-Wei Luo[1], Xiangwei Jiang[1],
[1]Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China
[2]MaxLinear Inc., Carlsbad, CA, USA

P16 - Numerical Investigation of the Photogating Effect in $MoTe_2$ Photodetectors
J.M. Gonzalez-Medina[1 2], E.G. Marin[1 3], A. Toral-Lopez[1 2], F. G. Ruiz[1 2], A. Godoy[1 2]
[1]Dpto. Electrónica, Universidad de Granada, Spain
[2]Pervasive Electronics Advanced Research Laboratory, CITIC, Universidad de Granada, Spain
[3]Dipartimento di Ingegneria dell'Informazione, Università di Pisa, Italy.

P17 - Physical Insights into the Transport Properties of RRAMs Based on Transition Metal Oxides
Toufik Sadi[1], Oves Badami[2], Vihar Georgiev[2], Jie Ding[3], Asen Asenov[2]
[1]Engineered Nanosystems Group, School of Science, Aalto University, AALTO, Finland
[2]School of Engineering, Electronic and Nanoscale Engineering, University of Glasgow, Glasgow, Scotland, UK
[3]College of Electrical and Power Engineering, Taiyuan University of Technology, China.

P18 - Molecular Dyanamics Simulation of Thermal Chemical Vapor Deposition for Hydrogenated Amorphous Silicon on Si (100) Substrate by Reactive Force-Field
Naoya Uene[1], Takuya Mabuchi[2], Masaru Zaitsu[3], Shigeo Yasuhara[3], Takashi Tokumasu[4]
[1]Graduate school of engineering Tohoku university Sendai, Japan
[2]Frontier research institute for interdisciplinary sciences Tohoku university Sendai, Japan
[3]Research & development Japan advanced chemicals ltd. Sagamihara, Japan
[4]Institute of fluid science Tohoku university Sendai, Japan

P19 - Device-to-circuit modeling approach to Metal – Insulator – 2D material FETs targeting the design of linear RF applications
Alejandro Toral-López[1], Francisco Pasadas[2], Enrique G. Marín[1], Alberto Medina-Rull[1], Francisco J. G. Ruiz[1], David Jiménez[2], Andrés Godoy[1]
[1]Departamento de Electrónica y Tecnología de Computadores, Universidad de Granada, Granada, Spain
[2]Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Barcelona, Spain

P20 - Simulation and Investigation of Electrothermal Effects in Heterojunction Bipolar Transistors
Xujiao Gao, Gary Hennigan, Lawrence Musson, Andy Huang, Mihai Negoita
Electrical models and simulation, Sandia National Laboratories, Albuquerque, USA

P21 - Variability of Threshold Voltage Induced by Work-Function Fluctuation and Random Dopant Fluctuation on Gate-All-Around Nanowire nMOSFETs
Wen-Li Sung, Min-Hui Chuang, Yiming Li
Department of Electrical and Computer Engineering, Center for mmWave Smart Radar System and Technologies, National Chiao Tung University, Hsinchu, Taiwan.

P22 - A First Principle Insight into Defect Assisted Contact Engineering at the Metal-Graphene and Metal-Phosphorene Interfaces
Jeevesh Kumar, Adil Meersha, Ansh and Mayank Shrivastava
Department of Electronic Systems Engineering, Indian Institute of Science, Bengaluru, India

P23 - Transient Simulation of Field-Effect Biosensors: How to Avoid Charge Screening Effect
Kyoung Yeon Kim, Byung-Gook Park
Department of Electrical and Computer Engineering, Seoul National University, Seoul, South Korea

P24 - Electronic and structural properties of interstitial titanium in crystalline silicon from first-principles simulations
Gabriela Herrero-Saboya[1] [2], Layla Martin-Samos[3], Anne Hemeryck[2], Denis Rideau[4], Nicolas Richard[1]
[1]CEA, DAM, DIF Arpajon, France,
[2]LAAS-CNRS, Université de Toulouse, Toulouse, France
[3]CNR-IOM / Democritos National Simulation Center, c/o SISSA, Trieste, Italy
[4]STMicroelectronics, Crolles, France

P25 - Hybrid method for electromagnetic modelling of coherent radiation in semiconductor lasers.
Mateusz Marek Krysicki, Bartlomiej Salski, Pawel Kopyt
Warsaw University of Technology, Institute of Radioelectronics and Multimedia Technology, Warsaw, Poland

P26 - NEGF simulations of stacked silicon nanosheet FETs for performance optimization
Hong-Hyun Park[1], Woosung Choi[1], Mohammad Ali Pourghaderi[2], Jongchol Kim[2], Uihui Kwon[2], Dae Sin Kim[2]
[1]Device Laboratory Samsung Semiconductor Inc. San Jose, California, USA
[2]Semiconductor R&D Center Samsung Electronics, Hwasung-si, Gyeonggi-do, Korea

18.00-19.00 **Cocktail Reception** – Palazzo di Toppo Wassermann

Thursday September 5

09.00-09.10 **Presentation of SISPAD 2020**

09.10-10.00 **Plenary invited**
Room T9 Modeling Silicon CMOS devices for quantum computing
Venitucci Benjamin, Li Jing, Bourdet Léo, Niquet Yann-Michel
CEA/IRIG/MEM/L_Sim, Grenoble, France

10.00-10.20 **Coffee break**

Room T9 **Session 5**
Atomistic and ab-initio modeling
Chairperson: L. Martin-Samos, SISSA,Trieste, Italy

10.20-10.40 5.1 - ATOMOS: An ATOmistic MOdelling Solver for dissipative DFT transport in ultra-scaled HfS2 and Black phosphorus MOSFETs
Aryan Afzalian, Geoffrey Pourtois
Imec, Leuven, Belgium

10.40-11.00 5.2 - Atomistic modeling of nanoscale ferroelectric capacitors using a density functional theory and non-equilibrium Green's-function method
Daniele Stradi, Ulrik G. Vej-Hansen, Petr A. Khomyakov, Maeng-Eun Lee, Gabriele Penazzi, Anders Blom, Jess Wellendorff, Søren Smidstrup, Kurt Stokbro
Synopsys Denmark ApS, Copenhagen, Denmark

11.00-11.20 5.3 - Trigonal Tellurium Nanostructure Formation Energy and Band gap
Aaron Kramer[1], Maarten L. Van de Put[2], Christopher L. Hinkle[3], and William G. Vanden berghe[2]
[1]Department of Physics and [2]Department of Materials Science and Engineering, University of Texas at Dallas, Richardson, Texas, USA
[3]Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA

11.20-11.40 5.4 - Defect creation and Diffusion under electric fields from first-principles: the prototypical case of silicon dioxide
N. Salles[1 3], L. Martin-Samos[1], S. de Gironcoli[2], L. Giacomazzi[1 3], M. Valant[3], A Hemeryck[4], P. Blaise[5], B. Sklenard[5], N. Richard[6]
[1]CNR-IOM/Democritos National Simulation Center, Istituto Officina dei Materiali, c/o SISSA, Italy
[2]SISSA, Italy
[3]Materials Research Laboratory, University of Nova Gorica, Slovenija
[4]LAAS-CNRS, Université de Toulouse, CNRS, Toulouse,France
[5]Univ. Grenoble Alpes, CEA, LETI, Grenoble, France
[6]CEA, DAM, DIF, Arpajon, France

11.40-12.00 5.5 - Effective work-function tuning of $TiN/HfO_2/SiO_2$ gate-stack; a density functional tight binding study
Hesameddin Ilatikhameneh[1], Hong-Hyun Park[1], Zhengping Jiang[1], Woosung Choi[1], Mohammad Ali Pourghaderi[2], Jongchol Kim[2], Uihui Kwon[2], Dae Sin Kim[2]
[1]Device lab, Samsung Semiconductor Inc., San Jose, California, USA
[2]Semiconductor Research and Development Center, Samsung Electronics, Hwasung-si, Korea

Room T4 **Session 6**
Compact and circuit oriented modelling
Chairperson: S.Martinie, CEA-LETI, Grenoble, France

10.20-10.40 6.1 - Single Event Transient Compact Model for FDSOI MOSFETs Taking Bipolar Amplification and Circuit Level Arbitrary Generation Into Account
Neil Rostand[1], Sébastien Martinie[2], Joris Lacord[2], Olivier Rozeau[2], Thierry Poiroux[2], Guillaume Hubert[1]
[1]DPHY ONERA, Toulouse, France
[2]DCOS CEA-LETI, Grenoble, France

10.40-11.00 6.2 - From devices to circuits: modelling the performance of 5nm nanosheets
Andrew R. Brown[1], Liping Wang[1], Plamen Asenov[1], Fabian J. Klüpfel[2], Binjie Cheng[1], Sébastien Martinie[3], Olivier Rozeau[3], Sylvain Barraud[3], Jean-Charles Barbé[3], Campbell Millar[1], Jürgen K. Lorenz[2]
[1]Synopsys Northern Europe Ltd. Glasgow, UK
[2]Fraunhofer IISB, Erlangen, Germany
[3]CEA Leti,38054 Grenoble, France

11.00-11.20 6.3 - Compact Modelling of Resistive Switching Devices based on the Valence Change Mechanism
Camilla La Torre[1], Alexander F. Zurhelle[1], Stephan Menzel[2]
[1]Instutitut für Werkstoffe der Elektrotechnik II, RWTH Aachen University & JARA-FIT, Aachen, Germany
[2]Peter Grünberg Institut (PGI-7), Forschungszentrum Juelich GmbH & JARA-FIT, Juelich, Germany

Room T4 **Session 7**
Temperature related effects
Chairperson: Y. Li, National Chiao Tung University, Taiwan

11.20-11.40 7.1 - Effect of Stacking Faults on the Thermoelectric Figure of Merit of Si Nanowires
Kantawong Vuttivorakulchai, Mathieu Luisier, and Andreas Schenk
Integrated Systems Laboratory ETH Zürich, Zürich, Switzerland

11.40-12.00 7.2 - Modeling of Temperature-Dependent MOSFET Aging
Fernando Ávila Herrera[1], Mitiko Miura-Mattausch[1], Hideyuki Kikuchihara[1], Takahiro Iizuka[1], Hans Jürgen Mattausch[1], Hirotaka Takatsuka[2]
[1]HiSIM Research Center, Hiroshima University, Higashihiroshima, Japan
[2]Technology Development Division, Mie Fujitsu Semiconductor Limited, Yokoyama, Japan

12.00-12.20 7.3 - TCAD analysis of FinFET temperature-dependent variability for analog applications
S. Donati Guerrieri, F. Bonani, G. Ghione
Dipartimento di Elettronica e Telecomunicazioni, Politecnico di Torino, ITALY

12.20-13.30 **Lunch**

Room T9 **Session 8**
Power devices and wide band-gap semiconductors
Chairperson: S. Reggiani, University of Bologna, Italy

13.30-14.00 Invited presentation
Nitride electronics exploiting ultrawide bandgap AlN
Debdeep Jena
Cornell University, USA

14.00-14.20 8.1 - Numerical Investigation of the Leakage Current and Blocking Capabilities of High-Power Diodes with Doped DLC Passivation Layers
Luigi Balestra[1], Susanna Reggiani[1], Antonio Gnudi[1], Elena Gnani[1], Giorgio Baccarani[1], Jagoda Dobrzynska[2], Jan Vobecký[2]
[1]ARCES and DEI, University of Bologna, Bologna, Italy.
[2]ABB Switzerland Ltd.Semiconductors, Lenzburg, Switzerland.

14.20-14.40 8.2 - Influence of Accurate Electron Drift Velocity Modelling on the Electrical Characteristics in GaN-on-Si HEMTs
Korbinian Reiser[1] [2], John Twynam[1], Christian Eckl[1], Helmut Brech[1], Robert Weigel[2]
[1]Infineon Technologies AG, Regensburg, Germany
[2]Institute for Electronics Engineering, Friedrich-Alexander-Universitaet Erlangen-Nuernberg, Erlangen-Nuernberg, Germany

14.40-15.00 8.3 - TCAD Simulations Combined with Free Carrier Absorption Experiments Revealing the Physical Nature of Hydrogen-Related Donors in IGBTs
Andreas Korzenietz[1], Frank Hille[2], Franz-Josef Niedernostheide[2], Christian Sandow[2], Gerhard Wachutka[1], Gabriele Schrag[1]
[1]Chair for Physics of Electrotechnology, Technical University of Munich Munich, Germany
[2]Infineon Technologies AG Neubiberg, Germany

15.00-15.20 8.4 - TCAD investigation of zero-cost high voltage transistor architectures for logic memory circuits
Jordan Locati[1], Christian Rivero[1], Julien Delalleau[1], Vincenzo Della Marca[2], Karine Coulié[2], Jordan Innocenti[1], Olivier Paulet[1], Arnaud Regnier[1], Stephan Niel[1]
[1]STMicroelectronics, Rousset, France
[2]Aix-Marseille University, CNRS, IM2NP UMR 7334, Marseille, France

15.20-15.40 8.5 - Barrier Engineering of Lattice Matched AlInGaN/ GaN Heterostructure Toward High Performance E-mode Operation
Niraj Man Shrestha[1], Chao-Hsuan Chen[2], Zuo-Min Tsai[3], Yiming Li[3], Jenn-Hawn Tarng[3], Seiji Samukawa[4]
[1]Department of Electrical and Computer Engineering and Center for mmWave Smart Radar System and Technologies, National Chiao Tung University, Hsinchu, Taiwan
[2]Institute of Communications Engineering, National Chiao Tung University, Hsinchu, Taiwan
[3]Institute of Communications Engineering, Department of Electrical and Computer Engineering, and Center for mmWave Smart Radar System and Technologies, National Chiao Tung University, Hsinchu, Taiwan
[4]Center for mmWave Smart Radar System and Technologies, National Chiao Tung University, Hsinchu, Taiwan and Institute of Fluid Science, Tohoku University, Sendai, Japan

Room T4 **Session 9**
Technology Optimization
Chairperson: V. Moroz, Synopsys, USA

14.00-14.20 9.1 - RF performance improvement on 22FDX® platform and beyond
Tom Herrmann, Alban Zaka, Nandha Kumar Subramani, Zhixing Zhao, Steffen Lehmann, Yogadissen Andee
GLOBALFOUNDRIES Dresden Dresden, Germany

14.20-14.40 9.2 - Leakage Performance Improvement in Multi-Bridge-Channel Field Effect Transistor (MBCFET) by Adding Core Insulator Layer
Saehoon Joung[1] [2] - Student Member -, SoYoung Kim[2]- Senior Member - IEEE
[1]Samsung Electronics Co. Foundry Division, Yield Enhancement, Process Integration Engineering Group, Ltd Kiheung, Republic of Korea
[2]College of Information and Communication Engineering,Sungkyunkwan University, Suwon,Gyeounggi-do,Republic of Korea

14.40-15.00 9.3 - Impact of MOL/BEOL Air-Spacer on Parasitic Capacitance and Circuit Performance at 3 nm Node
Ashish Pal, Sushant Mittal, El Mehdi Bazizi, Angada Sachid, Mehdi Saremi, Benjamin Colombeau, Gaurav Thareja, Samuel Lin, Blessy Alexander, Sanjay Natarajan and Buvna Ayyagari
Applied Materials, Santa Clara, USA

15.00-15.20 9.4 - Scaling-aware TCAD Parameter Extraction Methodology for Mobility Prediction in Tri-gate Nanowire Transistors
Cristina Medina-Bailon[1], Tapas Dutta[1], Fabian Klupfel[2], Sylvain Barraud[3], Vihar Georgiev[1], Jürgen Lorenz[2], Asen Asenov[1]
[1]School of Engineering, University of Glasgow, Glasgow, United Kingdom
[2]Fraunhofer Institut für Integrierte, Systeme und Bauelementetechnologie, Erlangen, Germany
[3]CEA, LETI, MINATEC campus and University Grenoble Alpes, Grenoble, France

15.40-16.00 **Coffee break**

Room T9 **Session 10**
Beyond CMOS materials and devices
Chairperson: A. Schenk, ETH Zurich, Switzerland

16.00-16.20 10.1 - DFT study of graphene doping due to metal contacts
P. Khakbaz[1], F. Driussi[1], A. Gambi[1], P. Giannozzi[2], S. Venica[1], D. Esseni[1], A. Gahoi[3], S. Kataria[3], M.C. Lemme[3] [4]
[1]DPIA, University of Udine, Udine, Italy
[2]DMIF, University of Udine, Udine, Italy
[3]RWTH Aachen University, Aachen, Germany
[4]AMO GmbH, Advanced Microelectronic Center, Aachen, Germany

16.20-16.40 10.2 - Device and Circuit Level Gate Configuration Optimization for 2D Material Field-Effect Transistors
Devin Verreck[1], Goutham Arutchelvan[1] [2], Marc M. Heyns[1] [2], Iuliana P. Radu[1]
[1]imec, Leuven, Belgium,
[2]Department of Materials Engineering, KU Leuven, Leuven, Belgium

16.40-17.00 10.3 - Accurate and Efficient Dynamic Simulations of Ferroelectric Based Electron Devices
T. Rollo[1], L. Daniel[2], D. Esseni[1]
[1]DPIA, University of Udine, Italy
[2]Electrical Engineering and Computer Science Depart., MIT, Cambridge, MA, USA

17.00-17.20 10.4 - Precise Transient Mechanism of Steep Subthreshold Slope PN-Body-Tied SOI-FET and Proposal of a New Structure for Reducing Leakage Current upon Turn-off
Takayuki Mori[1], Jiro Ida[1], Hiroki Endo[1], Yasuo Arai[2]
[1]Kanazawa Inst. of Tech. Nonoichi, Japan
[2]High Energy Accelerator, Research Org., KEK, Tsukuba, Japan

17.20-17.40 10.5 - Negative Capacitance Field-Effect Transistor Based on a Two-Dimensional Ferroelectric
M. Soleimani, N. Asoudegi, P. Khakbaz, M. Pourfath
School of Electrical and Computer Engineering, University College of Engineering, University of Tehran, Tehran, Iran

Room T4 **Session 11**
Interfaces, traps and defects
Chairperson: R. Rideau, STMicroelectronics, France

16.00-16.20 11.1 - Progress in dislocation stress field model and its appications
Uihui Kwon[1], Jeong-Guk Min[1], Seon-Young Lee[1], Alexander Schmidt[1], Dae Sin Kim[1], Yasuyuki Kayama[2], Yutaka Nishizawa[2], Kiyoshi Ishikawa[2]
[1]Semiconductor R&D Center, Samsung Electronics Corp. Ltd., Hwasung-si, Gyeonggi-do, Korea
[2]Device Solution Center, Samsung R&D Institute Japan, Tshurumi-ku, Yokohama, Japan

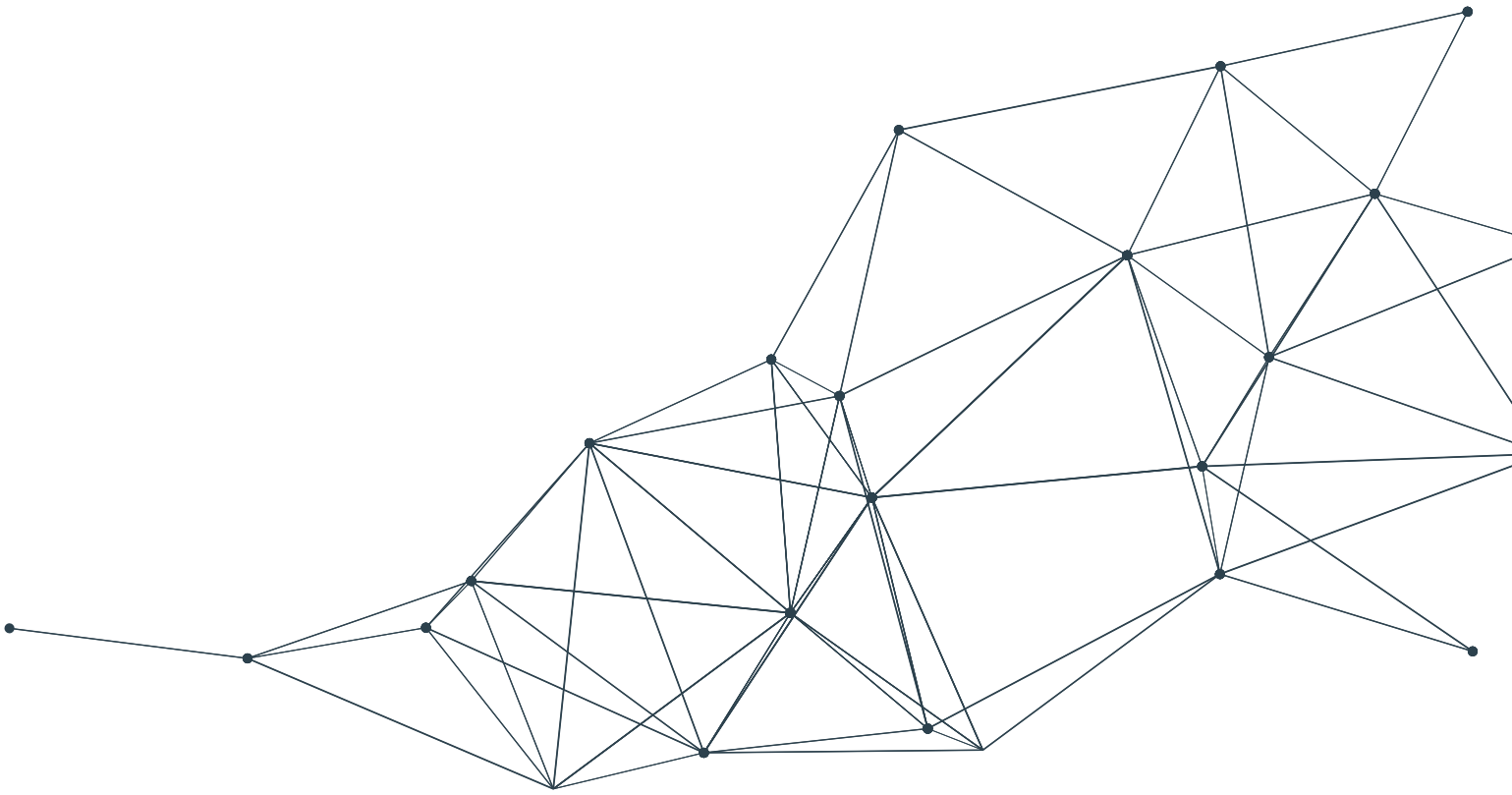
16.20-16.40 11.2 - Effect of Trap on Carrier Transport in InAs FET with Al^2O^3 Oxide: DFT-based NEGF simulations
Mincheol Shin, Yucheol Cho, Seonghyeok Jeon
School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea

16.40-17.00 11.3 - Trap Dynamics based 3D Kinetic Monte Carlo Simulation for Reliability Evaluation of UTBB MOSFETs
Wangyong Chen, Linlin Cai, Xiaoyan Liu, Gang Du
Institute of Microelectronics, Peking University, Beijing, China

17.00-17.20 11.4 - Polarization Effect Induced by Discrete Impurity at Semiconductor/Oxide Interface in Si-FinFET
Katsuhisa Yoshida, Kohei Tsukahara, Nobuyuki Sano
Institute of Applied Physics, University of Tsukuba, Ibaraki, Japan

17.20-17.40 11.5 - Relationship between capacitance and conductance in MOS capacitors
E. Caruso[1], J. Lin[1], S. Monaghan[1], K. Cherkaoui[1], L. Floyd[1], F. Gity[1], P. Palestri[2], D. Esseni[2], L. Selmi[3], P. K. Hurley[1]
[1]Tyndall National Institute, University College Cork, Ireland
[2]DPIA, University of Udine, Udine, Italy
[3]DIEF, University of Modena and Reggio Emilia, Modena, Italy

19.30-22.30 **Gala Dinner** at Palazzo Kechler



Friday September 6

09.10-10.00 **Plenary invited**
Room T9 Compact Modeling Perspective – Bridge to Industrial Applications
Mitiko Miura-Mattausch
Hiroshima University, Higashi-Hiroshima, Japan

10.00-10.20 **Coffee break**

Room T9 **Session 12**
Process modelling
Chairperson: J.Lorenz, Fraunhofer Institute for Integrated Systems and Device Technology IISB, Germany

10.20-10.50 Invited presentation
Interaction of oxygen and dopants in oxygen-inserted silicon
Daniel Connelly, Nyles W. Cody, Marek Hytha, Robert Stephenson, Hideki Takeuchi, Keith Doran Weeks, Robert Mears Atomera

10.50-11.10 12.1 - Modeling and Simulation of Atomic Layer Deposition
Lado Filipovic
Institute for Microelectronics, Technische Universität Wien, Vienna, Austria

11.10-11.30 12.2 - Novel Numerical Dissipation Scheme for Level-Set Based Anisotropic Etching Simulations
Alexander Toifl[1], Michael Quell[1], Andreas Hössinger[2], Artem Babayan[2], Siegfried Selberherr[3], Josef Weinbub[1]
[1]Christian Doppler Laboratory for High Performance TCAD, Institute for Microelectronics, TU Wien, Austria
[2]Silvaco Europe Ltd. Cambridge, United Kingdom
[3]Institute for Microelectronics, TU Wien, Austria

11.30-11.50 12.3 - Numerical simulations of nanosecond laser annealing of Si nanoparticles for plasmonic structures
A-S. Royet[1], S. Kerdilès[1], P. Acosta Alba[1], C. Bonafos[2], V. Paillard[2], F.Cristiano[3], B. Curvers[4], K. Huet[4]
[1]CEA-LETI, MINATEC Campus, Université Grenoble Alpes, Grenoble, France
[2]CEMES-CNRS, Université de Toulouse, Toulouse, France
[3]LAAS, CNRS, Université de Toulouse, Toulouse, France
[4]LASSE, SCREEN SPE, Gennevilliers, France

11.50-12.10 12.4 - Parallelized Level-Set Velocity Extension Algorithm for Nanopatterning Applications
Michael Quell[1], Alexander Toifl[1], Andreas Hössinger[2], Siegfried Selberherr[3], Josef Weinbub[1]
[1]Christian Doppler Laboratory for High Performance TCAD, Institute for Microelectronics, TU Wien, Austria
[2]Silvaco Europe Ltd. Cambridge, United Kingdom
[3]Institute for Microelectronics, TU Wien, Austria

12.10-12.30 12.5 - Process Simulation in the Browser: Porting ViennaTS using WebAssembly
Xaver Klemenschits, Paul Manstetten, Lado Filipovic, Siegfried Selberherr
Institute for Microelectronics, TU Wien, Wien, Austria

Room T4 **Session 13**
Sensors and optoelectronic devices
Chairperson: C. Jungemann, University of Aachen, Germany

10.30-10.50 13.1 - A model of the interface charge and chemical noise due to surface reactions in Ion Sensitive FETs
Leandro Julian Mele[1], Pierpaolo Palestri[1], Luca Selmi[2]
[1]DPIA, University of Udine, Udine, Italy.
[2]DIEF, University of Modena and Reggio Emilia, Modena, Italy

10.50-11.10 13.2 - Investigation and Modelling of Single-Molecule Organic Transistors
Fabrizio Torricelli[1], Eleonora Macchia[2 3], Paolo Romele[1], Kyriaki Manoli[2], Cinzia Di Franco[4], Zsolt M. Kovacs-Vajna[1], Gerardo Palazzo[2 5 6], Gaetano Scamarcio[4 5], Luisa Torsi[2 3 6]
[1]Department of Information Engineering, University of Brescia, Brescia, Italy
[2]Dipartimento di Chimica, Università degli Studi di Bari “Aldo Moro”, Bari, Italy
[3]The Faculty of Science and Engineering, Åbo Akademi University, Turku, Finland
[4]CNR, Istituto di Fotonica e Nanotecnologie, Sede di Bari, Bari, Italy
[5]Dipartimento InterAteneo di Fisica “M. Merlin”, Università degli Studi di Bari “Aldo Moro”, Bari, Italy
[6]CSGI (Centre for Colloid and Surface Science), Bari, Italy

11.10-11.30 13.3 - Advances in 3D CMOS image sensors optical modeling: combining realistic morphologies with FDTD
Benjamin Vianne[1], Axel Crocherie[1], Sofiane Guissi[2], Daniel Sieger[3], Stéphane Calderon[3], D. Rideau[1], Hélène Wehbe-Alause[1]
[1]STMicroelectronics, Crolles, France
[2]Lam Research, Meylan, France
[3]Coventor a Lam Research Company, Villebon sur Yvette, France

11.30-11.50 13.4 - Simulation of quantum dot based single-photon sources using the Schrödinger-Poisson-Drift-Diffusion-Lindblad system
Markus Kantner, Thomas Koprucki, Hans-Jürgen Wünsche and Uwe Bandelow
Weierstrass Institute for Applied Analysis and Stochastics Mohrenstr. 39, Berlin, Germany

11.50-12.10 13.5 - A generalized multi-particle drift-diffusion simulator for optoelectronic devices
Daniele Rossi, Matthias Auf der Maur, Aldo Di Carlo
Dept. of Electronic Engineering, Universit`a degli Studi di Roma “Tor Vergata”, Rome, Italy

12.10-12.30 13.6 - An Efficient Method for Modeling Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors
Federico Pace[1 2], Olivier Marcelot[1], Philippe Martin-Gonthier[1], Olivier Saint-Pé[2], Michel Breart de Boisanger[2], Rose-Marie Sauvage[3], Pierre Magnan[1]
[1]ISAE-SUPAERO, Université de Toulouse, Toulouse, France
[2]Airbus Defence & Space, ZI du Palais, Toulouse, France
[3]Direction Générale de l’Armement, Paris, France

12.30-13.30 **Lunch**

CONFERENCE PROCEEDINGS
The Congress bags contain a USB pen drive and a booklet with the final conference papers.

CERTIFICATE OF ATTENDANCE
The certificate of attendance will be available on line for all registered participants.

REGISTRATION DESK
Congress Secretariat Opening Hours:
Wednesday, 04th September 2019:
from 08.00 to 18.00
Thursday, 05th September 2019:
from 08.00 to 18.00
Friday, 06th September 2019:
from 08.00 to 13.30

LIABILITY
The organizer cannot accept liability for any personal accidents, loss of belongings or damage to private property of participants and accompanying persons that may occur during the congress.

LUNCH/COFFEE BREAK
Coffee break and lunch are included in the registration fee and they will take place on Wednesday, Thursday and Friday at the Catering Area. Please present your badge at the catering stations.

SOCIAL EVENTS / WELCOME COCKTAIL
04th September 2019
The cocktail reception will be held at Palazzo di Toppo Wassermann at 18.00

GALA DINNER
05th September 2019
The conference dinner will be held at Palazzo Kechler at 19.30
Dress Code: Informal.

TAXI
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STAFF
Should you have any questions, congress staff will be pleased to help you. Please contact the Registration Desk.

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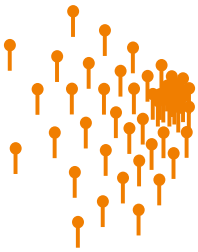

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