SISPAD 2017 Program

September 7

9:00–9:20 Opening and Welcome Remarks
K. Sonoda (*Renesas Electronics, Japan*)

Session 1: Plenary

Chairpersons: Akira Hiroki (*Kyoto Inst. Tech., Japan*)
Leonard F. Register (*Univ. Texas, Austin, USA*)

1-1 9:20–10:05 **[invited talk]**

"Physical Issues in Device Modeling: Length-Scale, Disorder, and Phase Interference"
N. Sano (*Tsukuba Univ., Japan*)

1-2 10:05–10:50 **[invited talk]**

"Stacked Nanowires/Nanosheets GAA MOSFET from Technology to Design Enablement"
J.-C. Barbé[1,2], S. Barraud[1,2], O. Rozeau[1,2], S. Martinie[1,2], J. Lacord[1,2], P. Blaise[1,2], Z. Zeng[1,3,4], L. Bourdet[1,3,4], F. Triozon[1,2], and Y. Niquet[1,2] ([1]*Univ. Grenoble Alpes, France*, [2]*CEA-Leti, France*, [3]*CEA-INAC, France*, [4]*MEM, France*)

1-3 10:50–11:35 **[invited talk]**

"Energy Efficient Computing with Hyperdimensional Vector Space Models"
S. Salahuddin (*Univ. California Berkeley, USA*)

11:35–13:00 *Lunch*

Session 2: Band Structure I : Interface Traps, Doping and Phonons

Chairpersons: Denis Rideau (*STMicroelectronics, France*)
Takahiro Iizuka (*Hiroshima Univ., Japan*)

2-1 13:00–13:30 **[invited talk]**

"New Approaches for First-Principles Modelling of Inelastic Transport in Nanoscale Semiconductor Devices with Thousands of Atoms"
T. Gunst[1], M. Brandbyge[1], M. Palsgaard[1,2], T. Markussen[2], and K. Stokbro[2] ([1]*TU Denmark, Denmark*, [2]*QuantumWise A/S, Denmark*)

2-2 13:30–13:50

"DFT-based Analysis of the Origin of Traps at the InAs/Si (111) Interface"
S. Sant, M. Luisier, and A. Schenk (*ETH Zurich, Switzerland*)

2-3 13:50–14:10

"Simulation of doping effect for HfO_2-based RRAM based on first-principles calculations"
W. Wei[1], X. Chuai[1], N. Lu[1], Y. Wang[1], L. Li[1], C. Ye[2], and M. Liu[1] ([1]*Chinese Academy of Sciences, China*, [2]*Hubei Univ., China*)

2-4 14:10–14:30

"Phonon confinement effects in diffusive quantum transport simulations with the effective mass approximation and k.p method"
A. Ziegler and M. Luisier (*ETH Zurich, Switzerland*)

2-5 14:30–14:50

"Self-consistent 30-band simulation approach for (non-)uniformly strained confined heterostructure tunnel field-effect transistors"
D. Verreck[1], A. Verhulst[1], M. Van de Put[2], B. Sorée[1,3,4], W. Magnus[1,4], N. Collaert[1], A. Mocuta[1], and G. Groeseneken[1,3] ([1]*imec, Belgium,* [2]*Univ. Texas at Dallas, USA,* [3]*KU Leuven, Belgium,* [4]*Univ. Antwerpen, Belgium*)

Session 3: Computational Methodology

Chairpersons: Yiming Li (*National Chiao Tung Univ., Taiwan*)
Shohiro Sho (*Osaka Univ., Japan*)

3-1 13:30–13:50

"A hybrid MPI/OpenMP parallelization method for a quantum drift diffusion model"
S. Sho and S. Odanaka (*Osaka Univ., Japan*)

3-2 13:50–14:10

"An Accurate Metric to Control Time Step of Transient Device Simulation by Matrix Exponential Method"
S. Kumashiro, T. Kamei, A. Hiroki, and K. Kobayashi (*Kyoto Inst. of Technology, Japan*)

3-3 14:10–14:30

"Finite-difference methodology for full-chip electromigration analysis applied to 3D IC test structure: simulation vs. experiment"
J.-H. Choy[1], A. Kteyan[2], V. Sukharev[1], S. Chatterjee[3], F. Najm[3], and S. Moreau[4] ([1]*Mentor Graphics Corp., USA,* [2]*Mentor Graphics Corp., Armenia,* [3]*Univ. of Toronto, Canada,* [4]*CEA-Leti, France*)

3-4 14:30–14:50

"Application of Multiobjective Optimizer Algorithms to the Design of SiC devices"
M. Bellini and L. Knoll (*ABB Corporate Research, Switzerland*)

14:50–15:10 *Coffee Break*

Session 4: Nanowire

Chairpersons: Yoshinari Kamakura (*Osaka Univ., Japan*)
Victor Moroz (*Synopsys, USA*)

4-1 15:10–15:40 **[invited talk]**

"Unique Challenges in Compact Modeling"
S. Mudanai and A.S. Roy (*Intel, USA*)

4-2 15:40–16:00

"Nanoscale-nMOSFET Junction Design: Quantum Transport Approach"
M.A. Pourghaderi[1], C. Park[1], J. Kim[1], C. Jeong[1], W.-Y. Chung[1], K.-H. Lee[1], H.-H. Park[2], A.-T. Pham[2], S. Jin[2], and W. Choi[2] ([1]*Samsung Electronics Institute, Korea,* [2]*Samsung Semiconductor Inc., USA*)

4-3 16:00–16:20

"Does a Nanowire Transistor Follow the Golden Ratio?: A 2D Poisson Schrödinger / 3D Monte Carlo Simulation Study"
T. Al-Ameri[1], V. Georgiev[1], F. Adamu-Lema[1], and A. Asenov[1,2] ([1]*Univ. Glasgow, UK,* [2]*Synopsys, UK*)

4-4 16:20–16:40

"Timing and Power Fluctuations on Gate-All-Around Nanowire CMOS Circuit Induced by Various Sources of Random Discrete Dopants"
W.-L. Sung, P.-J. Chao, and Y. Li (*National Chiao Tung Univ., Taiwan*)

4-5 16:40–17:00

"Small-Signal Analysis of Silicon Nanowire Transistors Based on a Poisson/Schrödinger/Boltzmann Solver"
M. Noei, D. Ruić, and C. Jungemann (*RWTH Aachen Univ., Germany*)

Session 5: Material and Geometry Impact

Chairpersons: Juergen Lorenz (*Fraunhofer Institut IISB, Germany*)
Yoshinori Oda (*Keio Univ., Japan*)

5-1 15:40–16:00

"Novel Experimentally Calibrated Multiphase TCAD Model for Cobalt Germanide Growth"
M. Rabie[1], I. Aden-Ali[2], and Y. Haddara[2] ([1]*GLOBALFOUNDRIES, USA*, [2]*McMaster Univ., USA*)

5-2 16:00–16:20

"Accelerated Direct Flux Calculations Using an Adaptively Refined Icosahedron"
P. Manstetten[1], A. Hössinger[2], J. Weinbub[1], and S. Selberherr[1] ([1]*TU Wien, Austria*, [2]*Silvaco Europe Ltd., UK*)

5-3 16:20–16:40

"3D Simulation of Silicon-Based Single-Electron Transistors"
F. Klüpfel and P. Pichler (*Fraunhofer IISB, Germany*)

5-4 16:40–17:00

"Simulation of micro-mirrors for optical MEMS"
M. Zanuccoli[1], C. Fiegna[1], I. Semenikhin[2], E. Cianci[3], C. Wiemer[3], A. Lamperti[3], G. Tallarida[3], L. Lamagna[4], S. Losa[4], S. Rossini[4], and F. Vercesi[4] ([1]*Univ. Bologna, Italy*, [2]*Russian Academy of Science, Russia*, [3]*CNR IMM, Italy*, [4]*STMicroelectronics, Italy*)

18:00–20:00 *Reception*

September 8

Session 6: Reliability

Chairpersons: Dondee Navarro (*Hiroshima Univ., Japan*)
Akira Hiroki (*Kyoto Inst. Tech., Japan*)

6-1 9:00–9:30 **[invited talk]**

"Modeling of BTI-Aging Vt Stability for Advanced Planar and FinFET SRAM Reliability"
Y.-H. Lee, J.H. Lee, Y.S. Tsai, S. Mukhopadhyay, and Y.F. Wang (*TSMC, Taiwan*)

6-2 9:30–9:50

"Single Event Transient in bulk MOSFETs: original modelling for SPICE application"
N. Rostand[1,2], S. Martinie[2], J. Lacord[2], O. Rozeau[2], J.-C. Barbé[2], and G. Hubert[1] ([1]*ONERA, France*, [2]*CEA-Leti, France*)

6-3 9:50–10:10

"A Unified Aging Model with Recovery Effect and Its Impact on Circuit Design"
W.-K. Lee, K. Huang, L.-C. Hsu, C. Huang, J. Liang, J. Chen, C. Hsiao, K.-W. Su, C.-K. Lin, and M.-C. Jeng (*TSMC, Taiwan*)

10:10–10:30 *Coffee Break*

6-4 10:30–10:50

"Circuit-Aging Modeling Based on Dynamic MOSFET Degradation and Its Verification"
N. Rohbani[1,2], H. Miyamoto[2], H. Kikuchihara[2], D. Navarro[2], T.K. Maiti[2], C. Ma[2], M. Miura-Mattausch[2], S.-G. Miremadi[1], and H.J. Mattausch[2] ([1]*Sharif Univ. of Technology, Iran,* [2]*Hiroshima Univ., Japan*)

6-5 10:50–11:10

"FinFET NBTI Degradation Reduction and Recovery Enhancement through Hydrogen Incorporation and Self-Heating"
H.Y. Wong[1], S. Mishra[2], S. Mahapatra[2], S. Motzny[1], and V. Moroz[1] ([1]*Synopsys Inc., USA,* [2]*IIT Bombay, India*)

6-6 11:10–11:30

"Modeling of Flicker Noise in Quasi-ballistic FETs"
A. Dasgupta and Y.S. Chauhan (*IIT Kanpur, India*)

Session 7: Power Devices

Chairpersons: Katsumi Eikyu (*Renesas, Japan*)
Nobuhiko Nakano (*Keio Univ., Japan*)

7-1 9:30–9:50

"Dependence of Avalanche Breakdown on Surface & Buffer Traps in AlGaN/GaN HEMTs"
V. Joshi[1,2], B. Shankar[2], S.P. Tiwari[1], and M. Shrivastava[2] ([1]*IIT Jodhpur, India,* [2]*Indian Institute of Science Bangalore, India*)

7-2 9:50–10:10

"TCAD for gate stack optimization in pGaN Gate HEMT devices"
M.-A. Jaud, Y. Baines, M. Charles, E. Morvan, P. Scheiblin, A. Torrès, M. Plissonier, and J.-C. Barbé (*CEA-Leti, France*)

10:10–10:30 *Coffee Break*

7-3 10:30–10:50

"Modified Angelov model for an exploratory GaN-HEMT technology with short, few-fingered gates"
S. Emekar, J. Jha, S. Mukherjee, M. Meer, K. Takhar, D. Saha, and S. Ganguly (*IIT Bombay, India*)

7-4 10:50–11:10

"Local Stress Engineering for the Optimization of p-GaN Gate HEMTs Power Devices"
T. Cosnier[1], L. Lucci[1], A. Torrès[1], and M. Pala[2] ([1]*CEA-Leti, France,* [2]*C2N, CNRS, Univ. Paris-Saclay, France*)

7-5 11:10–11:30

"Modeling of Electrical Activation Ratios of Phosphorus and Nitrogen Doped Silicon Carbide"
V. Šimonka[1], A. Hössinger[2], J. Weinbub[1], and S. Selberherr[1] ([1]*TU Wien, Austria,* [2]*Silvaco Europe Ltd., UK*)

11:30–13:00 *Lunch*

Session 8: Non-volatile Memory

Chairpersons: Kazuya Matsuzawa (*Toshiba, Japan*)
Uihui Kwon (*Samsung, Korea*)

8-1 13:00–13:30 **[invited talk]**

"Soft Error Rate Estimation with TCAD and Machine Learning"
M. Hashimoto, W. Liao, and S. Hirokawa (*Osaka Univ., Japan*)

8-2 13:30–13:50

"Physical Modeling of the Electroforming Process in Resistive-Switching Devices"
A. Marchewka[1], R. Waser[1,2], and S. Menzel[2] ([1]*RWTH Aachen Univ., Germany,* [2]*Peter Gruenberg Institut, Forschungszentrum Juelich, Germany*)

8-3 13:50–14:10

"Efficient Models for Designing GB-Level 3-D 1S1R Horizontal-Stacked-RRAM and Vertical-RRAM Arrays"
L. Song and J. Zhang (*Tsinghua Univ., China*)

8-4 14:10–14:30

"A Computationally Efficient Compact Model for Leakage in Cross-point Array"
A. Aziz[1], N. Jao[1], S. Datta[2], V. Narayanan[1], and S. Gupta[1] ([1]*The Pennsylvania State Univ., USA,* [2]*Univ. of Notre Dame, USA*)

8-5 14:30–14:50

"A SPICE-compatible model of SG-MONOS for 28nm flash macro design considering the parasitic resistance caused by trapped charges"
R. Koh[1], M. Miyamori[1], K. Tsuneno[1], T. Muta[1], and Y. Kawashima[2] ([1]*Renesas System Design, Japan,* [2]*Renesas Electronics, Japan*)

Session 9: Interconnects

Chairpersons: Takashi Kurusu (*Toshiba, Japan*)
Hiroyuki Takashino (*Sony Semiconductor Manufacturing, Japan*)

9-1 13:30–13:50

"Back-end Limitations in Advanced Nodes and Alternatives"
A. Ayres[1], O. Rozeau[2], B. Borot[1], L. Fesquet[3], G. Cibrario[2], and M. Vinet[2] ([1]*STMicroelectronics, France,* [2]*CEA-Leti, France,* [3]*Univ. Grenoble Alpes, France*)

9-2 13:50–14:10

"Atoms-to-Circuits Simulation Investigation of CNT Interconnects for Next Generation CMOS Technology"
J. Lee[1], J. Liang[2], S. Amoroso[3], T. Sadi[1,4], L. Wang[3], P. Asenov[3], A. Pender[3], D. Reid[3], V. Georgiev[1], C. Millar[3], A. Todri-Sanial[2], and A. Asenov[1] ([1]*Univ. Glasgow, UK,* [2]*Univ. of Montpellier, France,* [3]*Synopsys Inc., UK,* [4]*Aalto Univ., Finland*)

9-3 14:10–14:30

"The Impact of Vacancy Defects on CNT Interconnects: From Statistical Atomistic Study to Circuit Simulations"
J. Lee[1], S. Berrada[1], J. Liang[2], T. Sadi[1,3], V. Georgiev[1], A. Todri-Sanial[2], D. Kalita[4,5], R. Ramos[6,5], H. Okuno[4,5], J. Dijon[6,5], and A. Asenov[1] ([1]*Univ. Glasgow, UK,* [2]*Univ. of Montpellier, France,* [3]*Aalto Univ., Finland,* [4]*CEA-INAC, France,* [5]*Univ. Grenoble Alpes, France,* [6]*CEA-LITEN, France*)

9-4 14:30–14:50

"Modeling Electromigration in Nanoscaled Copper Interconnects"
L. Filipovic[1], R.L. deOrio[2], W.H. Zisser[1], and S. Selberherr[1] ([1]*TU Wien, Austria,* [2]*UNICAMP, Brazil*)

Poster Session [September 8, 15:00–17:00]

Chairperson: Nobuhiko Nakano (*Keio Univ., Japan*)

P1 "Comparison of Basis Sets for Efficient Ab-initio Modeling of Semiconductors," D. Vaidya, S. Lodha, and S. Ganguly (*IIT Bombay, India*)

P2 "On Electronic Structure and Geometry of MoX_2 (X = S, Se, Te) and Black Phosphorus by ab initio Simulation with Various van der Waals Corrections," Y.-C. Tsai and Y. Li (*National Chiao Tung Univ., Taiwan*)

P3 "Atomistic Simulation of Band-to-Band Tunneling in SiGe: Influence of Alloy Scattering," H.-H. Park[1], S. Jin[1], W. Choi[1], M. Luisier[2], J. Kim[3], and K.-H. Lee[3] ([1]*Samsung Semiconductor Inc., USA,* [2]*ETH Zurich, Switzerland,* [3]*Samsung Electronics Corp., Korea*)

P4 "Transport Simulations with Density-Matrix-Based Real-Time Time-Dependant Density Functional Theory," S. Andermatt[1], M.H. Bani-Hashemian[1], S. Brück[1], J. VandeVondele[2], and M. Luisier[1] ([1]*ETH Zurich, Switzerland,* [2]*Swiss National Supercomputing Centre, Switzerland*)

P5 "Analysis of Screening Effects in Multiple-Gate and Gate-All-Around Si NW array FETs," G. Darbandy[1], S. Mothes[1], M. Schröter[1,2], and M. Claus[1] ([1]*TU Dresden, Germany,* [2]*Univ. California at San Diego, USA*)

P6 "Analysis of Neutron-induced Soft Error Rates on 28nm FD-SOI and 22nm FinFET Latches by the PHITS-TCAD Simulation System," J. Furuta, S. Umehara, and K. Kobayashi (*Kyoto Inst. of Technology, Japan*)

P7 "On the Design Challenges of Drain Extended FinFETs for Advance SoC Integration," B.S. Kumar, M. Paul, and M. Shrivastava (*Indian Institute of Science Bangalore, India*)

P8 "Evaluation of reconfigurable tunnel FETs for low power and high performance operation," S. Blawid[1], D.L.M. deAndrade[1], F. Wolf[2], S. Mothes[2], and M. Claus[2] ([1]*Univ. de Brasilia, Brazil,* [2]*TU Dresden, Germany*)

P9 "PNIN-GAA-Tunnel FET with Palladium Catalytic Metal Gate as a Highly Sensitive Hydrogen Gas Sensor," J. Madan, S. Shekhar, and R. Chaujar (*Delhi Technological Univ., India*)

P10 "Computational Modeling of Hybrid Graphene/Quantum Dot Photodetector," H. Imran, S. Iqbal, A. Farooq, and N.Z. Butt (*Lahore Univ. of Management Sciences, Pakistan*)

P11 "Design of High Performance Graphene/Silicon Photodetectors," S. Iqbal, H. Imran, U.B. Qasim, and N.Z. Butt (*Lahore Univ. of Management Sciences, Pakistan*)

P12 "Effect of strain on electron mobility in graphene," H. Hirai, M. Ogawa, and S. Souma (*Kobe Univ., Japan*)

P13 "Time dependent quantum dynamical study of laser induced current switching in graphene," S. Souma, T. Akiyama, K. Sasaoka, and M. Ogawa (*Kobe Univ., Japan*)

P14 "Performance Evaluation of Ferroelectric MOSFETs based on Gibbs Free Energy," X. Zhang and G. Liang (*National Univ. of Singapore, Singapore*)

P15 "Angular dependence of nonparabolicity factor of energy band structures," N. Fujimoto, A. Hiroki, and S. Hiratoko (*Kyoto Inst. of Technology, Japan*)

P16 "Analytical model of Energy Level Alignment at Metal-Organic Interface facilitating Hole Injection," X. Shi, G. Xu, X. Duan, N. Lu, L. Li, and M. Liu (*Chinese Academy of Sciences, China*)

P17 "Effects of Surface Orientation and Body Thickness on the Performance of III-V Ultrathin-Body nMOSFETs," T.-H. Yu (*DesignFet Company, Taiwan*)

P18 "Simulation of GaN MOS capacitance with frequency dispersion and hsyteresis," K. Fukuda[1], J. Hattori[1], H. Asai[1], M. Shimizu[1], and T. Hashizume[2] ([1]*AIST, Japan,* [2]*Hokkaido Univ., Japan*)

P19 "Feature Scale Simulation for Advanced Processing," P. Moroz[1] and D. Moroz[2] ([1]*TEL Technology Center, USA,* [2]*Harvard Univ., USA*)

P20 "Modeling of the effective field dependent mobility for TCAD simulation of DRAM cell transistors considering the random discrete dopants," D. Kim, H. Yu, S. Rhee, and Y.J. Park (*Seoul National Univ., Korea*)

P21 "Towards Physics-Based DTCO for Performance of Advanced Technology Nodes," Z. Stanojević, O. Baumgartner, M. Karner, C. Kernstock, H.-W. Karner, H. Demel, G. Strof, and F. Mitterbauer (*Global TCAD Solutions GmbH, Austria*)

P22 "TCAD Simulation Methodology for Full 3-D Electro-Physical and Advanced Thermal Analysis of Power Modules," P. Príbytný, A. Chvála, J. Marek, and D. Donoval (*STU in Bratislava, Slovakia*)

P23 "Electrothermal Analysis of Power Multifinger HEMTs Supported by Advanced 3-D Device Simulation," A. Chvála[1], J. Marek[1], P. Príbytný[1], A. Šatka[1], S. Stoffels[2], N. Posthuma[2], S. Decoutere[2], and D. Donoval[1] ([1]*STU in Bratislava, Slovakia,* [2]*IMEC, Belgium*)

P24 "Simulation of Turn-off Oscillation Suppression in Silicon Insulated Gate Bipolar Transistors," S. Machida and K. Nomura (*Toyota Central R&D Labs. Inc., Japan*)

P25 "Compact Modeling of Normaly-on MOSFET Applicable for Any Technology Generations," T. Iizuka, Y. Hirano, T. Umeda, H. Kikuchihara, H. Miyamoto, D. Navarro, M. Miura-Mattausch, and H.J. Mattausch (*Hiroshima Univ., Japan*)

P26 "Accurate BEOL Statistical Modeling Methodology with Circuit-Level Multi-Layer Process Variations," Y.-S. Song[1,2], C.-Y. Chu[1], J. Jeon[1], U.-H. Kwon[1], K.-H. Lee[1], and S. Kim[2] ([1]*Samsung Electronics Corp., Korea,* [2]*Sung Kyun Kwan Univ., Korea*)

P27 "Implementing Physical Unclonable Functions Using PCM Arrays," E. Piccinini[1], R. Brunetti[2], and M. Rudan[1] ([1]*Univ. of Bologna, Italy,* [2]*Univ. of Modena and Reggio Emilia, Italy*)

September 9

Session 10: Transport

Chairpersons: Hideki Minari (*Sony Semiconductor Solutions, Japan*)
Satofumi Souma (*Kobe Univ., Japan*)

10-1 9:00–9:30 **[invited talk]**

"The Impact of Hetero-junction and Oxide-interface Traps on the Performance of InAs/Si and InAs/GaAsSb Nanowire Tunnel FETs"
A. Schenk[1], S. Sant[1], K. Moselund[2], H. Riel[2], E. Memisevic[3], and L.-E. Wernersson[3] ([1]*ETH Zurich, Switzerland,* [2]*IBM Research-Zurich, Switzerland,* [3]*Lund Univ., Sweden*)

10-2 9:30–9:50

"Analysis of quasi-ballistic hole transport capability of Ge and Si nanowire pMOSFETs by a quantum-corrected Boltzmann transport equation"
H. Tanaka, J. Suda, and T. Kimoto (*Kyoto Univ., Japan*)

10-3 9:50–10:10

"Multi-Subband Ensemble Monte Carlo Study of Tunneling Leakage Mechanisms"
C. Medina-Bailon[1], T. Sadi[2], C. Sampedro[1], J.L. Padilla[1], A. Godoy[1], L. Donetti[1], V. Georgiev[2], F. Gamiz[1], and A. Asenov[2] ([1]*Univ. Granada, Spain,* [2]*Univ. Glasgow, UK*)

10:10–10:30 *Coffee Break*

10-4 10:30–10:50

"Advanced Quasi-Self-consistent Monte Carlo Simulations on High-Frequency Performance of Nanometer-scale GaN HEMTs Considering Local Phonon Distribution"
N. Ito, R. Sawabe, and Y. Awano (*Keio Univ., Japan*)

10-5 10:50–11:10

"Analysis of Anisotropic Ionization Coefficient in Bulk 4H-SiC with Full-Band Monte Carlo Simulation"
R. Fujita[1], K. Konaga[1], Y. Ueoka[1], T. Kotani[2], Y. Kamakura[1], and N. Mori[1] ([1]*Osaka Univ., Japan,* [2]*Tottori Univ., Japan*)

10-6 11:10–11:30

"Hot Carrier Study Including e-e Scattering Based on a Backward Monte Carlo Method"
M. Kampl and H. Kosina (*TU Wien, Austria*)

Session 11: High Speed Switching Devices and Noise

Chairpersons: Shigeyasu Uno (*Ritsumeikan Univ., Japan*)
Yoshinori Oda (*Keio Univ., Japan*)

11-1 9:30–9:50

"Advanced non-quasi-static (NQS) compact model for characterization of non-resonant plasmonic terahertz detector"
S.H. Ahn, M.W. Ryu, E. Jang, H.J. Jeon, and K.R. Kim (*Ulsan National Institute of Science and Technology, Korea*)

11-2 9:50–10:10

"Simulation of THz Emission by Plasma Waves in GaAs Devices Based on the Boltzmann Transport Equation"
Z. Kargar, D. Ruić, T. Linn, and C. Jungemann (*RWTH Aachen Univ., Germany*)

10:10–10:30 *Coffee Break*

11-3 10:30–10:50

"High Speed Low Power All Spin Logic Devices Assisted by Negative Capacitance Amplified Voltage Controled Magnetic Anisotropy Effect"
T. Gao[1,2], L. Zeng[1,2], D. Zhang[1,2], X. Qin[1,2], M. Long[1,2], Y. Zhang[1,2], and W. Zhao[1,2] ([1]*Beihang Univ., China,* [2]*Fert Beijing Inst., China*)

11-4 10:50–11:10

"Sub 0.5 V bias voltage operation of a triple-topgate graphene tunnel field effect transistor"
S. Suzuki, A.M.M. Hamman, M.E. Schmidt, M. Muruganathan, and H. Mizuta (*JAIST, Japan*)

11-5 11:10–11:30

"RandomTelegraph Noise analysis in Redox-based Resistive Switching Devices Using KMC Simulations"
E. Abbaspour[1], S. Menzel[2], and C. Jungemann[1] ([1]*RWTH Aachen Univ., Germany,* [2]*Peter Gruenberg Institut, Forschungszentrum Juelich, Germany*)

11:30–13:00 *Lunch*

Session 12: Future Devices

Chairpersons: Hirokazu Hayashi (*Lapis Semiconductor, Japan*)
Andreas Schenk (*ETH Zurich, Switzerland*)

12-1 13:00–13:20

"Simulation Based DC and Dynamic Behaviour Characterization of Z2FET"
F. Adamu-Lema[1], M. Duan[1], C. Navaro[2], V. Georgiev[1], B. Cheng[3], X. Wang[3], C. Millar[3], F. Gamiz[2], and A. Asenov[1] ([1]*Univ. Glasgow, UK,* [2]*Univ. Granada, Spain,* [3]*Synopsys Inc., UK*)

12-2 13:20–13:40

"Z2FET DC hysteresis: deep understanding and preliminary model"
J. Lacord[1], S. Martinie[1], M. Parihar[2], K. Lee[2], M. Bawedin[2], S. Cristoloveanu[2], Y. Taur[3], and J.-C. Barbé[1] ([1]*CEA-Leti, France,* [2]*Univ. Grenoble Alpes, IMEP-LAHC, France,* [3]*Univ. of California, San Diego, USA*)

12-3 13:40–14:00

"2D-TCAD Simulation on Retention Time of Z2FET for DRAM Application"
M. Duan[1], F. Adamu-Lema[1], B. Cheng[2], C. Navarro[3], X. Wang[2], V. Georgiev[1], F. Gamiz[3], C. Millar[2], and A. Asenov[1,4] ([1]*Univ. Glasgow, UK,* [2]*Synopsys Inc., UK,* [3]*Univ. Granada, Spain,* [4]*Synopsys, UK*)

12-4 14:00–14:20

"Optimization guidelines of A2RAM cell performance through TCAD simulations"
F. TchemeWakam[1,2], J. Lacord[1], M. Bawedin[2], S. Martinie[1], S. Cristoloveanu[2], and J.-C. Barbé[1] ([1]*CEA-Leti, France,* [2]*Univ. Grenoble Alpes, IMEP-LAHC, France*)

12-5 14:20–14:40

"A Physical Model of the Abnormal Behavior of Hydrogen-Terminated Diamond MESFET"
H.Y. Wong, N. Braga, and R.V. Mickevicius (*Synopsys Inc., USA*)

Session 13: Band Structure II : 2D and Nano Systems

Chairpersons: Chioko Kaneta (*Fujitsu Laboratories Ltd., Japan*)
Satofumi Souma (*Kobe Univ., Japan*)

13-1 13:00–13:20

"Dielectric Properties of Mono- and Bilayers Determined from First Principles"
A. Laturia and W. Vandenberghe (*Univ. Texas at Dallas, USA*)

13-2 13:20–13:40

"Performance investigation of uniaxially strained phosphorene n-MOSFETs"
S. Jung, J. Seo, S. Heo, and M. Shin (*School of Electrical Engineering, KAIST, Korea*)

13-3 13:40–14:00

"Modeling of Black Phosphorus vertical TFETs without chemical doping for drain"
S.-C. Lu[1,2], Y. Kim[1,3], M. Mohamed[4], M. Gilbert[1,3], and U. Ravaioli[1,2] ([1]*Univ. of Illinois at Urbana-Champaign, USA*, [2]*Beckman Inst., USA*, [3]*Micro and Nanotechnology Lab., USA*, [4]*Lincoln Lab., MIT, USA*)

13-4 14:00–14:20

"First-principle calculations of the non-equilibrium polarization in ultra-small Si nanowire devices"
G. Mil'nikov[1], J. Iwata[2], N. Mori[1], and A. Oshiyama[2] ([1]*Osaka Univ., Japan*, [2]*The Univ. of Tokyo, Japan*)

14:20–15:00 *Coffee Break*

Session 14: SOI, Double-Gate and FinFET

Chairpersons: Koichi Fukuda (*AIST, Japan*)
Akira Hiroki (*Kyoto Inst. Tech., Japan*)

14-1 15:00–15:20

"Modeling of crystal impurities in III-V ultra-thin body field-effect transistors within the empirical tight-binding framework"
M. Rau[1], H.-H. Park[2], and M. Luisier[1] ([1]*ETH Zurich, Switzerland*, [2]*Samsung Semiconductor Inc., USA*)

14-2 15:20–15:40

"TCAD Analysis of SiGe Channel FinFET Devices"
J. Cho, F. Geelhaar, L. Vanamurthy, R. Sporer, and F. Benistant (*GLOBALFOUNDRIES, USA*)

14-3 15:40–16:00

"Fast evaluation of Continuous-RX impact on performance for Strained FDSOI"
J. Lacord, M.-A. Jaud, T. Poiroux, and J.-C. Barbé (*CEA-Leti, France*)

14-4 16:00–16:20

"Versatile Technology Modeling for 22FDX Platform Development"
E.M. Bazizi[1], A. Zaka[1], T. Herrmann[1], I. Cortes[1], L. Jiang[1], M.H.J. Goh[1], S. DebRoy[1], E. Nowak[1], G. Kluth[1], P. Javorka[1], L. Pirro[2], J. Mazurier[2], D. Harame[1], T. Kammler[1], J. Hoentschel[1], J. Schaeffer[1], F. Benistant[1], and B. Rice[1] ([1]*GLOBALFOUNDRIES, Germany*, [2]*CEA-Leti, France*)

14-5 16:20–16:40

"Optimization of RF-22nm FDSOI Figures of Merit with 3D TCAD simulation"
P. Scheiblin[1], A. Zaka[2], E.M. Bazizi[2], T. Herrmann[2], J. Lacord[1], L. Lucci[1], S. Morvan[1,2], L. Pirro[1,2], Y. Andee[1,2], J. Mazurier[1,2], D. Harame[2], and J.-C. Barbé[1] ([1]*CEA-Leti, France*, [2]*GLOBALFOUNDRIES, Germany*)

16:40–16:50 Closing
K. Sonoda (*Renesas Electronics, Japan*)

Conference Schedule

Date	Room	Morning	Afternoon 1	Afternoon 2	Evening
Thursday Sept. 7	A	9:00–11:35 1. Plenary (3 Invited)	13:00–14:50 2. Band Structure I (1 Invited + 4 Regulars)	15:10–17:00 4. Nanowire (1 Invited + 4 Regulars)	18:00–20:00 Reception
	B		13:30–14:50 3. Computational Methodology (4 Regulars)	15:40–17:00 5. Material and Geometry Impact (4 Regulars)	
Friday Sept. 8	A	9:00–11:30 6. Reliability (1 Invited + 5 Regulars)	13:00–14:50 8. Non-volatile Memory (1 Invited + 4 Regulars)		
	B	9:30–11:30 7. Power Devices (5 Regulars)	13:30–14:50 9. Interconnects (4 Regulars)		
	C			15:00–17:00 Poster Session (27 Posters)	
Saturday Sept. 9	A	9:00–11:30 10. Transport (1 Invited + 5 Regulars)	13:00–14:40 12. Future Devices (5 Regulars)	15:10–16:50 14. SOI, Double-Gate and FinFET (5 Regulars)	
	B	9:30–11:30 11. High Speed Switching Devices and Noise (5 Regulars)	13:30–14:20 13. Band Structure II (4 Regulars)		

[*as of August 29, 2017*]

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