

Compact Modeling

-Enabling Better Insight of Device Features-

09:15 - 09:20: Opening

09:20 - 10:00: **J. Takeya** (University of Tokyo, Japan): invited

Physics of Charge Transport in Organic Field-Effect Transistors

10:00 - 10:40: **C. Jungemann** (RWTH Aachen University, Germany): invited

Validity of Macroscopic Noise Models in the Case of High-Frequency Bipolar Transistors

10:40 - 11:00: **break**

11:00 - 11:40: **N. Goldsman** (University of Maryland, USA): invited

Key Issues in the Modeling of SiC Electronic Devices

11:40 - 12:10: **C. Ma** (Hiroshima University, Japan): invited

Universal Model of the Negative Bias Temperature Instability (NBTI) Effect for Circuit Aging Simulation

12:10 - 12:30: poster presentations

-**P. X. Tran** (International University, Vietnam)

A Comprehensive Model for the Changing I-V Characteristics of Graphene Transistors

-**M. Ghittorelli, F. Torricelli, Z. M. Kovacs-Vajna, and L. Calalongo** (University of Brescia, Italy)

Accurate Modeling of Amorphous Indium-Gallium-Zinc-Oxide TFTs Deposited on Plastic Foil

-**S. Sato, Y. Omura, and A. Mallik** (Kansai University, Japan)

Proposal of Simple Channel-Length-Dependent Current Model for Subthreshold Region of Nano-Wire Tunnel FET

-**H. Miyamoto, H. Zenitani, H. Kikuchiara, H. J. Mattausch, M. Miura-Mattausch, and T. Nakagawa** (HU & AIST, Japan)

Consistent Compact Modeling of MOSFETs from Bulk to Double-Gate Structures

12:30 - 13:50: **lunch**

13:50 - 14:30: **D. Warning** (Creative Chips GmbH, Germany): invited

NGSPICE – an Open Platform for Modeling and Simulation

14:30 - 15:00: **A. Schaldenbrand** (Cadence Design Systems, Japan): invited

Benefits of Verilog-A for Behavioral Modeling and Compact Modeling

15:00 - 15:30: **P. Lee** (Micron Memory Japan, Inc.): invited

Compact Model Coalition: World-Wide Model Standardization for an Expanding Industry

15:30 - 15:40: **break**

15:40 - 16:00: **F. Torricelli, M. Ghittorelli, M. Rapisarda, L. Mariucci, S. Jacob, R. Coppard, E. Cantatore, Z. M. Kovacs-Vajna, and L. Colalongo** (University of Brescia, Italy)

Analytical Drain Current Model of Both p- and n-Channel OTFTs for Circuit Simulation

16:00 - 16:20: **T. Nakagawa, T. Sekigawa, M. Hioki, Y. Ogasahara, H. Koike, H. Zenitani, H. Miyamoto, H. Kikuchiara, H. J. Mattausch, M. Miura-Mattausch, H. Oda, and N. Sugii** (AIST, HU, LEAP, Japan)

Parameter-Extraction Strategy of Ultra-Thin Silicon and BOX Layer MOSFETs for Low Voltage Applications

16:20 - 16:40: **T. Mizoguchi, T. Naito, Y. Kawaguchi, and W. Saito** (Toshiba, Japan)

Compact Modeling of GaN-MISFET for Power Applications

16:40 - 17:00: **T. Yamamoto and H. Kato** (Denso, Japan)

Analysis and Modeling of Injection Enhanced Insulated Gate Bipolar Transistor

17:00: Closing