Technical Programme

University of Glasgow

GSS

Programme At A Glance

Monday 2nd September

08:30	Registration (available all day)	
09:00	CEDA Workshop *(Regent)*	MORDRED Workshop *(Clyde)*
16:40	Workshops End	
18:00	Civic Reception (see page 22)	

Tuesday 3rd September

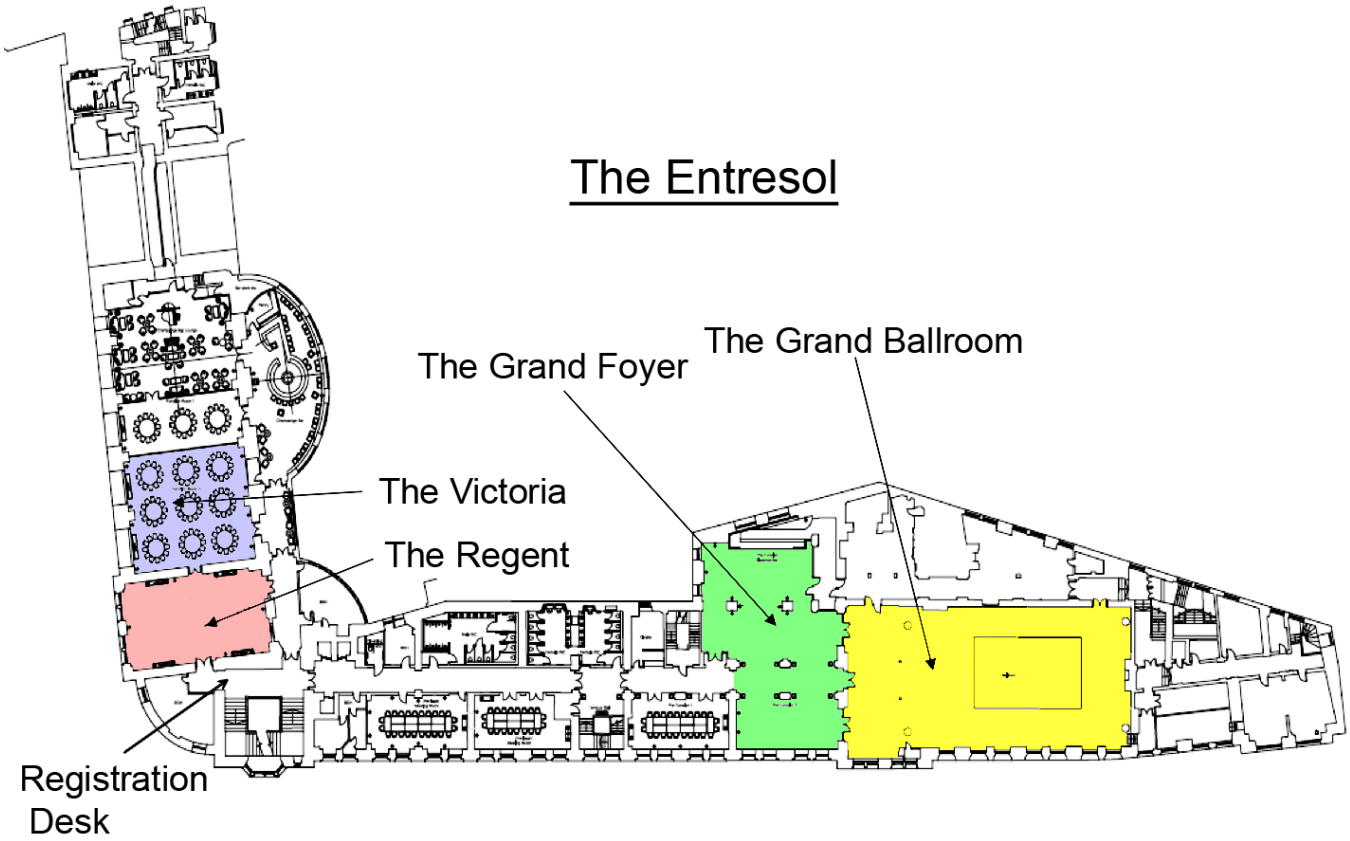
08:00	Registration/Coffee	
08:45	Welcome (***Ballroom)*** **-** *Asen Asenov (University of Glasgow/GSS)*	
08:50	Keynote *(Ballroom)* **-** ***Gary Patton (IBM)***	
09:40	Process Simulation 1 *(Ballroom)*	Reliability 1 *(Regent)*
10:30	Coffee Break (*Ballroom Foyer)*	
10:50	Process Simulation 2 *(Ballroom)*	Reliability 2 *(Regent)*
12:10	Lunch *(Victoria)*	
13:30	Plenary *(Ballroom)* **-** ***Chenming Hu (University of California, Berkley)***	
14:10	Compact Models (*Ballroom*)	Interconnects & Contacts *(Regent)*
15:10	Coffee Break (*Ballroom Foyer)*	
15:30	Nanowires *(Ballroom)*	Technology *(Regent)*
17:10	Technical Programme Ends	
18:30	Whisky Tasting *(The Lighthouse)*	

Wednesday 4th September

09:00	Plenary *(Ballroom)* **-** ***Cory Weber (Intel)***	
09:40	Variability *(Ballroom)*	Novel Materials+Devices 1 *(Regent)*
10:30	Coffee Break (*Ballroom Foyer)*	
10:50	FinFETs *(Ballroom)*	Novel Materials+Devices 2 *(Regent)*
12:10	Lunch *(Victoria)*	
13:30	Plenary *(Ballroom)* **-** ***Jeff Wu (TSMC)***	
14:10	TCAD *(Ballroom)*	Monte Carlo Transport *(Regent)*
15:10	Poster Session *(Ballroom Foyer)*	
17:00	Technical Programme Ends	
18:30	Conference Dinner *(Oran Mor)*	

Thursday 5th September

09:00	Plenary *(Ballroom) – Jo Finders (ASML)*	
09:40	Memories 1 *(Ballroom)*	Circuits *(Regent)*
10:30	Coffee Break *(Ballroom Foyer)*	
10:50	Memories 2 *(Ballroom)*	Transport *(Regent)*
12:10	Lunch *(Victoria)*	
13:30	Plenary *(Ballroom) – Gerhard Klimeck (Purdue University)*	
14:10	III-V Devices *(Ballroom)*	Models & Methodologies 1 (*Regent)*
15:10	Coffee Break *(Ballroom Foyer)*	
15:30	Quantum Transport *(Ballroom)*	Models & Methodologies 2 *(Regent)*
17:10	Closing Remarks *(Ballroom)*	
17:20	Drinks Reception *(Ballroom Foyer)*	



Workshops

Monday 2nd September

Two companion workshops will run concurrently prior to the start of the conference on Monday 2nd September.

Workshop 1: Modelling of Reliability and Degradation of Nanoelectronic Devices

Chairman: Adam Foster (Aalto University)

Overview: As a warm-up to the SISPAD meeting, a short satellite workshop based around European 7th framework collaborative project, MORDRED will be held. It focuses on developing multiscale modelling technology, supported by comprehensive experimental characterization techniques, to study the degradation and reliability of next generation Complimentary-Metal-Oxide-Semiconductor (CMOS) devices. The project will provide technologists, device engineers and designers in the nano CMOS industry with tools, reference databases and examples of how to produce future devices that are economical, efficient, and meet high performance, reliability and degradation standards.

In this satellite workshop, the highlight contributions of the MORDRED project will be discussed alongside presentations outlining the key issues in the field from leading experts.

Full Details: http://sispad2013.org/MORDRED_workshop.php

Workshop 2: T2E-CAD: Linking Technology and Electronic System CAD Chairman

Chairman: Sani Nassif (IBM)

Overview: This workshop is organised by the IEEE Council on Electronic Design Automation (CEDA), with several leading experts in the TCAD field presenting both the methodology and case studies.

Full Details: http://sispad2013.org/CEDA_workshop.php

Tuesday 3rd September

08:00	**Registration/Coffee**		
08:45	**Welcome *(Ballroom)* -** *Asen Asenov (University of Glasgow/GSS)*		
08:50	**Keynote *(Ballroom)* - *Gary Patton (IBM)***		
	Session 2: **Process Simulation 1 *(Ballroom)*** *Session Chairs: Gary Patton (IBM) & Jo Finders (ASML)*		**Session 1:** **Reliability 1 (*Regent)*** *Session Chairs: Tibor Grasser (TU Wien) & Anthony Oates (TSMC)*
09:40			
S2-1	**(Extended) A new kinetic lattice Monte Carlo modeling framework for the source-drain selective epitaxial growth process** *Renyu Chen and Woosung Choi (Device Laboratory, Samsung Semiconductor Inc.) and Alexander Schmidt, Keun-Ho Lee, and Youngkwan Park (Semiconductor R&D center, Samsung Electronics)*	S1-1	**(Extended) A Detailed Evaluation of Model Defects as Candidates for the Bias Temperature Instability** *Franz Schanovsky, Oskar Baumgartner, Wolfgang Goes, and Tibor Grasser (TU Wien)*
10:10			
S2-2	**A Numerical Model using Phase Field Method for Stress Induced Voiding in a Metal Line during Thermal Bake** *Yong-Seog Oh (Synopsys, Inc.), Sora Park, Jongsung Jeon, Dong-Cheon Baek, Jin-Seok Kim, and Windu Sari (Samsung Electronics Co.), and Hyerim Lee and Ibrahim Avci (Synopsys Inc.)*	S1-2	**3D TCAD Statistical Analysis of Transient Charging in BTI Degradation of Nanoscale MOSFETs** *Salvatore Maria Amoroso and Louis Gerrer (Device Modelling Group, University of Glasgow), and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)*
10:30	**Coffee Break *(Ballroom Foyer)***		

	Session 4: **Process Simulation 2 *(Ballroom)*** *Session Chairs: Gary Patton (IBM) & Jo Finders (ASML)*		Session 3: **Reliability 2 *(Regent)*** *Session Chairs: Tibor Grasser (TU Wien) & Anthony Oates (TSMC)*
10:50			
S4-1	**Dopant dynamics and defects evolution in implanted silicon under laser irradiations: a coupled continuum and Kinetic Monte Carlo approach** *G. Fisicaro (CNR IMM), L. Pelaz, M. Aboy, and P. Lopez (Department of Electronics, University of Valladolid), M. Italia (CNR IMM), K. Huet (Excico), F. Cristiano (LAAS CNRS), Z. Essa (LAAS CNRS/STMicroelectronics), Q. Yang and E. Bedel-Pereira (LAAS CNRS), M. Hackenberg (Fraunhofer Institute for Integrated Systems and Device Technology), P. Pichler (Fraunhofer Institute for Integrated Systems and Device Technology/ University of Erlangen-Nuremberg), M. Quillec and N. Taleb (Probion), and A. La Magna (CNR IMM)*	S3-1	**Direct Tunneling and Gate Current Fluctuations** *Oskar Baumgartner, Markus Bina, Wolfgang Goes, Franz Schanovsky, Hans Kosina, and Tibor Grasser (Institute for Microelectronics, TU Wien) and Maria Toledano-Luque and Ben Kaczer (imec)*
11:10			
S4-2	**Donor deactivation at high doping limit: donor pair and impurity band model** *Chihak Ahn and Woosung Choi (Samsung Semiconductor Inc.), Hiroyuki Kubotera and Yasuyuki Kayama (Samsung R&D Institute of Japan), Alexander Schmidt, Keunho Lee, and Youngkwan Park (Samsung Semiconductor R&D center), and Nick E. B. Cowern (Newcastle University)*	S3-2	**Assessment of the Statistical Impedance Field Method for the Analysis of the RTN Amplitude in Nanoscale MOS Devices** *Giulio Torrente and Niccolo' Castellani (Politecnico di Milano), Andrea Ghetti (Micron Technology), Christian Monzio Compagnoni, Andrea Leonardo Lacaita, and Alessandro Sottocornola Spinelli (Politecnico di Milano), and Augusto Benvenuti (Micron Technology)*

11:30

S4-3 **Atomistic Study of Sulfur Diffusion and S2 Formation in Silicon during Low-temperature Rapid Thermal Annealing**
Takahisa Kanemura (Center for Semiconductor Research and Development, Semiconductor & Storage Products Company, Toshiba Corporation), Koichi Kato (Advanced LSI Technology Laboratory, Corporate Research and Development Center, Toshiba Corporation), and Hiroyoshi Tanimoto, Nobutoshi Aoki, and Yoshiaki Toyoshima (Center for Semiconductor Research and Development, Semiconductor & Storage Products Company, Toshiba Corporation)

S3-3 **Quantum Insights in Gate Oxide Charge-Trapping Dynamics in Nanoscale MOSFETs**
Salvatore Maria Amoroso (Device Modelling Group, University of Glasgow), Jean Michel Sellier (IICT, Bulgarian Academy of Sciences), Mihail Nedjalkov (Institute for Microelectronics, TU Wien), Louis Gerrer (Device Modelling Group, University of Glasgow), Ivan Dimov (IICT, Bulgarian Academy of Sciences), Siegfried Selberherr (Institute for Microelectronics, TU Wien), and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)

11:50

S4-4 **Epitaxial Volmer-Weber Growth Modelling**
Raffaele A. Coppeta (Institut für Mikroelektronik an der TU Wien), Hajdin Ceric (Christian Doppler Laboratory for Reliability Issues in Microelectronics at the Institute for Microelectronics), Tibor Grasser (Institut für Mikroelektronik an der TU Wien), and Bala Karunamurthy (KAI Kompetenzzentrum Automobil- und Industrieelektronik GmbH)

S3-4 **A Physics-Based Statistical Model for Reliability of STT-MRAM Considering Oxide Variability**
Chih-Hsiang Ho, Soo Youn Kim, Yusung Kim, Dongsoo Lee, Georgios D. Panagopoulos, and Kaushik Roy (Purdue University)

12:10 **Lunch *(Victoria)***

13:30	**Plenary *(Ballroom) - Chenming Hu (University of California, Berkeley)***		
	Session 5: **Compact Models *(Ballroom)*** *Session Chair: Larry Nagel (Omega Enterprises)*		**Session 6:** **Interconnects+Contacts*(Regent)*** *Session Chairs: Victor Moroz (Synopsys) & Jurgen Lorenz (Fraunhofer IISB)*
14:10			
S5-1	**Recent Enhancements in BSIM6 Bulk MOSFET Model** *H.Agarwal (IIT Kanpur), S. Venugopalany (University of California Berkeley), M.-A. Chalkiadakia (Ecole Polytechnique Federale de Lausanne), N. Paydavosi and J. P. Duarte (University of California Berkeley), S. Agnihotri, C. Yadav, P. Kushwaha and Y. S. Chauhan (IIT Kanpur), C. Enz (Ecole Polytechnique Federale de Lausanne), A. Niknejd, and C. Hu (University of California Berkeley)*	S6-1	**Stress Estimation in Open Tungsten TSV** *Anderson Singulani, Hajdin Ceric, and Siegfried Selberherr (TU Wien)*
14:30			
S5-2	**An Accurate Compact Modelling Approach for Statistical Ageing and Reliability** *Jie Ding (Device Modelling Group, University of Glasgow), Dave Reid and Campbell Millar (GSS), and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)*	S6-2	**Limits of specific contact resistivity to Si, Ge, and III-V semiconductors using interfacial layers** *Gautam Shine and Krishna C. Saraswat (Stanford University)*
14:50			
S5-3	**Compact Modeling for Application-Specific High-Sigma Worst Case** *Hsuan-Han Wang, Yi-Ling Chen, Chang-Chieh Yang, Chung-Kai Lin, and Min-Chie Jeng (Taiwan Semiconductor Manufacturing Company)*	S6-3	**Impact of Intermetallic Compound on Solder Bump Electromigration Reliability** *Hajdin Ceric, Anderson Pires Singulani, Roberto Lacerda de Orio, and Siegfried Selberherr (Institute for Microelectronics, TU Wien)*
15:10	**Coffee Break *(Victoria)***		

	Session 7: Nanowires *(Ballroom)* *Session Chair: Massimo Rudan (ARCES - University of Bologna)*		Session 8: Technology *(Regent)* *Session Chairs: Victor Moroz (Synopsys) & Jurgen Lorenz (Fraunhofer IISB)*
15:30			
S7-1	**A Tight-binding Study of Channel Modulation in Atomic-scale Si:P Nanowires** *Hoon Ryu (Korea Institute of Science and Technology Information), Sunhee Lee (Samsung Advanced Institute of Technology), Bent Weber, Suddhasatta Mahapatra, and Michelle Y. Simmons (Centre for Quantum Computer Technology, University of New South Wales), Lloyd C. L. Hollenberg (Centre for Quantum Computer Technology, University of Melbourne), and Gerhard Klimeck (Network for Computational Nanotechnology, Purdue University)*	S8-1	**22nm Technology Yield Optimization Using Multivariate 3D Virtual Fabrication** *Benjamin R. Cipriany (IBM), David M. Fried (Coventor), Basanth Jagannathan and Gregory Costrini (IBM), Ken Greiner (Coventor), Ahmed Nayaz Noemaun, Katsunori Onishi, Shreesh Narasimha, Bidan Zhang, Christopher D. Sheraw, and Jason E. Meiring (IBM), Daniel Faken (Coventor), Mahender Kumar, Karen A. Nummy, and Ning Zhan (IBM), Stephen R. Breit (Coventor), and James P. Norum, Stephen S. Furkay, Rajeev Malik, Paul D. Agnello, and Haraprasad Nanjundappa (IBM)*
15:50			
S7-2	**Full band calculations of low-field mobility in p-type Silicon nanowire MOSFETs** *Neophytos Neophytou, Zlatan Stanojevic, and Hans Kosina (Technical University of Vienna)*	S8-2	**Mechanism of Super Steep Subthreshold Slope Characteristics with Body-Tied SOI MOSFET** *Takayuki Mori and Jiro Ida (Kanazawa Institute of Technology)*
16:10			
S7-3	**Electrostatics and Ballistic Transport Studies in Junctionless Nanowire Transistors** *Tsung-Hsing Yu, Ethan Hsu, C-W Liu, J.P. Colinge, Y-M Sheu, Jeff Wu, and C.H. Diaz (TSMC)*	S8-3	**Double Patterning: Simulating a Variability Challenge for Advanced Transistors** *Peter Evanschitzky, Alex Burenkov, and Jürgen Lorenz (Fraunhofer IISB)*
16:30			
S7-4	**Strain effects on transport properties of Si nanowire devices** *Viet-Hung Nguyen (L_Sim, SP2M, UMR-E CEA/UJF-Grenoble 1), François Triozon (CEA, LETI, MINATEC), and Yann-Michel Niquet (L_Sim, SP2M, UMR-E CEA/UJF-Grenoble 1)*	S8-4	**Fin Bending due to Stress and its Simulation** *Alp H. Gencer, Dimitrios Tsamados, and Victor Moroz (Synopsys)*

16:50

S7-5 **Impact of Band Non-parabolicity on the Onset Voltage in a Cylindrical Tunnel Field-effect Transistor**
H. Carrillo-Nuñez (IM2NP), Wim Magnus (Departement Fysica, Universiteit Antwerpen/imec), William G. Vandenberghe (University of Texas at Dallas, Department of Materials Science and Engineering) Bart Sorée (Departement Fysica, Universiteit Antwerpen/imec) and François M. Peeters (Departement Fysica, Universiteit Antwerpen)

S8-5 **Understanding Workfunction Tuning in HKMG by Lanthanum Diffusion Combining Simulations and Measurements**
Alessio Spessot and Christian Caillat (Micron Technology), Romain Ritzenthaler and Tom Schram (imec), and Pierre Fazan (Micron Technology Belgium)

17:10 **Technical Programme Ends**

18:30 **Whisky Tasting *(The Lighthouse)* (see Page 23)**

Wednesday 4th September

09:00	**Plenary *(Ballroom)* - *Cory Weber (Intel)***		
	Session 9: **Variability *(Ballroom)*** *Session Chair: C.-K. Lin (TSMC)*		**Session 10:** **Novel Materials & Devices 1 *(Regent)*** *Session Chair: Neil Goldsman (University of Maryland)*
09:40			
S9-1	**(Extended) Effects of Phonon Scattering on Discrete-Impurity-Induced Current Fluctuation in Silicon Nanowire Transistors** *Nobuya Mori (Osaka University), Masashi Uematsu (Keio University), Gennady Mil'nikov and Hideki Minari (Osaka University), and Kohei M. Itoh (Keio University)*	S10-1	**(Extended) Fast Simulation of Spin Transfer Torque Devices in a General Purpose TCAD Device Simulator** *Frederik Ole Heinz (Synopsys Switzerland) and Lee Smith (Synopsys Inc.)*
10:10			
S9-2	**Simulation of Correlated Line-Edge Roughness in Multi-Gate Devices** *Xiaobo Jiang, Runsheng Wang, Jiang Chen, and Ru Huang (Peking University)*	S10-2	**Change of the Electronic Conductivity of Graphene Nanoribbons and Carbon Nanotubes Caused by a Local Deformation** *Masato Ohnishi, Ken Suzuki, and Hideo Miura (Tohoku University)*
10:30	**Coffee Break *(Ballroom Foyer)***		
	Session 11: **FinFETs *(Ballroom)*** *Session Chair: Cory Weber (Intel)*		**Session 12:** **Novel Materials & Devices 2 *(Regent)*** *Session Chair: Chandra Mouli (Micron)*
10:50			
S11-1	**Unified FinFET Compact Model: Modelling Trapezoidal Triple-Gate FinFETs** *Juan Pablo Duarte, Navid Paydavosi, Sriramkumar Venugopalan, Angada Sachid, and Chenming Hu (University of California, Berkeley)*	S12-1	**Ab-initio and Continuum Simulation of High-Field Chemistry of Diphenylgermane and Diphenylsilane for Scanning Probe Direct Write** *Wenjun Jiang (Department of Physics, University of Washington), Marco Rolandi (Department of Materials Science & Engineering, University of Washington), Haoyu Lai and Scott T. Dunham (Department of Electrical Engineering, University of Washington)*

11:10

S11-2 **Unified Compact Modelling Strategies for Process and Statistical Variability in 14-nm node DG FinFETs**
X. Wang and B. Cheng (Device Modelling Group, University of Glasgow), A. R. Brown, C. Millar, C. Alexander, and D. Reid (GSS), J. B. Kuang and S. Nassif (IBM Austin Research Lab) and A. Asenov (Device Modelling Group, University of Glasgow/GSS)

S12-2 **A Modified Top-of-the-Barrier Solver for Graphene and Its Application to Predict RF Linearity**
Ahsan U. Alam, Kyle D. Holland, and Sabbir Ahmed (Department of Electrical and Computer Engineering, University of Albertaa), Diego Kienle (Theoretische Physik I, Universitat Bayreuth), and Mani Vaidyanathan (Department of Electrical and Computer Engineering, University of Alberta)

11:30

S11-3 **Performance Advantage and Energy Saving of Triangular-Shaped FinFETs**
Kehuey Wu (National Nano Device Laboratories) and Wei-Wen Ding and Meng-Hsueh Chiang (Department of Electronic Engineering, National Ilan University)

S12-3 **Impact of near-contact barriers on the subthreshold slope of short-channel CNTFETs**
Martin Claus (Technische Universität Dresden, Germany), Stefan Blawid (Universidade de Brasília, Brazil), and Michael Schröter (UC San Diego, USA)

11:50

S11-4 **A Comparative Study of Fin-Last and Fin-First SOI FinFETs**
Darsen Lu, Josephine Chang, Michael A. Guillorn, Chung-Hsun Lin, Jeffrey Johnson, Phil Oldiges, Ken Rim, Mukesh Khare, and Wilfried Haensch (IBM Research)

S12-4 **Performance Analysis and Comparison of Two 1T/1MTJ-based Logic Gates**
Hiwa Mahmoudi, Thomas Windbacher, Viktor Sverdlov, and Siegfried Selberherr (Institute for Microelectronics, TU Wien)

12:10 **Lunch *(Victoria)***

13:30	**Plenary *(Ballroom)* - *Jeff Wu (TSMC)***		
	Session 14: **TCAD *(Ballroom)*** *Session Chair: Jeff Wu (TSMC)*		**Session 13:** **Monte Carlo Transport *(Regent)*** *Session Chair: Christoph Jungemann (ITHE RWTH Aachen University)*
14:10			
S14-1	**Density Gradient calibration for 2D quantum confinement : Tri-Gate SOI transistor application** *Nicolas Pons, François Triozon, and Marie-Anne Jaud (CEA-LETI), Remi Coquand (CEA-LETI/STMicroelectronics), Sébastien Martinie (CEA-LETI), Yann-Michel Niquet and V.-H Nguyen (CEA-INAC), and Anouar Idrissi-El Oudrhiri and Sylvain Barraud (CEA-LETI)*	S13-1	**Efficient 3D Monte Carlo Simulation of Orientation and Stress Effects in FinFETs** *Fabian Bufler and Frederik Ole Heinz (Synopsys Schweiz GmbH) and Lee Smith (Synopsys Inc.)*
14:30			
S14-2	**Impact of Back-end-of-line on Thermal Impedance in SiGe HBTs** *Amit Kumar Sahoo, Sébastien Fregonese, Mario Weiß, C. Maneux, Nathalie Malbert, and Thomas Zimmer (Laboratoire IMS, CNRS - UMR 5218, Université de Bordeaux 1)*	S13-2	**Toward computationally efficient Multi-Subband Monte Carlo Simulations of Nanoscale MOSFETs** *Patrik Osgnach, Alberto Revelant, Daniel Lizzit, Pierpaolo Palestri, David Esseni, and Luca Selmi (DIEGM, University of Udine)*
14:50			
S14-3	**Quantum Confinement Point of View for Mobility and Stress Responses on (100) and (110) Single-Gate and Double-Gate nMOSFETs** *Anson C-C Wang, Edward Chen, Tzer-Min Shen, Jeff Wu, and Carlos H. Diaz (TSMC)*	S13-3	**Density Functional and Monte Carlo-based Electron Transport Simulation in 4H-SiC(0001)/SiO2 DMOSFET Transition Region** *S. Salemi, D. P. Ettisserry, A. Akturk, and N. Goldsman (University of Maryland) and A. Lelis (US Army Research Lab)*
15:10	**Poster Session (see page 14)**		
17:00	**Technical Programme Ends**		
18:30	**Conference Dinner *(Oran Mor)* (see page 24)**		

Thursday 5th September

09:00	**Plenary *(Ballroom) – Jo Finders (ASML)***		
	Session 16: **Memories 1 *(Ballroom)*** *Session Chair: Pierpaolo Palestri (DIEGM, University of Udine)*		**Session 15:** **Circuits *(Regent)*** *Session Chair: Saurabh Sinha (ARM)*
09:40			
S16-1	**(Extended) Simulation of CBRAM devices with the level set method** *P.Dorion (CEA-LETI & UPMC Univ J.-L Lions Laboratory), O.Cueto, M.Reyboz, E.Vianello, and J.C. Barbé (CEA-LETI), A.Grigoriu (Univ. Paris Diderot,), and Y.Maday (UPMC Univ J.-L Lions Laboratory)*	S15-1	**(Extended) Evaluating the Accuracy of SRAM Margin Simulation Through Large Scale Monte-Carlo Simulations with Accurate Compact Models** *Plamen Asenov and David New (ARM), Dave Reid and Campbell Millar (GSS), and Scott Roy (University of Glasgow) and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)*
10:10			
S16-2	**A Unified Model of Metallic Filament Growth Dynamics for Conductive-Bridge Random Access Memory** *Shengjun Qin, Jinyu Zhang, and Zhiping Yu (Institute of Microelectronics,Tsinghua University)*	S15-2	**Accelerated Variation Simulation through Parameter Reduction** *William "Paul" Griffin II and Kaushik Roy (Purdue University)*
10:30	**Coffee Break *(Ballroom Foyer)***		
	Session 18: **Memories 2 *(Ballroom)*** *Session Chair: Jeff Watt (Altera)*		**Session 17:** **Transport *(Regent)*** *Session Chair: Nobuya Mori (Osaka University)*
10:50			
S18-1	**An Analytical Model for Predicting Forming/Switching Time in Conductive-Bridge Resistive Memory (CBRAM)** *Shaoli Lv, Jun Liu and Lingling Sun (CAD Institute,Hangzhou Dianzi University) and He Wang, Jinyu Zhang, and Zhiping Yu (Institute of Microelectronics,Tsinghua University)*	S17-1	**Coupled Drift-Diffusion (DD) and Multi-Subband Boltzmann Transport Equation (MSBTE) Solver for 3D Multi-Gate Transistors** *Seonghoon Jin (Samsung Semiconductor), Sung-Min Hong (GIST), Woosung Choi (Samsung Semiconductor), and Keun-Ho Lee and Youngkwan Park (Samsung Electronics)*

11:10

S18-2 **Rigorous Simulation Study of a Novel Non-Volatile Magnetic Flip Flop**
Thomas Windbacher, Hiwa Mahmoudi, Viktor Sverdlov, and Siegfried Selberherr (Institute for Microelectronics, TU Wien)

S17-2 **Surface-Roughness-Scattering in Non-Planar Channels -- the Role of Band Anisotropy**
Zlatan Stanojevic and Hans Kosina (TU Wien, Institute for Microelectronics)

11:30

S18-3 **A hybrid spin-charge mixed-mode simulation framework for evaluating spin-transfer torque MRAM bit-cells utilizing multiferroic tunneling junctions**
Xuanyao Fong and Kaushik Roy (Purdue University)

S17-3 **A self-consistent solution of the Poisson, Schrödinger and Boltzmann equations by a full Newton-Raphson approach for nanoscale semiconductor devices**
Dino Ruic and Christoph Jungemann (ITHE RWTH Aachen University)

11:50

S18-4 **Addressing Key Challenges in 1T-DRAM: Retention Time, Scaling and Variability - Using a Novel Design with GaP Source-Drain**
Ashish Pal, Aneesh Nainani and Krishna Saraswat (Stanford University)

S17-4 **Spherical Harmonics Solver for a Coupled Hot-Electron-Hot-Phonon System**
Mindaugas Ramonas (RWTH Aachen University/Center for Physical Sciences and Technology, SPI) and Christoph Jungemann (RWTH Aachen University)

12:10 **Lunch *(Victoria)***

13:30 **Plenary *(Ballroom) – Gerhard Klimeck (Purdue University)***

Session 19:

III-V Devices *(Ballroom)*

Session Chair: Y. J. Lee (Qualcomm)

Session 20:

Models & Methodologies 1 *(Regent)*

Session Chairs: Gerhard Klimeck (Purdue University) and Asen Asenov (University of Glasgow/GSS)

14:10

S19-1 **Atomistic simulation of a III-V p-i-n junction**
Kurt Stokbro, Anders Blom, and Søren Smidstrup (QuantumWise)

S20-1 **First-principle investigation of Ti wetting layer influence on metal-graphene contact**
Xiang Ji, Yan Wang, and Zhiping Yu (Tsinghua University)

14:30

S19-2 **Comparison of Raised Source/Drain Implant-Free Quantum-Well and Tri-Gate MOSFETs using 3D Monte Carlo Simulation**
Ewan Towie and Craig Riddet (Device Modelling Group, University of Glasgow) and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)

S20-2 **Identification and Quantification of 4H-SiC (0001)/SiO2 Interface Defects by Combining Density Functional and Device Simulations**
D.P. Ettisserry, S. Salemi, N. Goldsman, S. Potbhare, and A. Akturk (Dept. of ECE, University of Maryland) and A. Lelis (U.S. Army Research Laboratory)

14:50

S19-3 **Calculation of the valence band structures in strained $In_{0.7}Ga_{0.3}As$ devices with different surface orientation**
Pengying Chang, Lang Zeng, Xiaoyan Liu, Wei Kangliang, Jieyu Qin, Kai Zhao, Gang Du, and Xing Zhang (Peking University)

S20-3 **Quantitative Full 3D Blooming Analysis on 1.4um BSI CMOS Image Sensor**
Mitsuhiro Sengoku (Technology CAD Group, Toshiba I.S. Corp.) and Hisao Yoshimura, Yuki Sugiura, Sakiko Shimizu, Ryoji Hasumi, and Makoto Monoi (Analog & Imaging IC Div. Toshiba Corp. S&S Products Company)

15:10 **Coffee Break *(Ballroom Foyer)***

Session 21:

Quantum Transport *(Ballroom)*

Session Chairs: Scott Roy (University of Glasgow) & Marc Bescond (IM2NP – CNRS)

Session 22:

Models & Methodologies 2 *(Regent)*

Session Chairs: Gerhard Klimeck (Purdue University) and Asen Asenov (University of Glasgow/GSS)

15:30

S21-1 **Two-dimensional Transient Wigner Particle Model**
Jean Michel Sellier (IICT, Bulgarian Academy of Sciences), Mihail Nedjalkov (Institute for Microelectronics, TU Wien), Ivan Dimov (IICT, Bulgarian Academy of Sciences), and Siegfried Selberherr (Institute for Microelectronics, TU Wien)

S22-1 **The Novel Stress Simulation Method for Contemporary DRAM Capacitor Arrays**
Kyu-Baik Chang, Yun Young Kim, Jiwoong Sue, Hojoon Lee, Won-Young Chung, Keun-Ho Lee, Young-Kwan Park and EunSeung Jung (Semiconductor R&D Center, Samsung Electronics), and Ilsub Chung (Sungkyunkwan University)

15:50

S21-2 **Comparison of Ballistic Transport Characteristics of Monolayer Transition Metal Dichalcogenides (TMDs) MX_2 (M = Mo, W; X = S, Se, Te) n-MOSFETs**
Jiwon Chang, Leonard F. Register, and Sanjay K. Banerjee (The University of Texas at Austin)

S22-2 **Microscopic Description of the Inter-Trap Transitions in a-Chalcogenides**
Massimo Rudan, Fabio Giovanardi, and Fabrizio Buscemi (ARCES and DEI - University of Bologna), Rossella Brunetti (FIM - University of Modena and Reggio Emilia), and Giuliano Marcolini (ARCES and DEI - University of Bologna)

16:10

S21-3 **One-shot current conserving approach of phonon scattering treatment in nano-transistors**
M. Bescond, E. Dib, C. Li, H. Mera, N. Cavassilas, F. Michelini, and M. Lannoo (IM2NP - CNRS)

S22-3 **Modeling of Reliability Issues in RF MEMS Switches**
Gabriele Schrag, Thomas Kuenzig, and Gerhard Wachutka (Munich University of Technology)

16:30

S21-4 **Interactions Between Precisely Placed Dopants and Interface Roughness in Silicon Nanowire Transistors: Full 3-D NEGF Simulation Study**
Vihar P. Georgiev and Ewan A. Towie (Device Modelling Group, University of Glasgow) and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)

S22-4 **3D-nHD: A hydrodynamic model for trap-limited conduction in a 3D network**
Andrea Cappelli (FIM Department - University of Modena and Reggio Emilia), Enrico Piccinini (ARCES - University of Bologna), Feng Xiong and Ashkan Behnam (MNTL - University of Illinois at Urbana-Champaign), Rossella Brunetti (FIM Department - University of Modena and Reggio Emilia), Eric Pop (MNTL - University of Illinois at Urbana-Champaign), and Carlo Jacoboni (FIM Department - University of Modena and Reggio Emilia)

16:50

S21-5 **Quantum Transport Simulation of Bilayer Pseudospin Field-Effect Transistor (BisFET) on Tight-binding Hartree-Fock Model**
Xuehao Mou, Leonard F. Register, and Sanjay K. Banerjee (The University of Texas at Austin, United States)

S22-5 **A Process/Device/Circuit/System Compatible Simulation Framework for Poly-Si TFT Based SRAM Design**
Chen-Wei Lin (NCTU, Taiwan), Chih-Hsiang Ho and Chao Lu (Purdue University), Mango C.-T. Chao (NCTU, Taiwan), and Kaushik Roy (Purdue University)

17:10 **Closing Remarks *(Ballroom)***

17:20 **Drinks Reception *(Ballroom Foyer)***

Poster Session – Wednesday 4th September, 15:10 – 17:00

Ballroom Foyer

P1 **3-D Simulation of Silicon Oxidation: Challenges, Progress and Results**
Damrong Guoy, Alp H. Gencer, Zhiqiang Tan, Satish Chalasani, Mark Johnson, Luis Villablanca, and Simeon Simeonov (Synopsys)

P2 **TCAD Modeling and Simulation of Non-Resonant Plasmonic THz Detector Based on Asymmetric Silicon MOSFETs**
Min Woo Ryu, Jeong Seop Lee, and Kibog Park (Ulsan National Institute Science and Technology), Wook-Ki Park and Seong-Tae Han (Korea Electrotechnology Research Institute), and Kyung Rok Kim (Ulsan National Institute Science and Technology)

P3 **Circuit-level modeling of FinFet sub-threshold slope and DIBL mismatch beyond 22nm**
Pablo Royer (Universidad Politécnica de Madrid), Paul Zuber (IMEC), and Binjie Cheng and Asen Asenov (University of Glasgow) and Marisa López-Vallejo (Universidad Politécnica de Madrid)

P4 **Modeling the Growth of Thin SnO_2 Films using Spray Pyrolysis Deposition**
Lado Filipovic and Siegfried Selberherr (Institute for Microelectronics, TU Wien), Giorgio Cataldo Mutinati, Elise Brunet, Stephan Steinhauer, and Anton Koeck (Molecular Diagnostics, Health & Environment, AIT GmbH), Jordi Teva, Jochen Kraft, Joerg Siegert, and Franz Schrank (ams AG), and Christian Gspan and Werner Grogger (Institute for Electron Microscopy and Fine Structure Research, Graz University of Technology and Centre for Electron Microscopy Graz)

P5 **Modeling Direct Band-to-Band Tunneling using QTBM**
Lidija Filipovic, Oskar Baumgartner, and Hans Kosina (TU Wien, Institute for Microelectronics)

P6 **Nonlinear PCA for Source Optimization in Optical Lithography**
Pardeep Kumar (Research Scholar) and Babji Srnivasan and Nihar R. Mohapatra (Assistant Professor)

P7 **PDK development of 10nm III-V/Ge IFQW CMOS technology including statistical variability**
Si-Yu Liao, Ewan A. Towie, Daniel Balaz, and Craig Riddet (Device Modelling Group, University of Glasgow) and Binjie Cheng and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)

P8 **Fast 3D Electro-Thermal Device/Circuit Simulation Based on Automated Interaction of SDevice and HSpice Simulators**
Aleš Chvála, Daniel Donoval, Juraj Marek, Patrik Príbytný, and Marián Molnár (Institute of Electronics and Photonics, Slovak University of Technology in Bratislava)

P9 **A new time-dependent analytic compact model for radiation-induced photocurrent in epitaxial structures**
Jason C. Verley, Eric R. Keiter, and Charles E. Hembree (Sandia National Laboratories), Carl L. Axness (Sandia National Laboratories (ret.)), and Bert Kerr (New Mexico Institute of Mining and Technology)

P10 **Influence of Temperature on the Standard Deviation of Electromigration Lifetimes**
Roberto Lacerda de Orio, Hajdin Ceric, and Siegfried Selberherr (Institute for Microelectronics, TU Wien)

P11 **Evaluation of Spin Lifetime in Strained UT2B Silicon-On-Insulator MOSFETs**
Dmitri Osintsev, Viktor Sverdlov, and Siegfried Selberherr (Institute for Microelectronics, TU Wien)

P12 **Impurity scattering in p-type silicon nanowire FET: k.p approach**
Nima Dehdashti Akhavan, Gregory Jolley, Gilberto Umana-Membreno, Jarek Antoszewski, and Lorenzo Faraone (University of Western Australia)

P13 **Electromigration Analyses of Open TSVs**
W. H. Zisser and H. Ceric (Christian Doppler Laboratory for Reliability Issues in Microelectronics at the Institute for Microelectronics) and R. L. de Orio and S. Selberherr (Institute for Microelectronics, TU Wien)

P14 **Modeling and Simulation of Dopant Segregation at NiSi/Si Interface Using Chemical Potential Approach**
Ashish Kumar and Mark E. Law (University of Florida)

P15 **TCAD study of Single Photon Avalanche Diode on 0.35µm High Voltage Technology**
Frederic Roger, Jordi Teva, Ewald Wachmann, Jong Mun Park, and Rainer Minixhofer (ams AG)

P16 **3-D Modeling of Fringing Gate Capacitance in Gate-all-Around Cylindrical Silicon Nanowire MOSFETs**
TaeYoon An and SoYoung Kim (College of Information and Communication Engineering, Sungkyunkwan University, Korea)

P17 **Simulation of Terahertz Plasmons in Graphene with Grating-Gate Structures**
A. Satou and V. Ryzhii (Tohoku University), F. T. Vasko and V. V. Mitin (University at Buffalo), and T. Otsuji (Tohoku University)

P18 **Microtexture Dependence of Stress-induced Migration of Electroplated Copper Thin Film Interconnections Used for 3D Integration**
Ken Suzuki, Osamu Asai, Ryosuke Furuya, Jaeuk Sung, Naokazu Murata, and Hideo Miura (Tohoku University)

P19 **Compact Physical Models for Gate Charge and Gate Capacitances of AlGaN/GaN HEMTs**
Fetene Mulugeta Yigletu and Benjamin Iñiguez (Dept. of Electrical Electronics and Automation Engineering, Universitat Rovira i Virgili) and Sourabh Khandelwal and Tor Fjeldly (Dept. of Electronics and Telecommunication, Norwegian University of Science and Technology)

P20 **Efficient Wigner Function Simulation for Nanowire MOSFETs and Comparison to Quantum Drift-Diffusion**
O. Badami, D.Saha, and S. Ganguly (Indian Institute of Technology, Bombay)

P21 **Improving subthreshold MSB-EMC simulations by dynamic particle weighting**
Carlos Sampedro, Francisco Gámiz, and Andrés Godoy (University of Granada), Raul Valin (University of Swansea), and Antonio Garcia-Loureiro (University of santiago de Compostela)

P22 **Bridging Design to Manufacturability by Layout Enhanced Analyses Process Simulations**
Mark Lu, Cong-Shu Zhou, Yi Tian, Chang Liu, Yuan-Wei Zheng, Guo-Zhong You, Qing Yang, Shyue-Fong Quek, Soo-Muay Goh, Hein-Mun Lam, Jian Zhang, Peter Benyon, and Christine P. Tan (GLOBALFOUNDRIES Singapore)

P23 **Compact Modeling of SOI MOSFETs with Ultra Thin Silicon and BOX Layers for Ultra Low Power Applications**
Yukiya Fukunaga, Mitiko Miura-Mattausch, Uwe Feldmann, and Hideyuki Kikuchihara (Hiroshima University), Tadashi Nakagawa (AIST), and Masataka Miyake and Hans Juergen Mattausch (Hiroshima University)

P24 **Impact of Back biasing in Ultra Short Channel UTBB SOI nMOSFETs**
Kai Zhao (Institute of Microelectronics, Peking University), Tiao Lu (School of Mathematical Sciences, LMAM and CAPT, Peking University), and Gang Du, Xiao-yan Liu, and Xing Zhang (Institute of Microelectronics, Peking University)

P25 **Simulation on Endurance Characteristic of Charge Trapping Memory**
Zhiyuan Lun, Taihuan Wang, Lang Zeng, Kai Zhao, Xiaoyan Liu, Yi Wang, Jinfeng Kang and Gang Du (Peking University)

P26 **Analysis of the Latchup Process in High-Voltage Trench-IGBT Cell Arrays**
Christopher Toechterle (Munich University of Technology), Frank Pfirsch and C. Sandow (Infineon Technologies AG), and Gerhard Wachutka (Munich University of Technology)

P27 **Globally hyperbolic moment method for solving BTE including phonon scattering**
Wenqi Yao, Ruo Li, and Tiao Lu (School of Mathematical Science, Peking University) and Xiaoyan Liu, Gang Du, and Kai Zhao (Institute of Microelectronics, Peking University)

P28 **Influence of the back-gate bias on the electron mobility of trigate MOSFETs**
Francisco G. Ruiz, Enrique G. Marín, Isabel M. Tienda-Luna, Andrés Godoy, Celso Martínez Blanque, and Francisco Gámiz (University of Granada)

P29 **Quasi Self-consistent Monte Carlo Particle Simulations of Local Heating Properties in Nano-scale Gallium Nitride FETs**
Taichi Misawa, Shusuke Oki, and Yuji Awano (Keio University)

P30 **Performance Evaluation of p-channel FinFETs using 3D Ensemble Monte Carlo Simulation**
Craig Riddet and Ewan A. Towie (Device Modelling Group, University of Glasgow) and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)

P31 **Novel Design of Multiple Negative-Differential Resistance (NDR) Device in a 32nm CMOS Technology using TCAD**
Sunhae Shin and Kyung Rok Kim (UNIST)

P32 **Analytical Modelling of Current-Voltage Characteristics of Ballistic Graphene Nanoribbon Field-Effect Transistors**
George S. Kliros (Hellenic Air-Force Academy)

P33 **Simulating Ion Transport and its Effects in Silicon Carbide Power MOSFET Gate Oxides**
Daniel B. Habersat and Aivars J. Lelis (U.S. Army Research Laboratory) and Neil Goldsman (Dept. of Electrical and Computer Engineering, University of Maryland)

P34 **Simulated effect of epitaxial growth variations on THz emission of SiGe/Ge quantum cascade structures**
Pavlo Ivanov, Alexander Valavanis, Zoran Ikonic, and Robert Kelsall (School of Electronic and Electrical Engineering, University of Leeds)

Social Events

Civic Reception

A civic reception at Glasgow City Chambers will take place on Monday 2nd September, with a welcome speech by a city dignitary.

The City Chambers building was designed by Glaswegian architect William Young and inaugurated by Queen Victoria in 1888, and has been used as the headquarters of the municipal government of Glasgow ever since.

Location: City Chambers, Glasgow, G2 1DU

Travel: Located a short walk from The Grand Central Hotel:

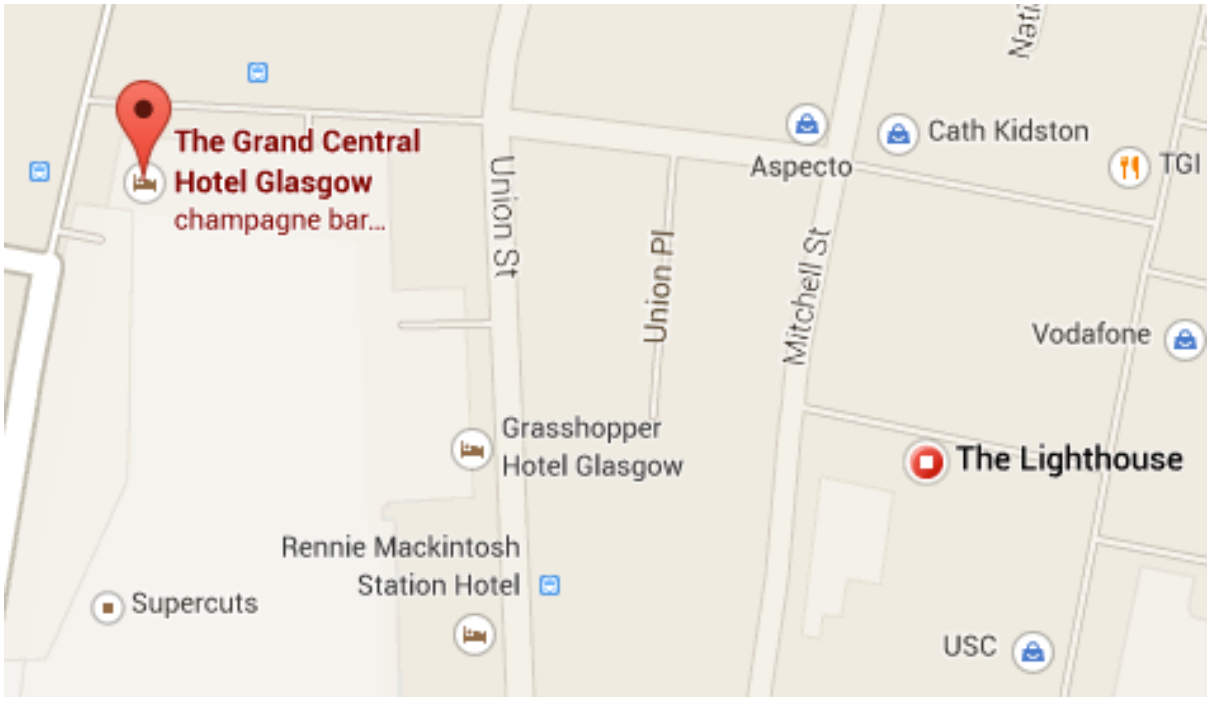
Whisky Tasting

The tutored Whisky Tasting is being carried out by The Good Spirits Co. (http://www.thegoodspiritsco.com), and you will have the chance to try 4 very special single malt whiskies. There will also be some canapés to enjoy and some unique mementos to take away with you. Additionally, there will be soft drinks available. The tasting will start at 6.30pm.

The venue is Gallery 4 in The Lighthouse (http://www.thelighthouse.co.uk) - Scotland's Centre for Design and Architecture housed in a building originally designed by Charles Rennie Mackintosh.

Location: The Lighthouse, 11 Mitchell Lane Glasgow, Scotland G1 3NU

Travel: Located a short walk from The Grand Central Hotel:



Conference Dinner

The conference dinner is being held in the auditorium of Òran Mór (a pub/restaurant/venue set up in a former church in the west end of Glasgow), which features a celestial ceiling mural by Alasdair Gray, one of Scotland's largest pieces of public art.

Arrive 18.30 for welcome drinks and canapés, a 3 course dinner will then be served starting at 19.30.

Location: Òran Mór, Top of Byres Road, Glasgow, G12 8QX - http://oran-mor.co.uk

Travel: either a short taxi ride from Grand Central Hotel, or take the Subway (http://www.spt.co.uk/subway/, tickets are £1.40 for a single, £2.60 for a return) from either St Enoch or Buchanan Street stations to Hillhead, then it is a short (~10 minute) walk along Byres Road, with the venue on your right at the corner of Byres Road and Great Western Road. Use the entrance on Great Western Road to get access up to the auditorium.