## Thursday, September 8

**Session 1: Plenary Session (Seiun)**

Chairpersons: Y. Kamakura, *Osaka Univ., Japan*
N. Goldsman, *Univ. Maryland, USA*

9:05

**Opening and Welcome Remarks**
K. Matsuzawa
*Toshiba, Japan*

9:15

**1-1** **TCAD Challenges and some Fraunhofer Solutions**
J. Lorenz
*Fraunhofer IISB, Germany*

10:00

**1-2** **Critical Analysis of 14nm Device Options**
P. Oldiges, R. Muralidhar, P. Kulkarni, C-H. Lin, K. Xiu, D. Guo, M. Bajaj and N. Sathaye
*IBM Corp., USA*

10:45

**1-3** **First-principles study of Si CMOS materials and nanostructures**
K.-J. Chang[1], H.-K. Noh[1], E.-A. Choi[2] and B. Ryu[3]
*[1]KAIST, Korea, [2]Samsung Electronics Co., Ltd., Korea and [3]Samsung Advanced Institute of Technology, Korea*

11:30 **Lunch**

**Session 2: Reliability I (Ginga)**

Chairpersons: Y. Oda, *Panasonic, Japan*
T.-M. Shen, *TSMC, Taiwan*

13:00

**2-1** **Quantum-Mechanical Modeling of NBTI in High-k SiGe MOSFETs**
Ph. Hehenberger[1], W. Goes[1], O. Baumgartner[1], J. Franco[2], B. Kaczer[2] and T. Grasser[1]
*[1]TU Wien, Austria and [2]IMEC, Belgium*

13:20

**2-2** **Multi Scale Modeling of Multi Phonon Hole Capture in the Context of NBTI**

F. Schanovsky, O. Baumgartner and T. Grasser

*TU Wien, Austria*

13:40

**2-3** **Modeling Statistical Distribution of Random Telegraph Noise Magnitude**

K. Sonoda, M. Tanizawa, K. Ishikawa and Y. Inoue

*Renesas Electronics Corp., Japan*

14:00

**2-4** **A Compact Model for Early Electromigration Lifetime Estimation**

R. L. de Orio, H. Ceric and S. Selberherr

*TU Wien, Austria*

**Session 3: Nanowire (Izumi)**

Chairpersons: N. Mori, *Osaka Univ., Japan*

A. Akturk, *Univ. Maryland, USA*

13:00

**3-1** **Effects of Atomic Disorder on Carrier Transport in Si Nanowire Transistors**

H. Minari[1,3], T. Zushi[2], T. Watanabe[2,3], Y. Kamakura[1,3] and N. Mori[1,3]

*[1]Osaka Univ., Japan, [2]Waseda Univ., Japan and [3]CREST, Japan*

13:20

**3-2** **Strong Anisotropy and Diameter Effects on the Low-Field Mobility of Silicon Nanowires**

N. Neophytou and H. Kosina

*TU Wien, Austria*

13:40

**3-3** **Simulation of Channel Electron Mobility Due to Scattering with Interfacial Phonon-Plasmon Modes in Silicon Nanowire under the Presence of High-k Oxide and Metal Gate**

K. Xiu

*IBM SRDC, USA*

14:00

**3-4** **Fully Analytic Compact Model of Ballistic Gate-All-Around MOSFET with Rectangular Cross Section**

T. Numata[1,4], S. Uno[2,4], Y. Kamakura[3,4], N. Mori[3,4] and K. Nakazato[1]
*[1]Nagoya Univ., Japan, [2]Ritsumeikan Univ., Japan, [3]Osaka Univ., Japan and [4]CREST, Japan*

14:20

**3-5** **Analytical model of drain current in nanowire MOSFETs including quantum confinement, band structure effects and quasi-ballistic transport: device to circuit performances analysis**

J. Dura[1,2], S. Martinie[2], D. Munteanu[2], F. Triozon[1], S. Barraud[1], Y.M. Niquet[3] and J.L. Autran[2]
*[1]CEA-LETI MINATEC, France, [2]UMR CNRS, France and [3]INAC, France*

14:40

**3-6** **Electron-phonon scattering in Si and Ge: from bulk to nanodevices**

D. Rideau[1], W. Zhang[2], Y.M. Niquet[3], C. Delerue[2], C. Tavernier[1] and H. Jaouen[1]
*[1]STMicroelectronics, France, [2]ISEN, France and [3]CEA-UJF, France*

15:00 **Coffee Break**

**Session 4: Memory and Spin (Ginga)**

Chairpersons: T. Kurusu, *Toshiba, Japan*
M. Stettler, *Intel, USA*

15:20

**4-1** **KNACK: A Hybrid Spin-Charge Mixed-Mode Simulator for Evaluating Different Genres of Spin-Transfer Torque MRAM Bit-cells**

X. Fong, S. K. Gupta, N. N. Mojumder, S. H. Choday, C. Augustine and K. Roy
*Purdue Univ., USA*

15:40

**4-2** **Study of Current Induced Magnetic Domain Wall Movement with Extremely Low Energy Consumption by Micromagnetic Simulation**

K. Kawabata, M. Tanizawa, K. Ishikawa, Y. Inoue, M. Inuishi and T. Nishimura

*Renesas Electronics Corp., Japan*

16:00

**4-3** **Properties of InAs- and Silicon-Based Ballistic Spin Field-Effect Transistors**

D. Osintsev, V. Sverdlov, A. Makarov and S. Selberherr

*TU Wien, Austria*

16:20

**4-4** **Coupling the Level Set Method with an electro-thermal solver to simulate GST based PCM cells**

A. Glière, O. Cueto and J. Hazart

*CEA, LETI, France*

16:40

**4-5** **Quantum Electronic Trap-to-Band Transitions in Chalcogenides Induced by Electron-Electron Interaction**

F. Buscemi[1], E. Piccinini[1], F. Giovanardi[1], M. Rudan[1], R. Brunetti[2] and C. Jacoboni[2]

*[1]Univ. Bologna, Italy and [2]Univ. Modena and Reggio Emilia, Italy*

**Session 5: Transport (Izumi)**

Chairpersons: M. Ogawa, *Kobe Univ., Japan*

M. Rudan, *Univ. Bologna, Italy*

15:20

**5-1** **Tight-binding Study of Γ-L Bandstructure Engineering for Ballistic III-V nMOSFETs**

Z. Yuan, A. Nainani, X. Guan, H. -S. P. Wong and K. C. Saraswat

*Stanford Univ., USA*

15:40

**5-2** **A Wigner Function-Based Determinist Method for the Simulation of Quantum Transport in Silicon Nanowire Transistors**

S. Barraud, T. Poiroux and O. Faynot

*CEA-Leti, France*

16:00

**5-3** **Wigner Monte Carlo Approach to Quantum and Dissipative Transport in Si-MOSFETs**

S. Koba, H. Tsuchiya and M. Ogawa

*Kobe Univ., Japan*

16:20

**5-4** **Impact of Channel Shape on Carrier Transport Investigated by Ensemble Monte Carlo/Molecular Dynamics Simulation**

T. Kamioka[1,4], H. Imai[1,4], T. Watanabe[1,4], K. Ohmori[2,4], K. Shiraishi[2,4] and Y. Kamakura[3,4]

[1]*Waseda Univ., Japan,* [2]*Tsukuba Univ., Japan,* [3]*Osaka Univ., Japan and* [4]*JST-CREST, Japan*

16:40

**5-5** **Large-Signal Full-Band Monte Carlo Device Simulation of Millimeter-Wave Power GaN HEMTs with the Inclusion of Parasitic and Reliability Issues**

D. Guerra[1], D. K. Ferry[1], S. M. Goodnick[1], M. Saraniti[1] and F. A. Marino[2]

[1]*Arizona State Univ., USA and* [2]*Univ. Padova, Italy*

17:00

**5-6** **Efficient Simulation of Quantum Cascade Lasers using the Pauli Master Equation**

O. Baumgartner, Z. Stanojević and H. Kosina

TU Wien, Austria

18:00 **Reception**

## Friday, September 9

**Session 6: TCAD (Ginga)**

Chairpersons: S. Yamakawa, *Sony Corp., Japan*

J. Lorentz, *Fraunhofer IISB, Germany*

9:00

**6-1** **(Invited) The Non-Equilibrium Green Function approach as a TCAD tool for future CMOS technology**

A. Martinez[1], N. Seoane[2], M. Aldegunde[3], A. Asenov[4] and J.-R. Barker[4]

[1]*Univ. Swansea, UK ,* [2]*Univ. Santiago de Compostela, Spain,* [3]*CESGA, Spain and* [4]*Univ. Glasgow, UK*

9:30

**6-2** **Exploring MOL Design Options for a 20nm CMOS Technology using TCAD**

A. Scholze, S. Furkay, S-D. Kim and S. Jain
*IBM SRDC, USA*

9:50

**6-3** **Impact of Substrate Bias on GIDL for Thin-BOX ETSOI Devices**
P. Kulkarni[1], Q. Liu[2], A. Khakifirooz[1], Y. Zhang[1], K. Cheng[1], F. Monsieur[2] and P. Oldiges[1]
*[1]IBM, USA and [2]STMicroelectronics, USA*

10:10 **Coffee Break**

10:30

**6-4** **Impact of Quantum Confinement on Stress induced nMOSFET Threshold Voltage Shift**
H. Takashino, M. Tanizawa, T. Okagaki, T. Hayashi, M. Taya, H. Ishida, K. Ishikawa and Y. Inoue
*Renesas Electronics Corp., Japan*

10:50

**6-5** **Thermoelectromechanical Simulation of GaN HEMTs**
M.G. Ancona and S.C. Binari
*Naval Research Lab., USA*

11:10

**6-6** **Development of $SF_6/O_2$/Si Plasma Etching Topography Simulation Model using New Flux Estimation Method**
T. Ikeda[1], H. Saito[1], F. Kawai[1], K. Hamada[1], T. Ohmine[2], H. Takada[2] and V. Deshpande[3]
*[1]Toyota Motor Corp., Japan, [2]Nihon Synopsys G.K., Japan and [3]Synopsys Switzerland LLC, Switzerland*

11:30 **Lunch**

**Session 7: Reliability II (Ginga)**

Chairpersons: K. Sonoda, *Renesas Electronics, Japan*
C. Mouli, *Micron Semiconductor, USA*

13:00

**7-1** **(Invited) Density Functional Theory Based Simulation of Carrier Transport in Silicon**

**Carbide and Silicon Carbide-Silicon Dioxide Interfaces**

A. Akturk[1], S. Salemi[1], N. Goldsman[1], S. Potbhare[1] and A. Lelis[2]

*[1]Univ. Maryland, USA and [2]Army Research Lab., USA*

13:30

**7-2** **Secondary generated holes as a crucial component for modeling of HC degradation in high-voltage n-MOSFET**

S. Tyaginov[1], I. Starkov[1], O. Triebl[1], H. Ceric[1], T. Grasser[1], H. Enichlmair[2], J.M. Park[2] and C. Jungemann[3]

*[1]TU Wien, Austria, [2]Austriamicrosystems AG, Austria and [3]RWTH Aachen, Germany*

13:50

**7-3** **Analysis of Worst-Case Hot-Carrier Degradation Conditions in the Case of n- and p-channel High-Voltage MOSFETs**

I. Starkov[1], H. Ceric[1], S. Tyaginov[1], T. Grasser[1], H. Enichlmair[2], J.M. Park[2] and C. Jungemann[3]

*[1]TU Wien, Austria, [2]Austriamicrosystems AG, Austria and [3]RWTH Aachen, Germany*

14:10

**7-4** **Reliability of NAND Flash Memories Induced by Anode Hole Generation in Floating-Gate**

Y. Kitahara, D. Hagishima and K. Matsuzawa

*Toshiba Corp., Japan*

14:30

**7-5** **Multilevel Simulation for the Investigation of Fast Diffusivity Paths**

H. Ceric, R. L. de Orio, F. Schanovsky, W. H.Zisser and S. Selberherr

TU Wien, Austria

15:00-17:00

**Poster Session (Izumi)**

Chairperson: S. Amakawa, *Hiroshima Univ., Japan*

**P1** **High-Quality Mesh Generation Based on Orthogonal Software Modules**

J. Weinbub, J. Cervenka, K. Rupp and S. Selberherr

*TU Wien, Austria*

**P2** **A Versatile Finite Volume Simulator for the Analysis of Electronic Properties of Nanostructures**

Z. Stanojević [1], M. Karner[2], K. Schnass[2], C. Kernstock[2], O. Baumgartner[1] and H.Kosina[1]
*[1]TU Wien, Austria and [2]Global TCAD Solutions, Austria*

**P3** **Parallel Preconditioning for Spherical Harmonics Expansions of the Boltzmann Transport Equation**

K. Rupp, T. Grasser and A. Jüngel
*TU Wien, Austria*

**P4** **Adaptive Variable-Order Spherical Harmonics Expansion of the Boltzmann Transport Equation**

K. Rupp, T. Grasser and A. Jüngel
*TU Wien, Austria*

**P5** **Inverse Modeling of sub-100nm MOSFET with PDE-Constrained Optimization**

C. Shen and D. Gong
*Cogenda Pte Ltd., Singapore*

**P6** **A Smart Approach for Process Variation Correlation Modeling**

C-K. Lin, C. Hsiao, W-M. Chan and M-C. Jeng
*Taiwan Semiconductor Manufacturing Co., Taiwan*

**P7** **A Parameterized SPICE Macromodel of Resistive Random Access Memory and Circuit Demonstration**

H-L. Chang[1], H-C. Li[1], C. W. Liu[1], F. Chen[2] and M.-J. Tsai[2]
*[1]National Taiwan Univ., Taiwan, R.O.C and [2]Industrial Technology Research Instit., Taiwan, R.O.C.*

**P8** **The Flexible Compact SOI-MOSFET Model HiSIM-SOI Valid for Any Structural Types**

M. Miyake[1], S. Kusu[1], H. Kikuchihara[1], A. Tanaka[1], Y. Shintaku[1], M. Ueno[1],
J. Nakashima[1], U. Feldmann[1,] H. J. Mattausch[1], M. Miura-Mattausch[1] and T. Yoshida[2]
*[1]Hiroshima Univ., Japan and [2]NEC Informatec Systems, Ltd., Japan*

**P9** **Modeling of Enhanced 1/f Noise in TFT with Trap Charges**

T. Nakahagi[1], D. Sugiyama[1], S. Yukuta[1], M. Miyake[1], M. Miura-Mattausch[1] and S. Miyano[2]
*[1]Hiroshima Univ., Japan and [2]NEC Energy Device, Ltd., Japan*

**P10** **Physical Circuit-Device Simulation of ESD and Power Devices**

V. Axelrad[1], H. Hayashi[2] and I. Kurachi[3]
*[1]SEQUOIA Design Systems Inc., USA, [2]OKI Semiconductor Co. Ltd., Japan and [3]Powerchip Technology Corp., Taiwan*

**P11** **A Novel Simulation Methodology for Development of ESD Primitives on a 0.18µm Analog, Mixed-Signal High Voltage Process Technology**

F. Roger, J. Cambieri and R. Minixhofer
*Austriamicrosystems, Austria*

**P12** **TCAD simulations of irradiated power diodes over a wide temperature range**

M. Bellini[1] and J. Vobecký[2]
*[1]ABB CHCRC, Switzerland and [2]ABB Semiconductors Ltd, Switzerland*

**P13** **3D TCAD Simulation of Advanced CMOS Image Sensors**

Z. Essa[1,2], P. Boulenc[1], C. Tavernier[1], F. Hirigoyen[1], A. Crocherie[1] and J. Michelot[1]
*[1]STMicroelectronics, France and [2]PHELMA Grenoble INP, France*

**P14** **a-Si/c-$Si_{1-x}Ge_x$/c-Si Heterojunction Solar Cells**

S. A. Hadi[1], A. Nayfeh[1], P. Hashemi[2] and J. Hoyt[2]
*[1]Masdar Inst. Science and Technol., UAE and [2]MIT, USA*

**P15** **Impact of Energetic Disorder and Localization on the Conductivity and Mobility of Organic Semiconductors**

F. Torricelli[1], L. Colalongo[2], L. Milani[2], Z. M. K.-Vajna[2] and E. Cantatore[1]
*[1]Eindhoven Univ. of Technol., Netherlands and [2] Brescia Univ., Italy*

**P16** **Effect of the trap density and distribution of the silicon nitride layer on the retention characteristics of charge trap flash memory devices**

J. H. You[1], H. W. Kim[1], D. H. Kim[1], T. W. Kim[1] and K. W. Lee[2]
*[1]Hanyang Univ., Korea and [2]Hynix Semiconductor Inc., Korea*

**P17** **Enhancement of the device characteristics for nanoscale charge trap flash memory devices utilizing a metal spacer layer**

H. W. Kim[1], J. H. You[1], D. U. Lee[1], T. W. Kim[1] and K. W. Lee[2]

*[1]Hanyang Univ., Korea and [2]Hynix Semiconductor Inc., Korea*

**P18** **An Abnormal Floating Gate Interference and a Low Program Performance in 2y nm NAND Flash Devices**

E. Kwon, D. Oh, B. Lee, J-H. Yi, S. Kim, G. Cho, S. Park and J. Choi

*Hynix Semiconductor Inc., Korea*

**P19** **First Principles Study of the Switching Mechanism in Resistance Random Access Memory Devices**

H. Kasai[1], S. M. Aspera[1], H. Kishi[1], N. Awaya[2], S. Ohnishi[2] and Y. Tamai[2]

*[1]Osaka Univ., Japan and [2]Sharp Corp., Japan*

**P20** **First Principle Study of the Stability of H Atoms in SiN Layers on MONOS-Type Memories During Program/Erase Operations**

K. Yamaguchi[1], A. Otake[1], K. Kamiya[1], K. Shiraishi[1] and Y. Shigeta[2]

*[1]Tsukuba Univ., Japan and [2]Osaka Univ., Japan*

**P21** **Study on Carrier Mobility in Graphene Nanoribbons**

X. Yu[1], J. Zhang[1], J. Kang[1], H. Qian[1], Z. Yu[1] and Y. Tan[2]

*[1]Tsinghua Univ., China and [2]Purdue Univ., USA*

**P22** (withdrawn)

**P23** **Nanostructuration of Graphene Nanoribbons for thermoelectric applications**

F. Mazzamuto, J. S-Martin, V. H. Nguyen, Y. Apertet and P. Dollfus

*Paris-Sud Univ., France.*

**P24** **Analysis of geometrical structure and transport property in InAs/Si heterojunction nanowire tunneling field effect transistors**

Y. Miyoshi[1], M. Ogawa[1], S. Souma[1] and H. Nakamura[2]

*[1]Kobe Univ., Japan and [2]IBM-Japan, Japan*

**P25** **Simulation of Plasma Immersion Ion Implantation**

A. Burenkov[1], P. Pichler[1], J. Lorenz[1], Y. Spiegel[2], J. Duchaine[2] and F. Torregrosa[2]
*[1]Fraunhofer IISB, Germany and [2]Ion Beam Services, France*

**P26** **Sticking coefficient of hydrogen radicals on ArF photoresist estimated by parallel plate structure in conjunction with numerical analysis**

A. Malinowski[1,2,3], M. Sekine[1], M. Hori[1], K. Ishikawa[1], H. Kondo[1], T. Suzuki[1], T. Takeuchi[1], H. Yamamoto[1], A. Jakubowski[2], L. Lukasiak[2] and D. Tomaszewski[3]
*[1]Nagoya Univ., Japan, [2]Warsaw Univ. of Technol., Poland and [3]Inst. Electron Technol., Poland*

## Saturday, September 10

**Session 8: Compact Model (Ginga)**

Chairpersons: T. Tanaka, *Fujitsu Semiconductor, Japan*
A. Heringa, *NXP Semiconductors, Netherland*

9:20

**8-1** **(Invited) A Spice-based Multi-physics Simulation Technique for Integrated MEMS**

H. Toshiyoshi
*Univ. Tokyo, Japan*

9:50 **Coffee Break**

10:10

**8-2** **2D Analytical Model for the Study of NEM Relay Device Scaling**

X. Shen, S. Chong, D. Lee, R. Parsa, R. T. Howe and H.-S. P. Wong
*Stanford Univ., USA*

10:30

**8-3** **Accurate and global model of SOI H gate body-tied MOSFET for circuit simulator**

M. Mochizuki[1], H. Hayashi[1], S. Ishii[1], S. Ohira[1], I. Kurachi[1] and N. Miura[2]
*[1]Oki Semiconductor Co., Ltd., Japan and [2]Oki Semiconductor Miyagi Co., Ltd., Japan*

10:50

**8-4** **Modeling Temperature and Bias Stress Effect on Threshold Voltage of a-Si:H TFTs for Gate Driver Circuit Simulation**

C.-H. Shen, Y. Li, I.-H. Lo, P.-J. Lin and S.-C. Chung

*National Chiao Tung Univ., Taiwan*

11:10

**8-5** **Characterization and Modeling of Self-Heating Effect on Transient Current Overshoot in Poly-Si TFTs Fabricated on Glass Substrate**

T. Ota[1], H. Tsuji[1,2], Y. Kamakura[1] and K. Taniguchi[1]
*[1]Osaka Univ., Japan and [2]CREST, Japan*

**Session 9: Tunneling (Izumi)**

Chairpersons: K. Fukuda, *AIST, Japan*
T. Grasser, *TU Wien, Austria*

10:10

**9-1** **3D Modeling based on Current Continuity for STM Carrier Profiling of Semiconductor Devices**

K. Fukuda[1], M. Nishizawa[1], T. Tada[1], L. Bolotov[2], K. Suzuki[3], S. Sato[3], H. Arimoto[1] and T. Kanayama[1]
*[1]NIRC AIST, Japan, [2]Tsukuba Univ., Japan and [3] Fujitsu Semiconductor Ltd., Japan*

10:30

**9-2** **Analysis of Si, InAs, and Si-InAs Tunnel Diodes and Tunnel FETs Using Different Transport Models**

A. Schenk[1], R. Rhyner[1], M. Luisier[2] and C. Bessire[3]
*[1]ETH Zürich, Switzerland, [2]Purdue Univ., USA and [3]IBM Research-Zurich, Switzerland*

10:50

**9-3** **Analytical Approximation of Complex Band Structures for Band-to-Band Tunneling Models**

X.Guan, D. Kim, K. C. Saraswat and H.-S. P. Wong
*Stanford Univ., USA*

11:10

**9-4** **Field Induced Quantum Confinement in Indirect Semiconductors: Quantum Mechanical and Modified Semiclassical Model**

W. G. Vandenberghe[1,2], B. Sorée[1,2], W. Magnus[1,3], G. Groeseneken[1,2], A. S. Verhulst[1] and M. V. Fischetti[4]
*[1]imec, Belgium, [2]Katholieke Univ. Leuven, Belgium, [3]Univ. Antwerpen, Belgium and [4]Univ. Texas Dallas, USA*

11:30 **Lunch**

**Session 10: Fluctuation (Ginga)**

Chairpersons: Y. Li, *National Chiao Tung Univ., Taiwan*
A. Martinez, *Univ. Glasgow, UK*

13:00

**10-1** **Statistical MOSFET Current Variation Due to Variation in Surface Roughness Scattering**

C.L. Alexander[1] and Asen Asenov[1,2]

*[1]Univ. Glasgow, UK and [2]Gold Standard Simulations Ltd., UK*

13:20

**10-2** **A Mobility Model Correction for 'Atomistic' Drift-Diffusion Simulation**

S. M. Amoroso[1], C. L. Alexader[2], S. Markov[2], G. Roy[3] and A. Asenov[2,3]

*[1]Politecnico di Milano-IU.NET, Italy, [2]Univ. Glasgow, UK and [3]Gold Standard Simulations Ltd., UK*

13:40

**10-3** **The Effect of Compact Modelling Strategy on SNM and Read Current variability in Modern SRAM**

P. Asenov[1], F. A. –Lema[1], S. Roy[1], C. Millar[1,2], A. Asenov[1,2], G. Roy[2], U. Kovac[2] and D. Reid[2]

*[1]Univ. Glasgow, UK and [2]Gold Standard Simulations Ltd., UK*

14:00

**10-4** **Nanosized Metal Grains Induced Electrical Characteristic Fluctuation in 16 nm Bulk and SOI FinFET Devices with TiN/$HfO_2$ Gate Stack**

H.-W. Cheng, Y. Li, C.-Y. Yiu and H.-W. Su

*National Chiao Tung Univ., Taiwan*

14:20

**10-5** **Correlation between Interface Traps and Random Dopants in Emerging MOSFETs**

Y.-Y.Chiu, Y. Li and H.-W. Cheng

*National Chiao Tung Univ., Taiwan*

14:40

**10-6** **Schottky-barrier change by structural disorders at metal/Si interfaces: First-principles study**

K. Kobinata and T. Nakayama

*Chiba Univ., Japan*

**Session 11: Numerical Simulation Method (Izumi)**

Chairpersons: T. Iwasaki, *Hitachi Ltd., Japan*

P. Oldiges, *IBM, USA*

13:00

**11-1** **A Wavelet Method to Solve High-dimensional Transport Equations in Semiconductor Devices**

V. Peikert and A. Schenk

*ETH Zürich, Switzerland*

13:20

**11-2** **Numerical Methods for A Quantum Energy Transport Model Arising in Scaled MOSFETs**

S. Sho and S.Odanaka

*Osaka Univ., Japan*

13:40

**11-3** **A Level Set Simulator for Nanooxidation using Non-Contact Atomic Force Microscopy**

L. Filipovic and S. Selberherr

*TU Wien, Austria*

14:00

**11-4** **Bridge-Function Pseudospectral Method for Quantum Mechanical Simulation of Nano-Scaled Devices**

Y. Saitou, T. Nakamori, S. Souma and M. Ogawa

*Kobe Univ., Japan*

14:20

**11-5** **Low-dimensional Quantum Transport Models in Atomistic Device Simulations**

G. Mil'nikov[1,2], N. Mori[1,2] and Y. Kamakura[1,2]

[1]*Osaka Univ., Japan and* [2]*CREST, JST, Japan*