Interaction between TCAD, compact models and circuit simulation

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www.elec.gla.ac.uk/groups/dev_mod

Summary

- Background
- Statistical variability
- Statistical compact models
- Statistical circuit simulation
- Conclusions

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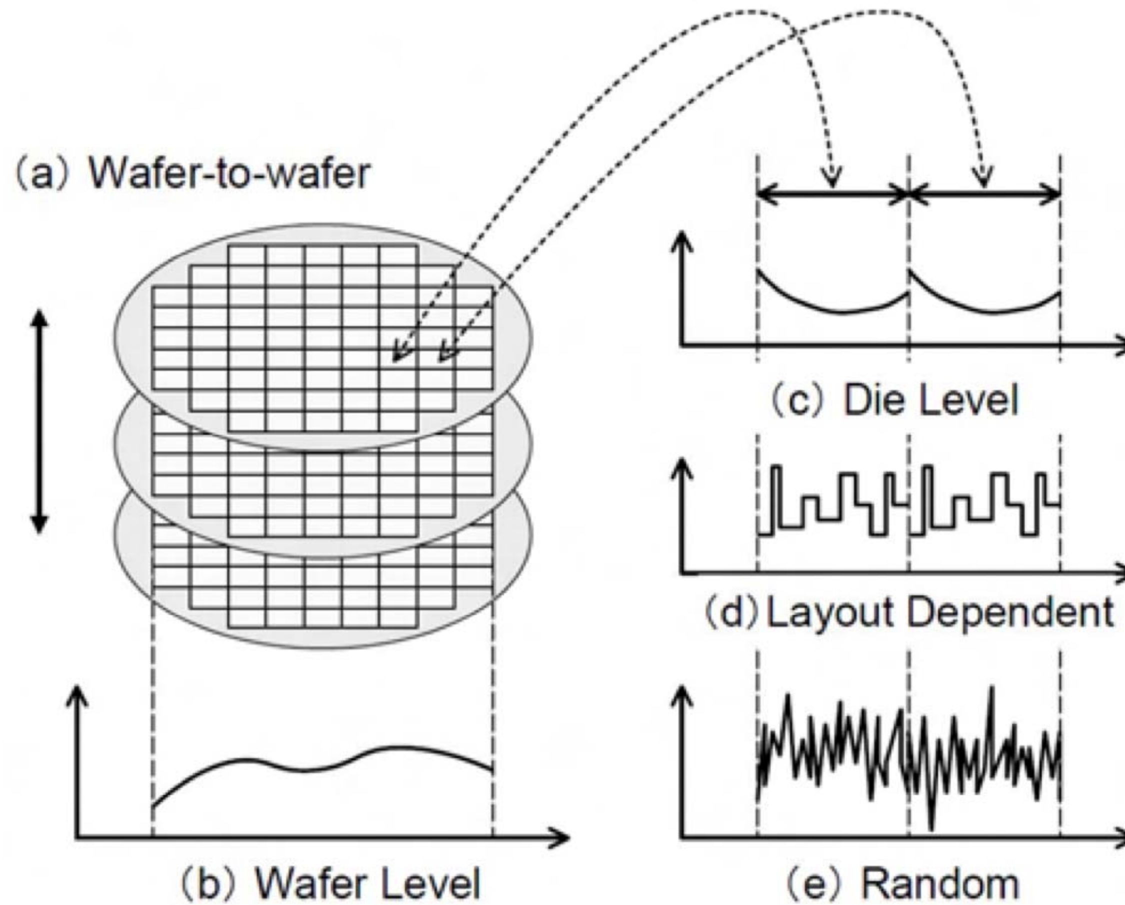
Summary

- Background

Variability classification



After K. Takeuchi (NEC)

Variability in 65 nm (L=60 nm, W=140 nm)

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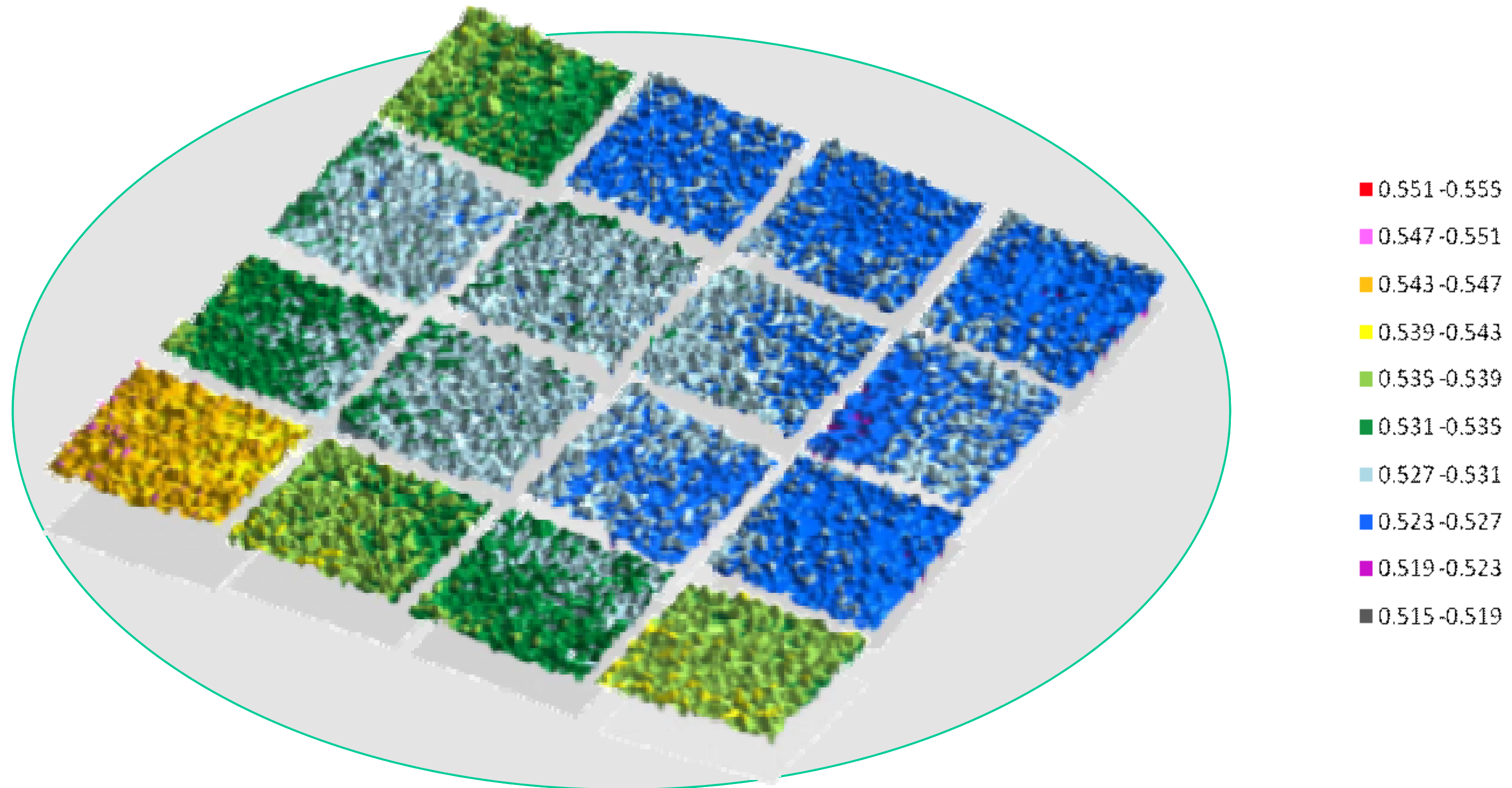
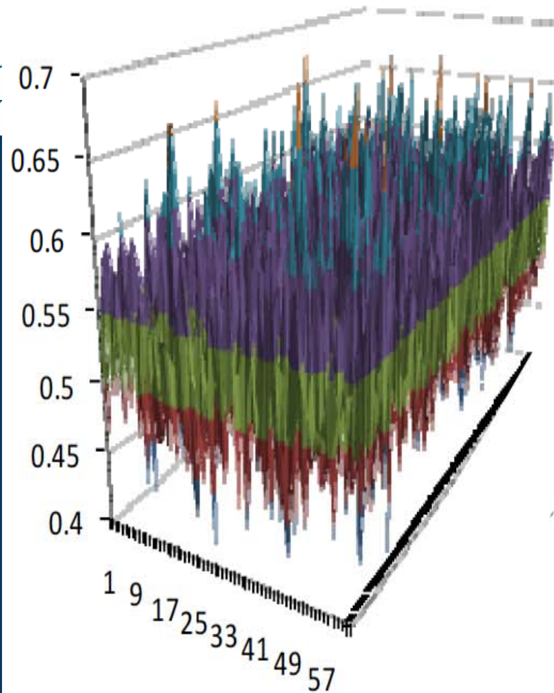


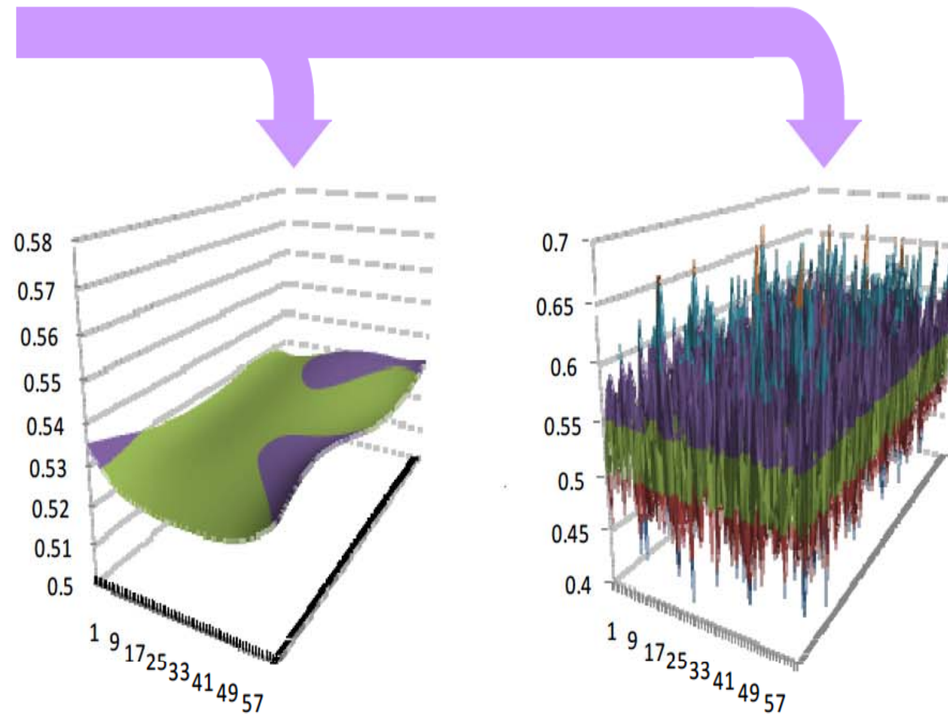
T. Hiramoto (Tokyo Univ)

Variability in 65 nm (L=60 nm, W=140 nm)

University of Glasgow



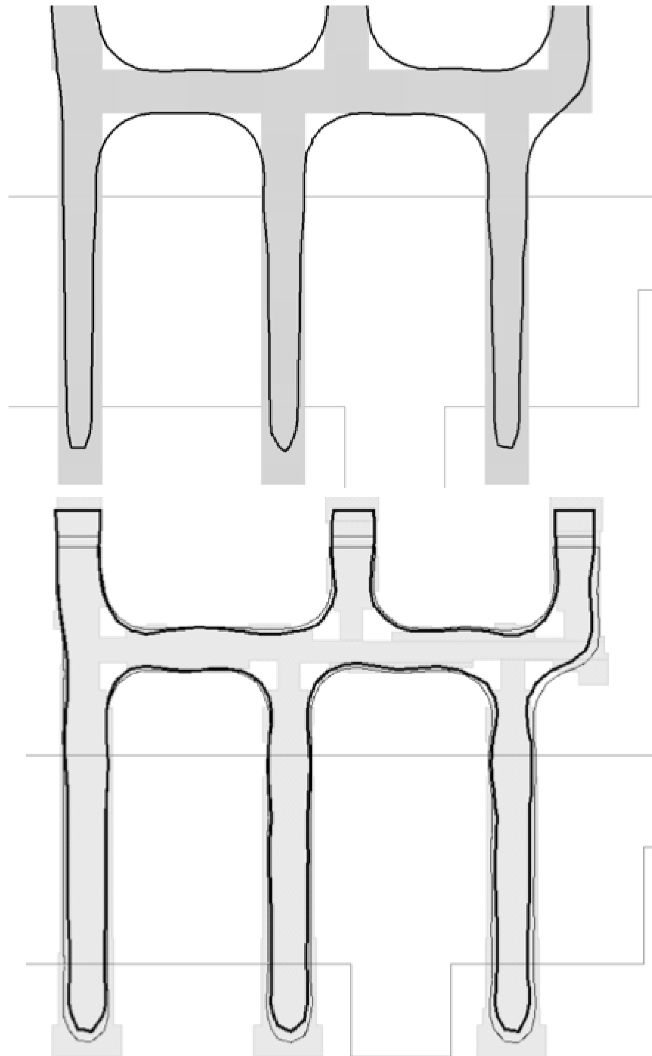
Original distribution data

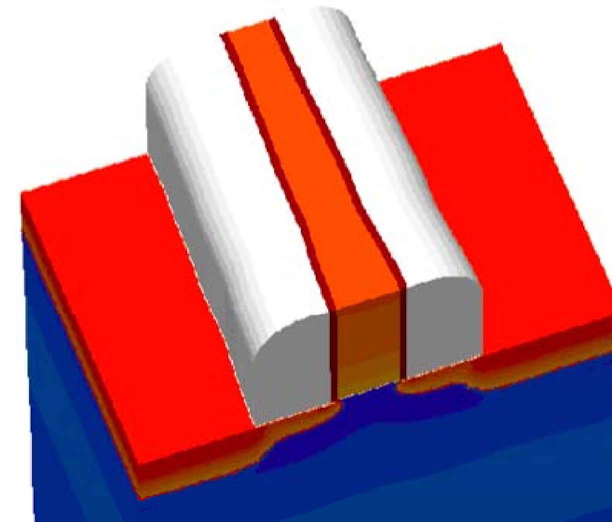


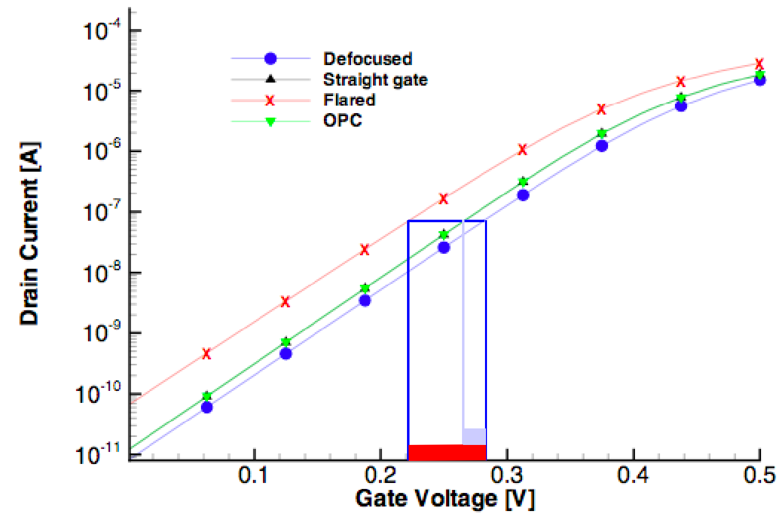
T. Hiramoto (Tokyo Univ)

OPC and strain related variability

65 nm example Synopsys (SISPAD 06)

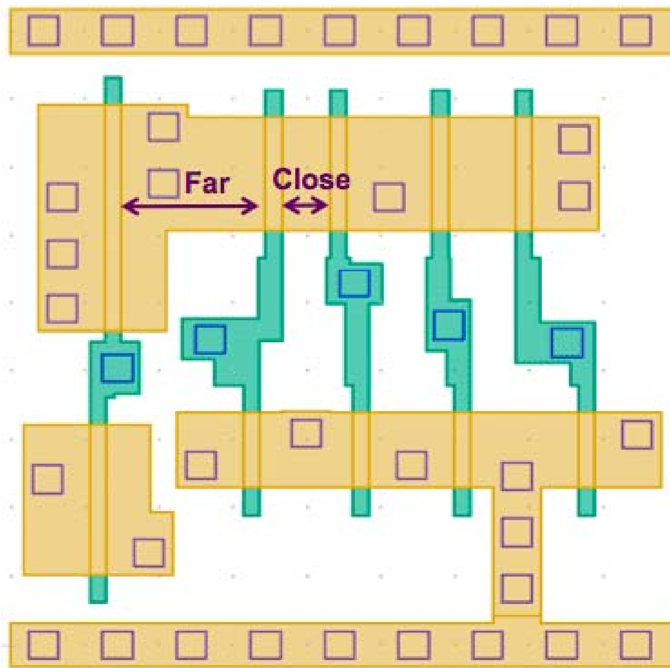


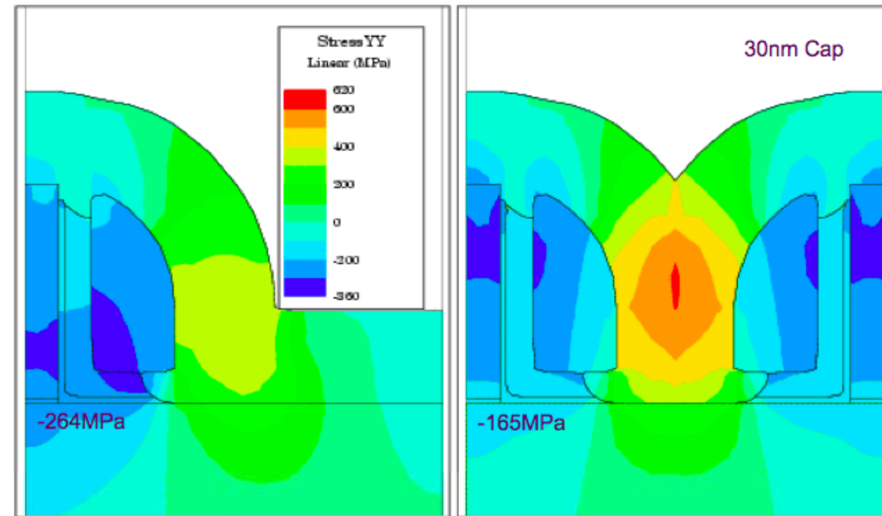


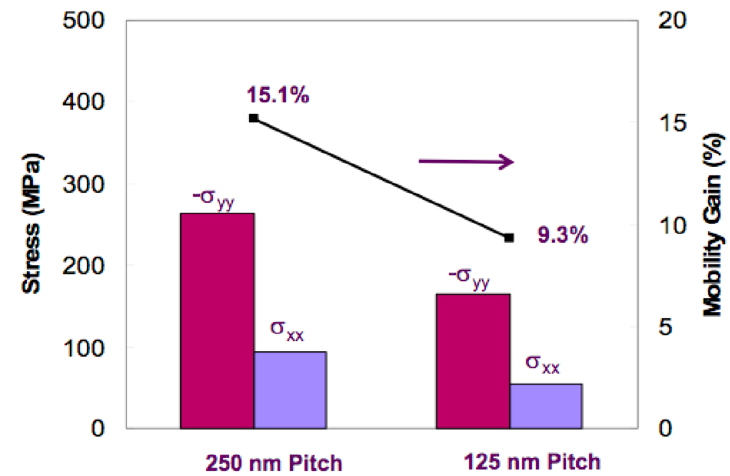


Strain induced variability

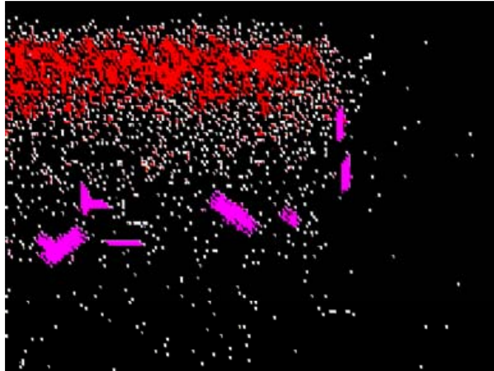
After W. Fichtner

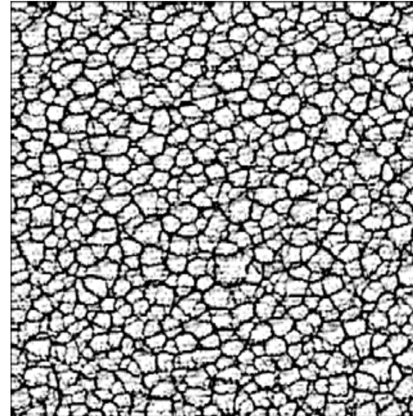


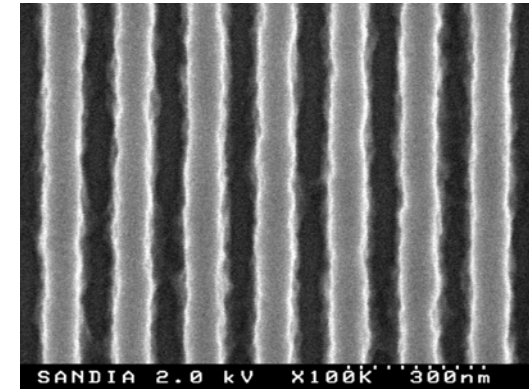


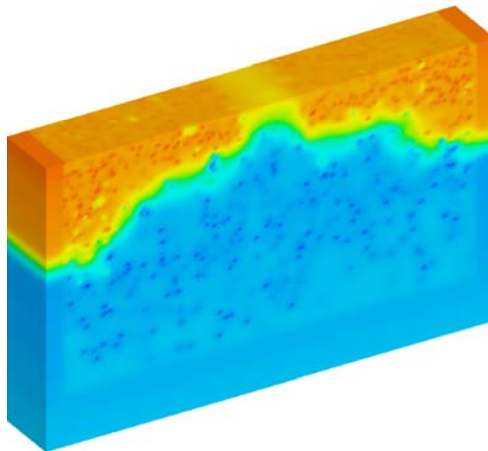


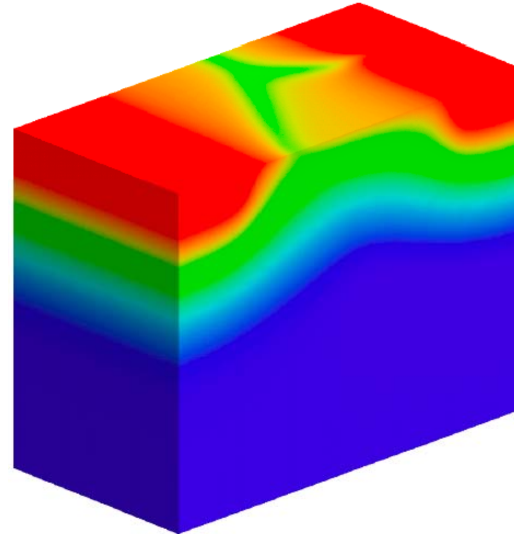
Statistical variability

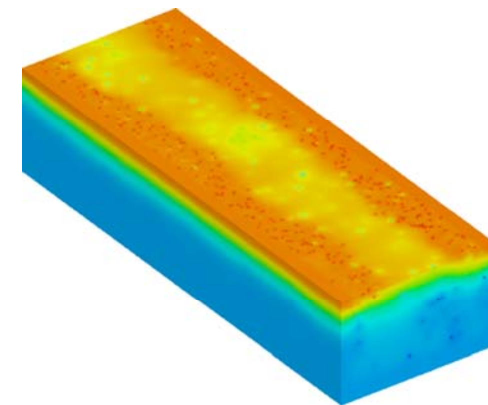










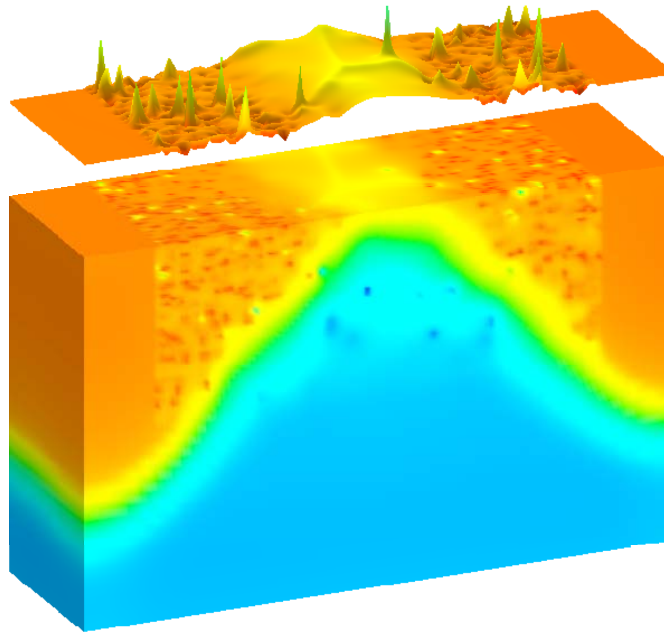


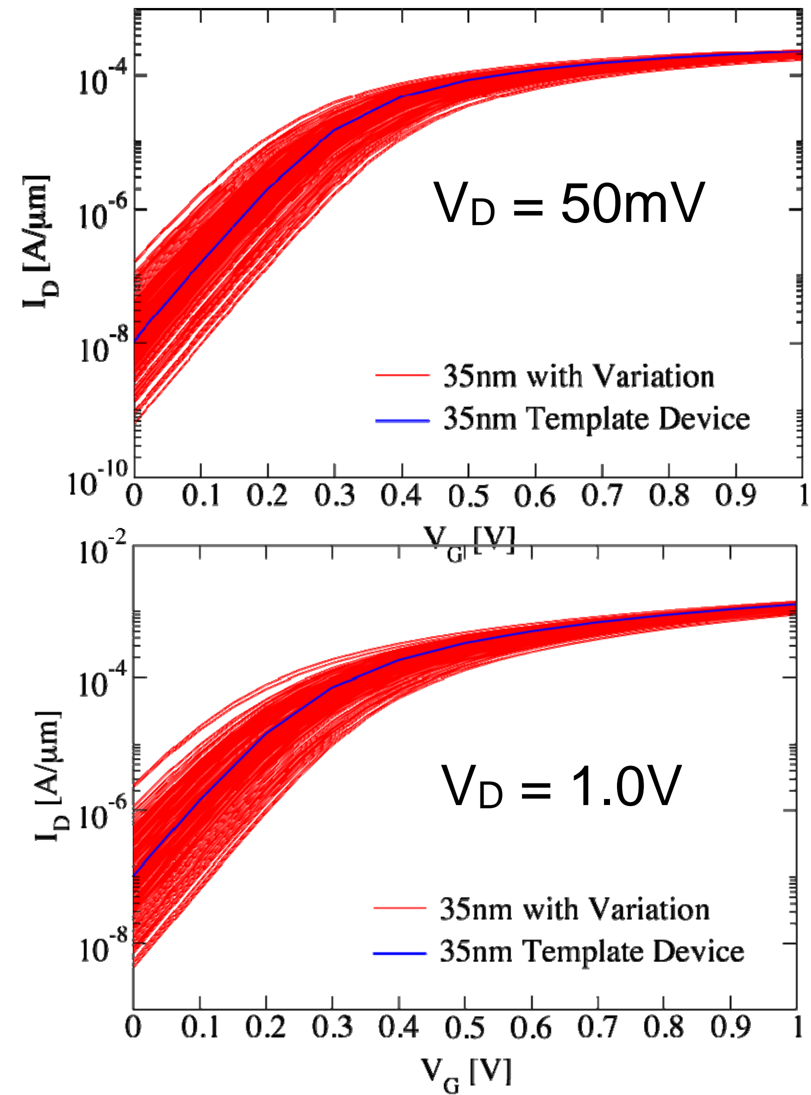
Random dopants

Polysilicon/high-k Granularity

Line edge roughness

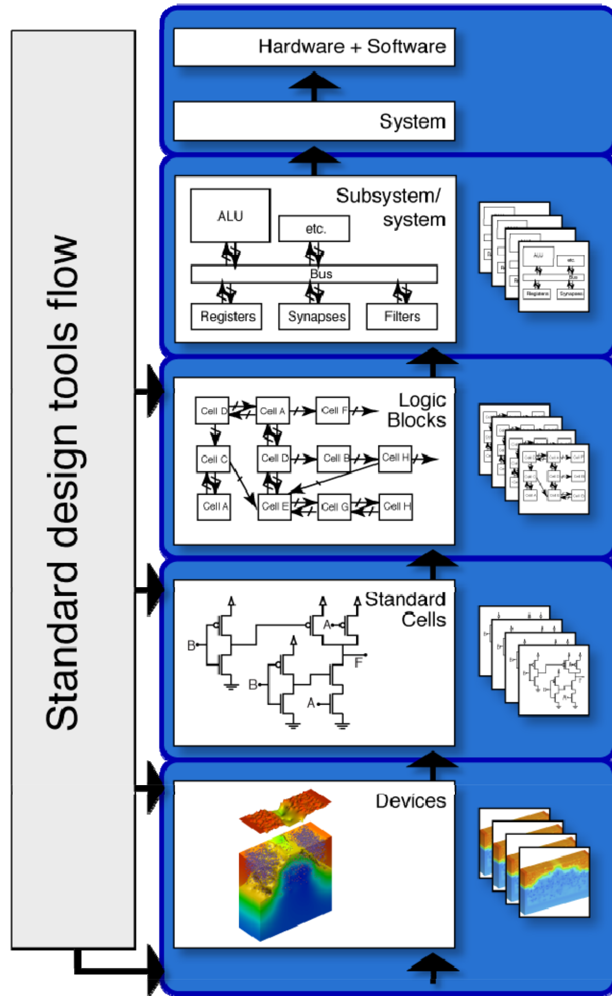
The most comprehensive technology available

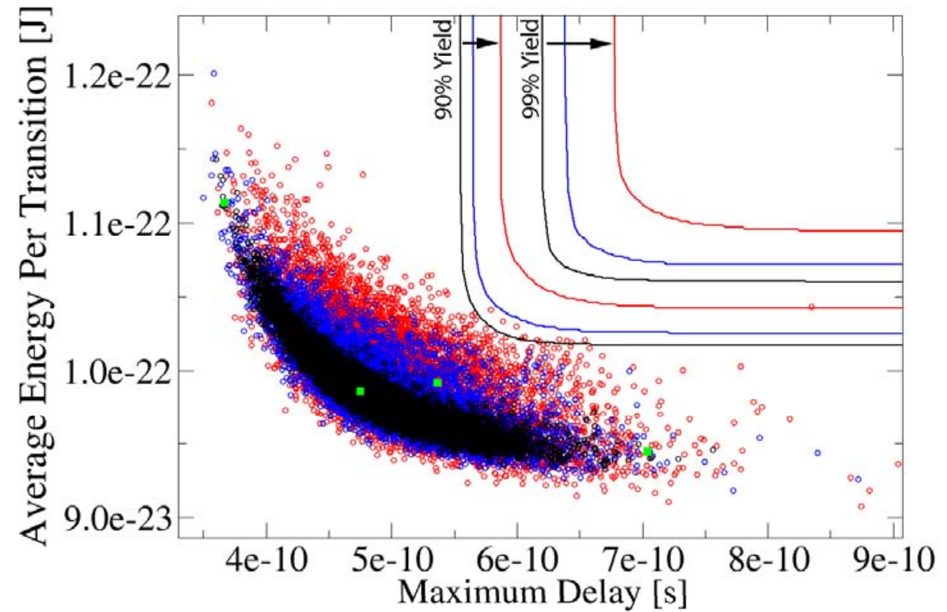


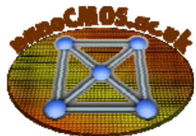


RDD+LER+PSG
Compact models

Hierarchical statistical simulation and verification







Performance/power/yield trade off is a necessity

Summary

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- Statistical variability
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Transport (scattering) related variability

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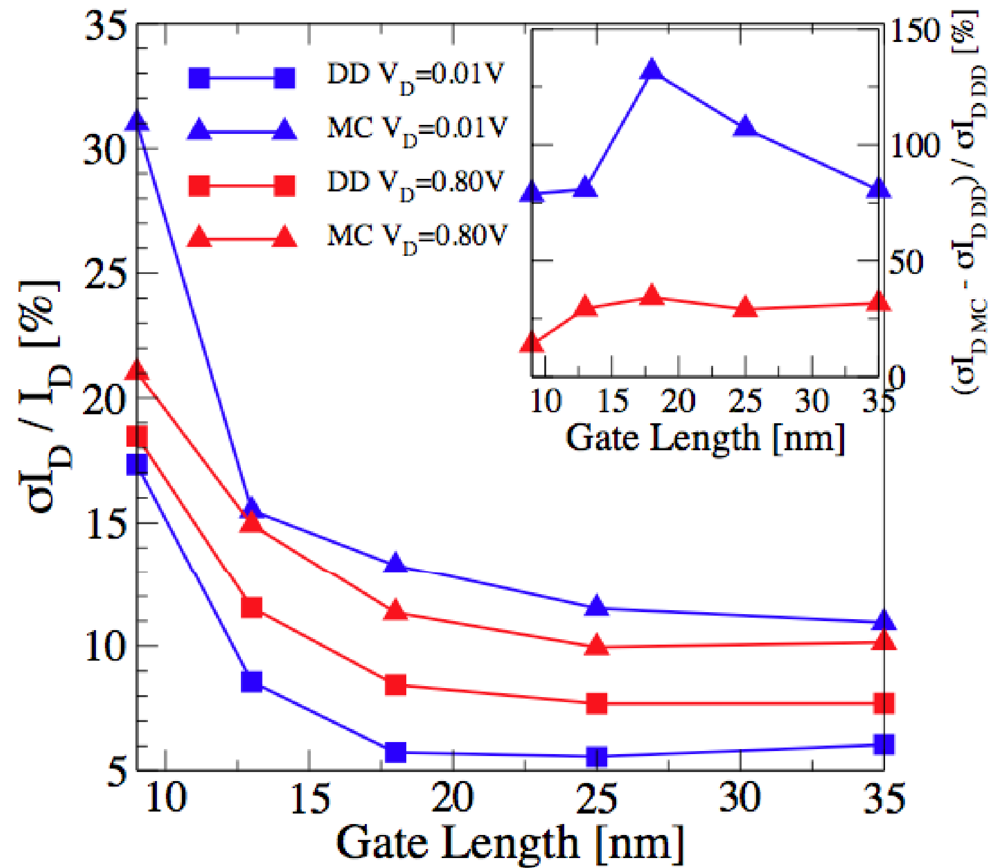
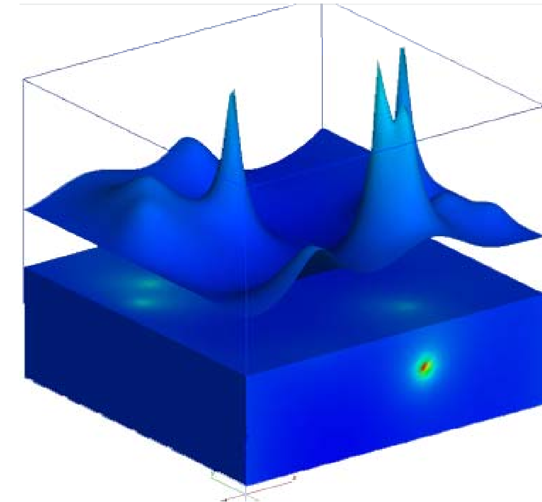
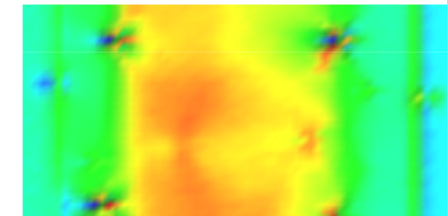
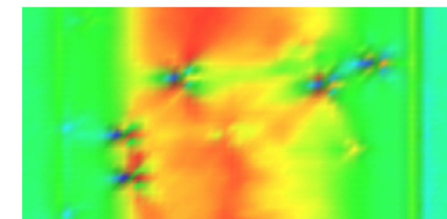
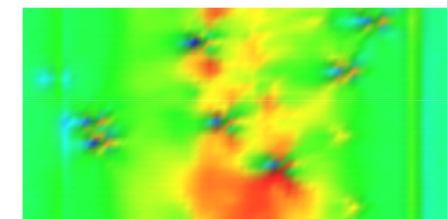




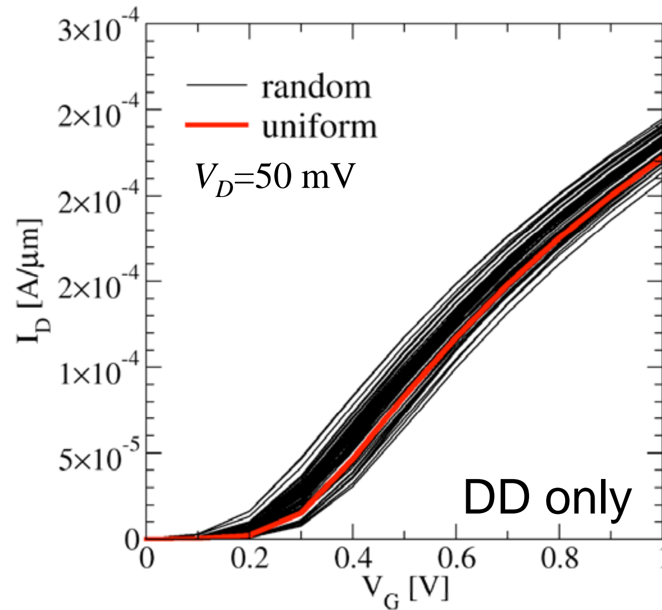


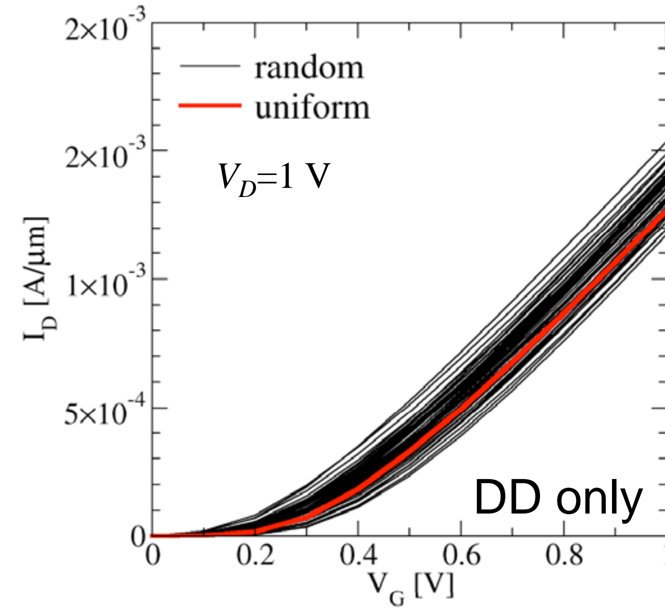


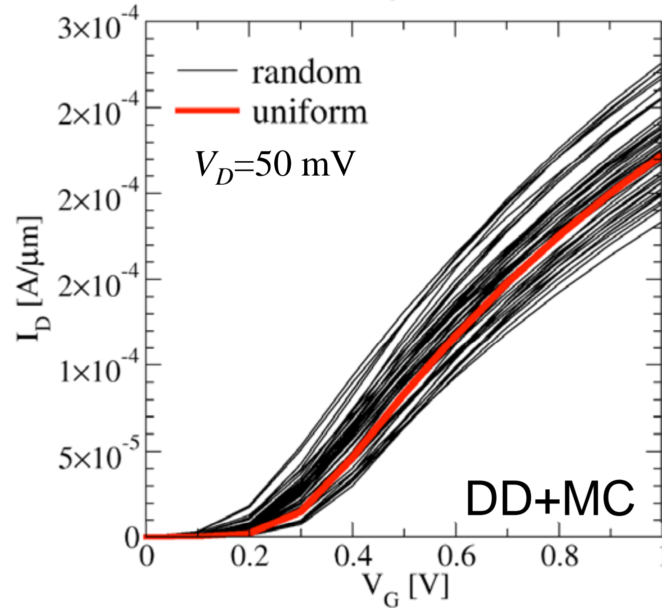


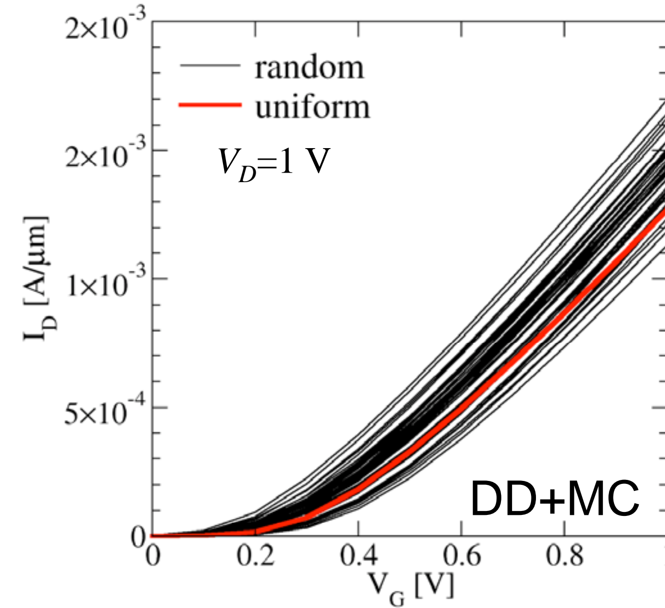
DEVICE MODELLING GROUP

The impact of the transport related variability





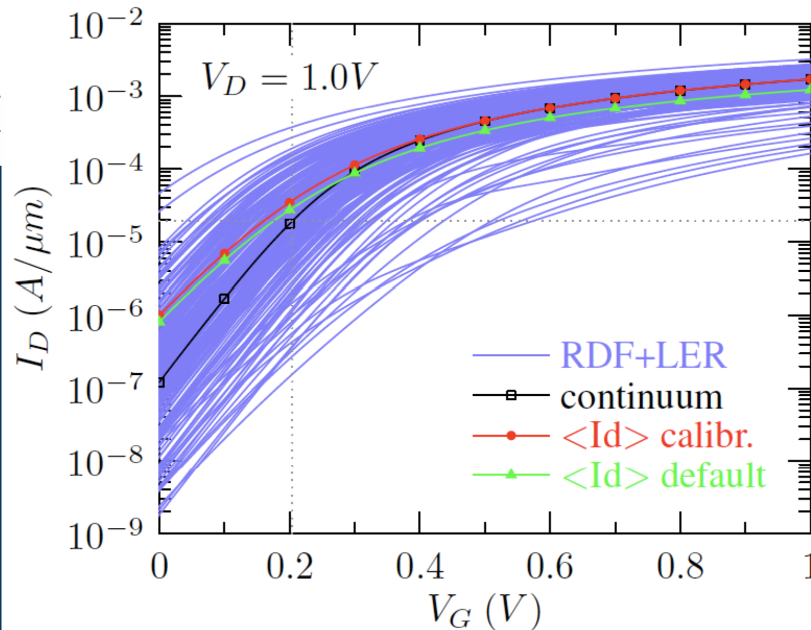


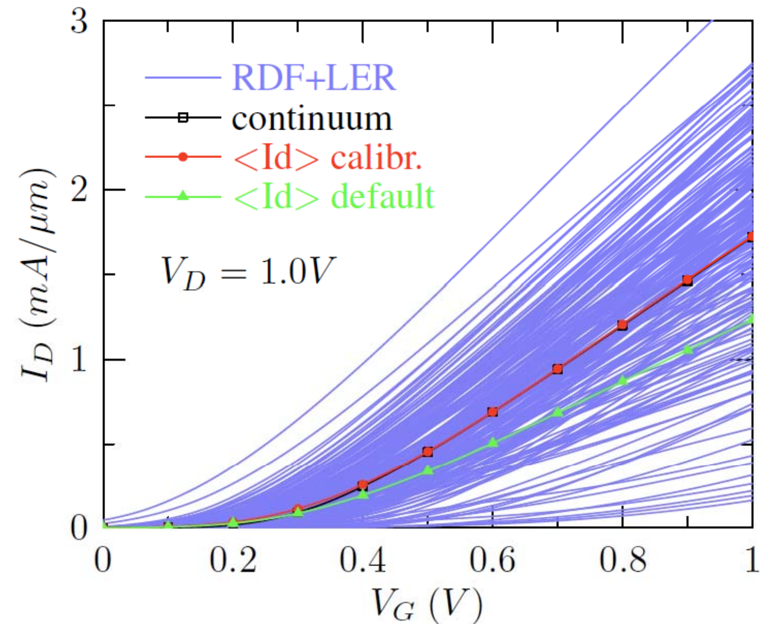


35 nm MOSFET

Generation of target Id-Vg characteristics

18 nm MOSFETs



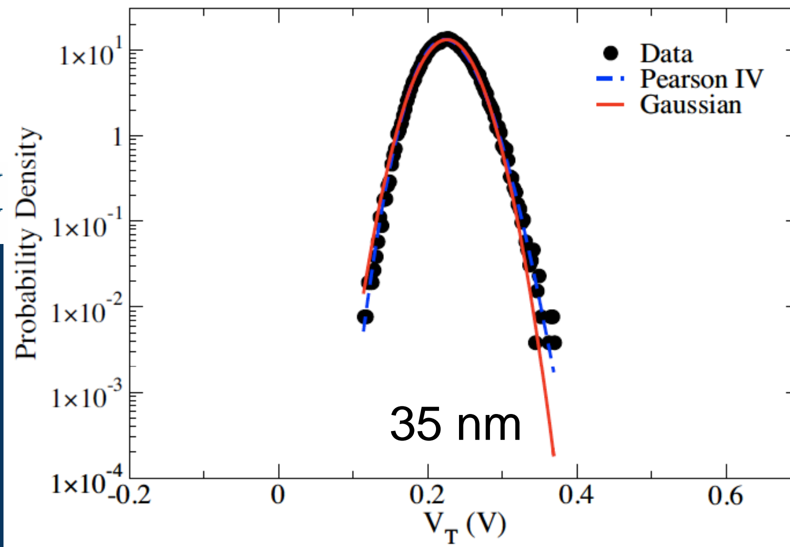


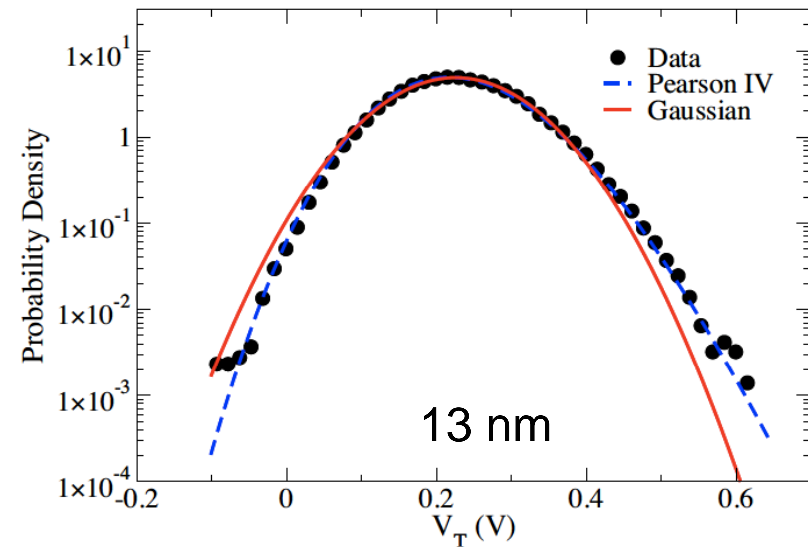
Generation of full target Id-Vg characteristics is tricky

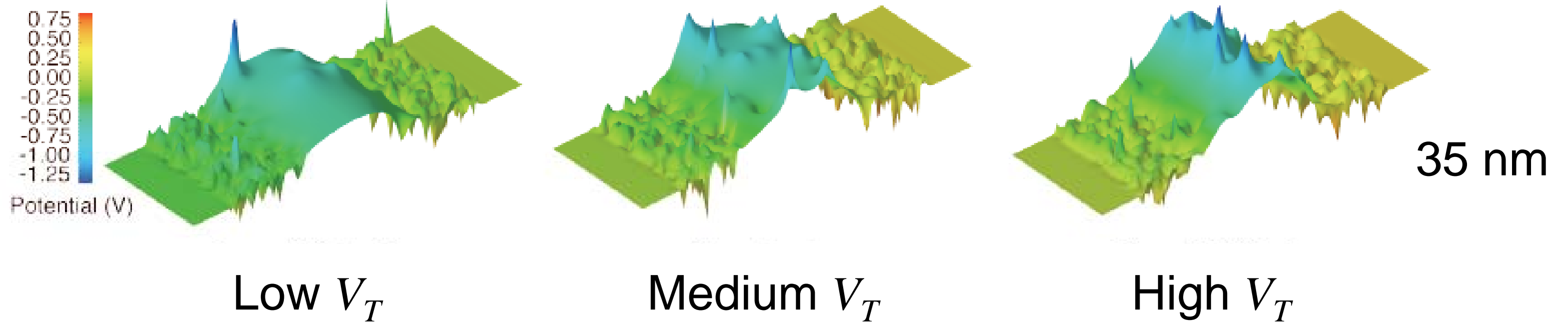
Special attention has to be paid to:

- Resolution of the individual dopants
- Doping concentration and field mobility models
- Statistical calibration

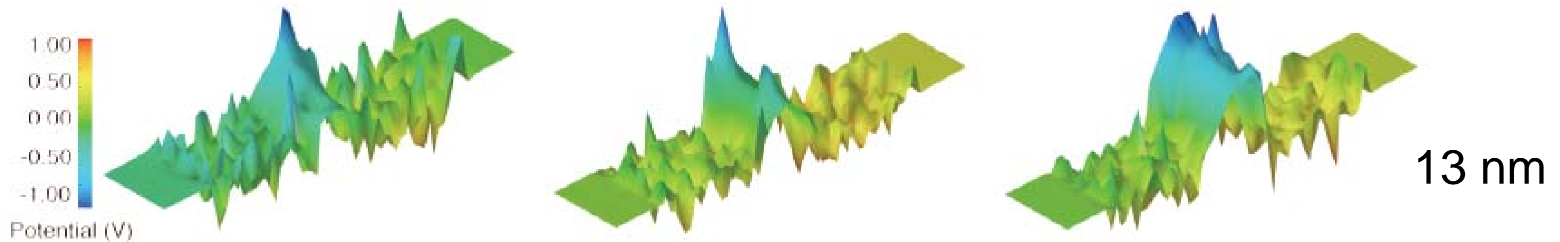
Simulation of 100000 statistical sample







Low V_T Medium V_T High V_T



Summary

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- Statistical compact models
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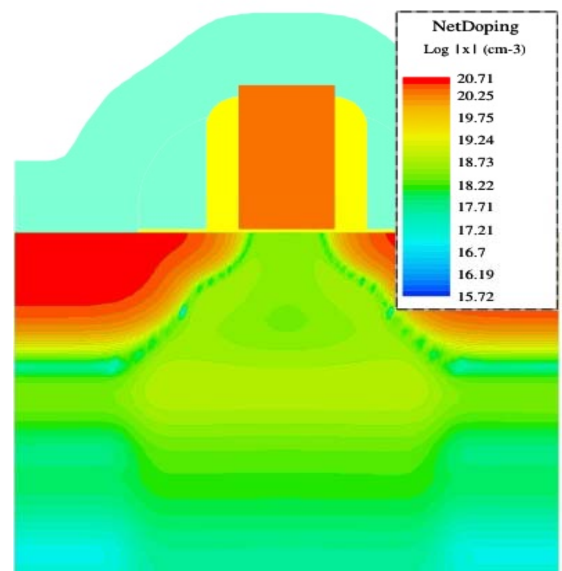
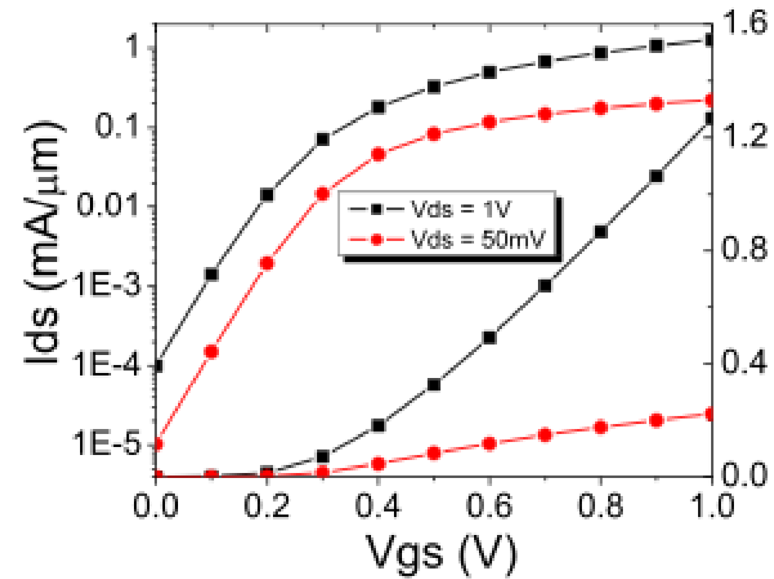
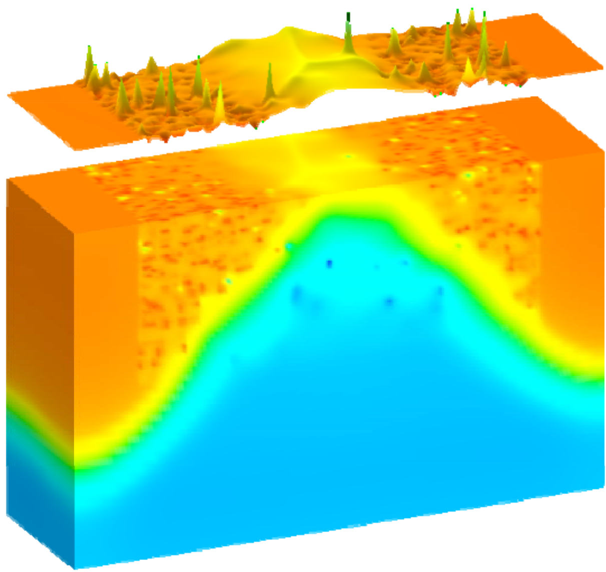
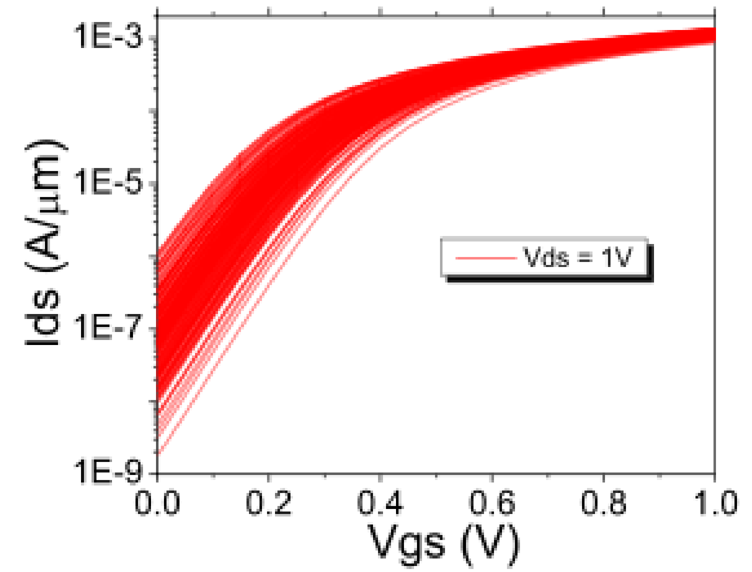
Test bed 35 nm MOSFET

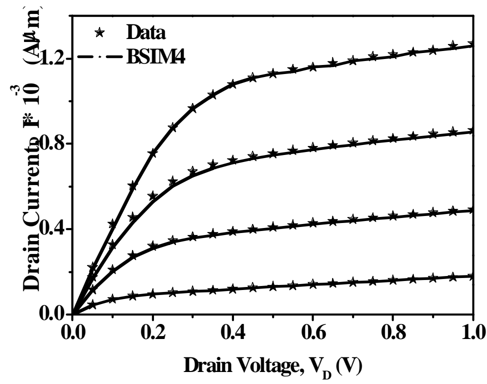


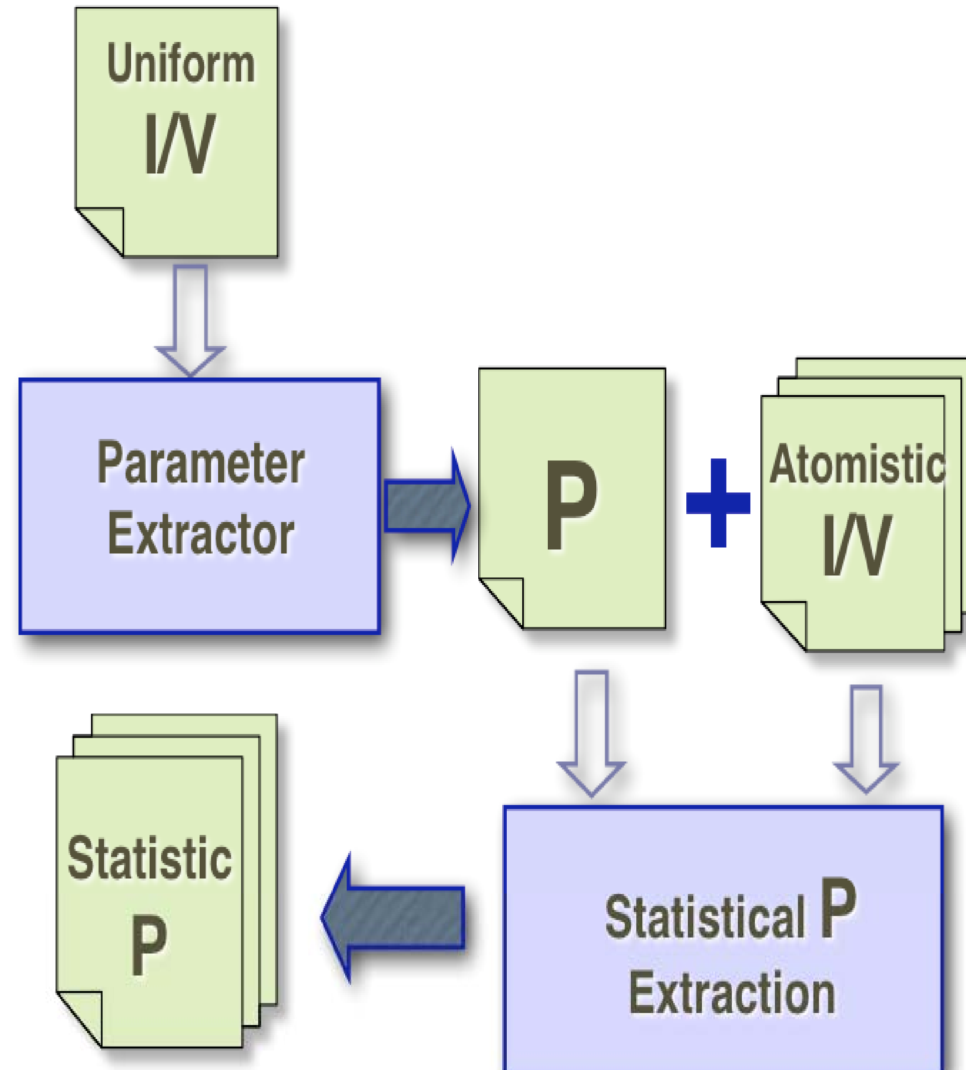


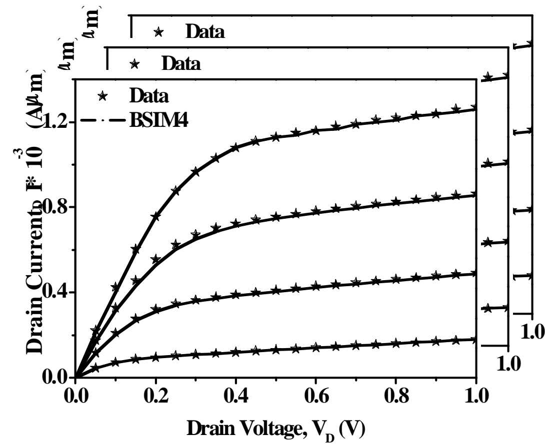




Two stage parameter extraction

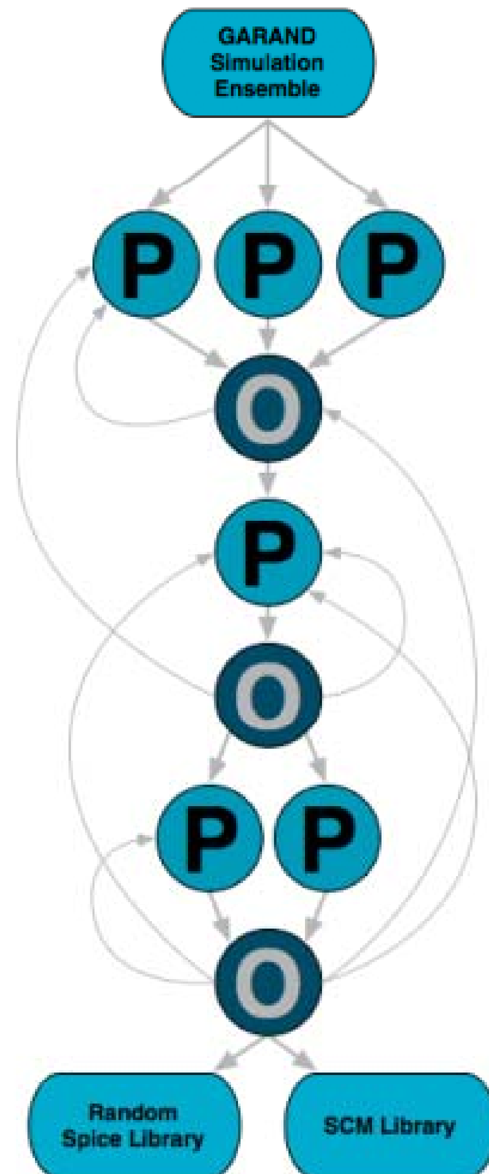






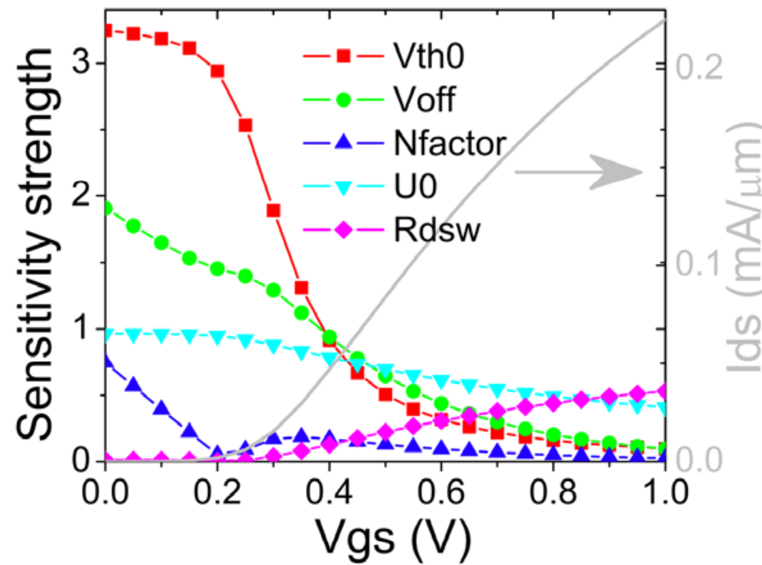
200 microscopically different transistors

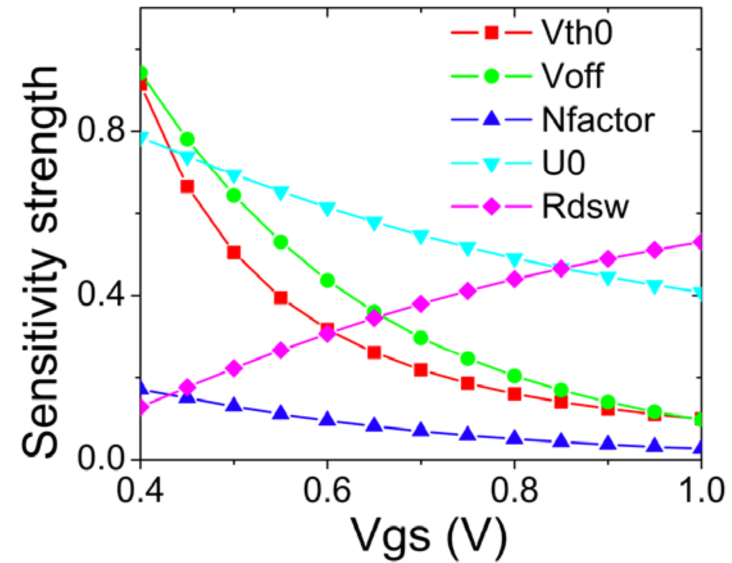
State machine extraction engine

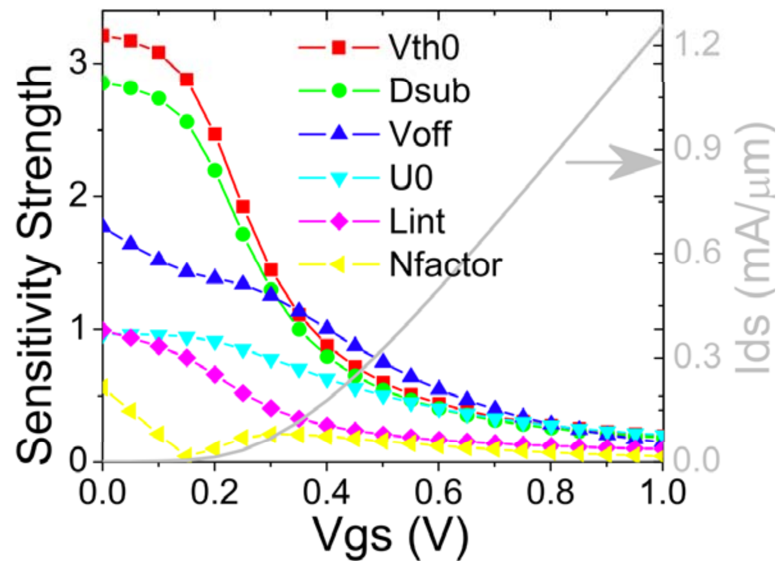


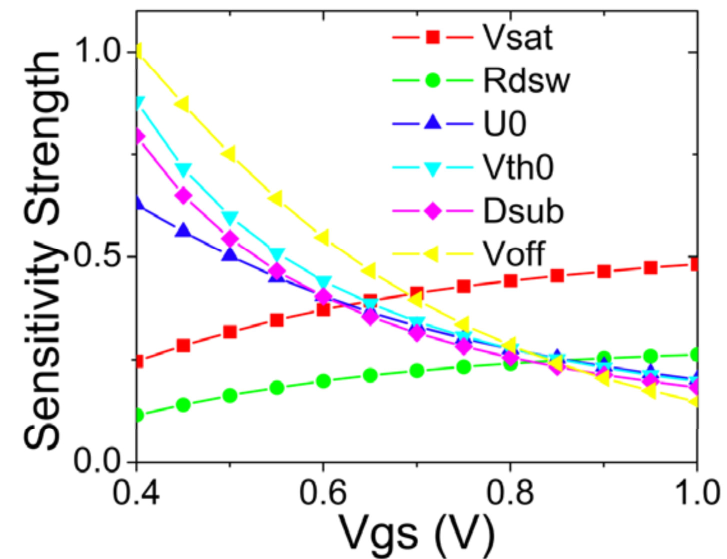
- Speed and flexibility
- Multiple back end simulators
- Multiparameter/multidevice optimisation
- Direct PCA extraction
- Direct NPM extraction
- Automated RandomSpice library
- Fully scriptable fitting strategy
- Parallel statistical fitting

Comprehensive sensitivity analysis

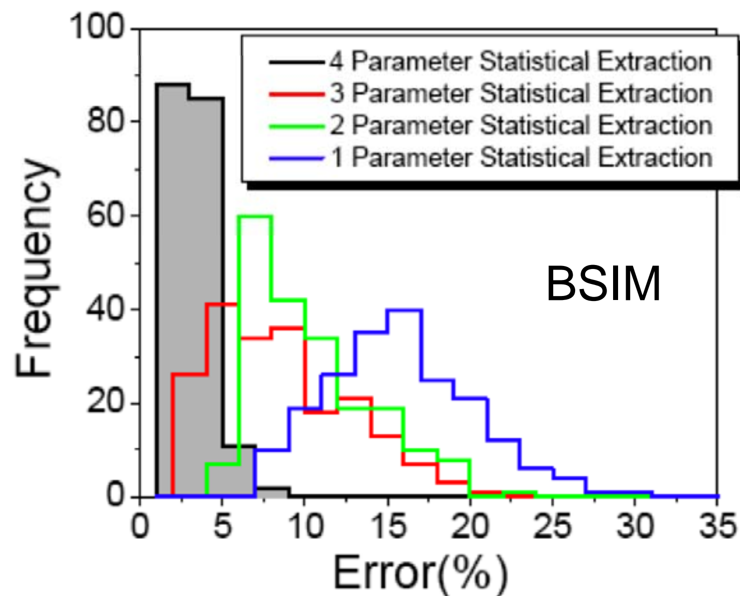


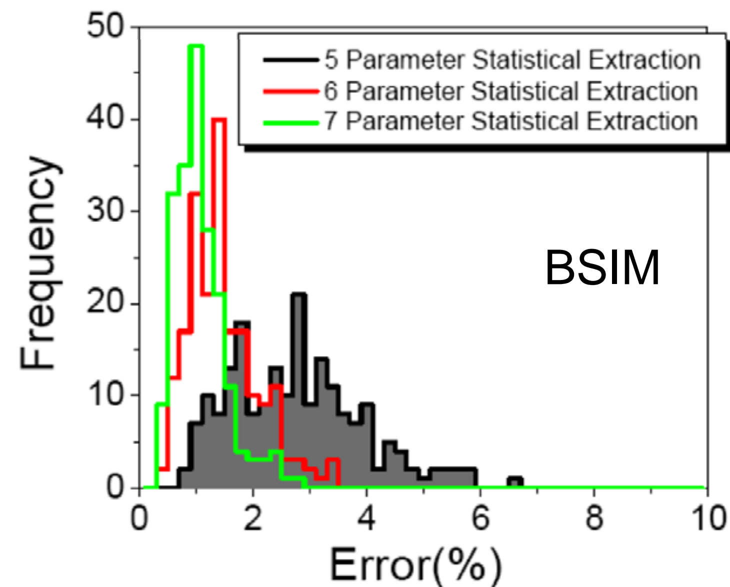


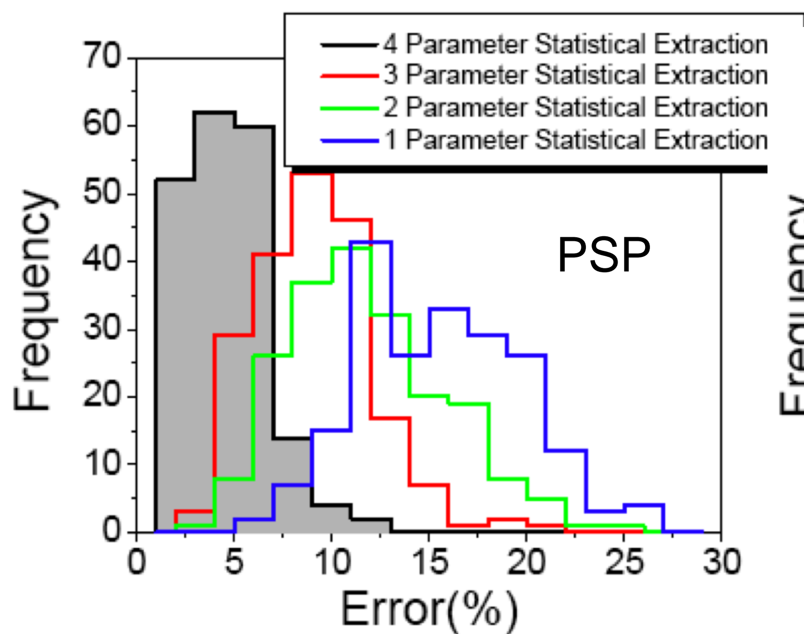


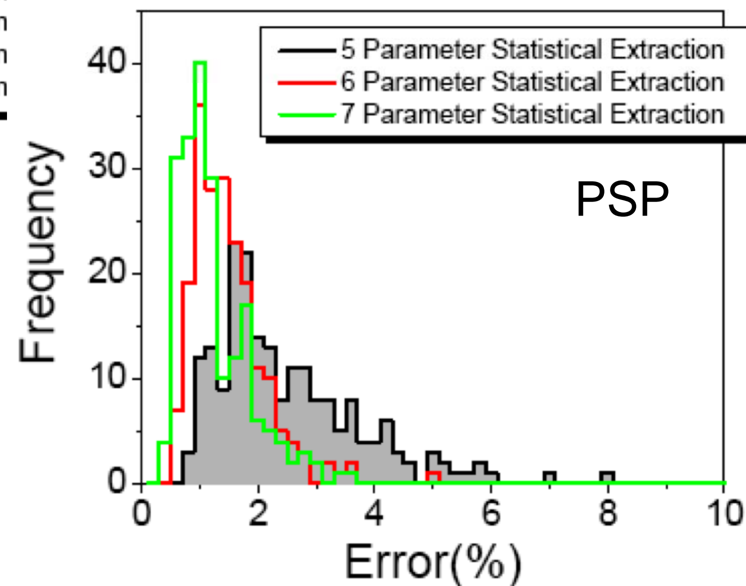


Parameter selection







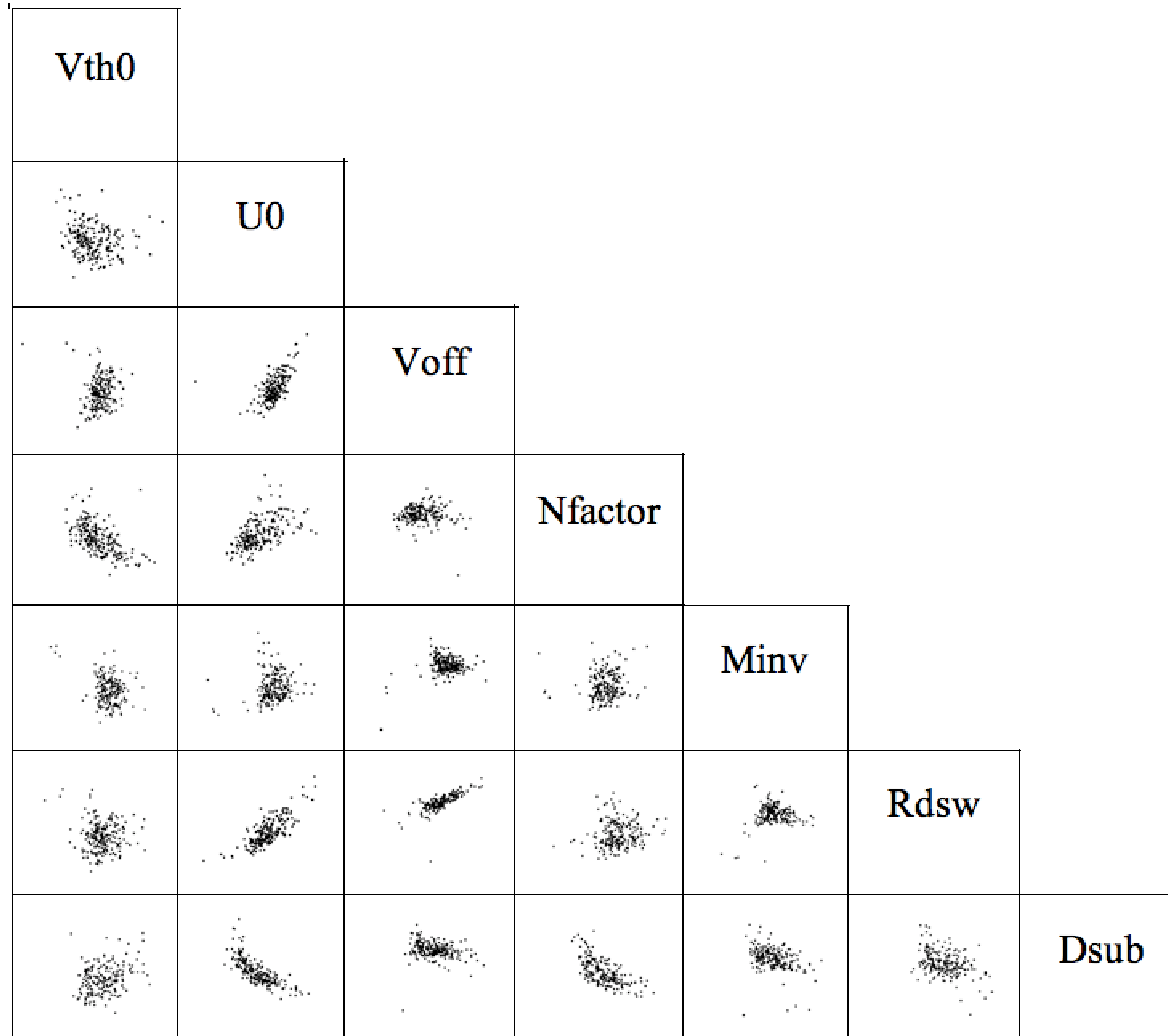


DEVICE MODELLING GROUP

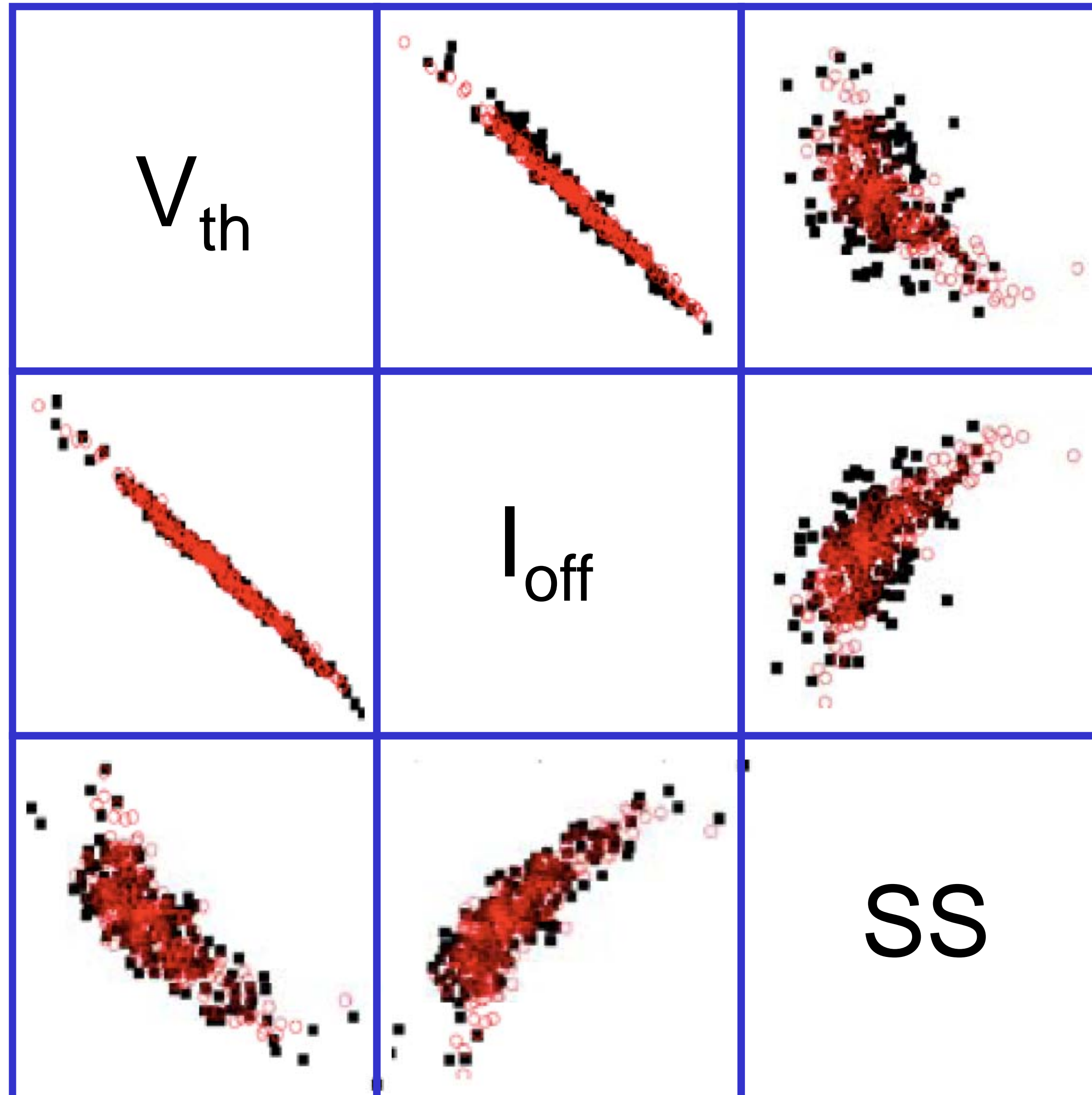
Statistical accuracy

V_{th}				
	I_{on}			
		I_{off}		
			DIBL	
				SS

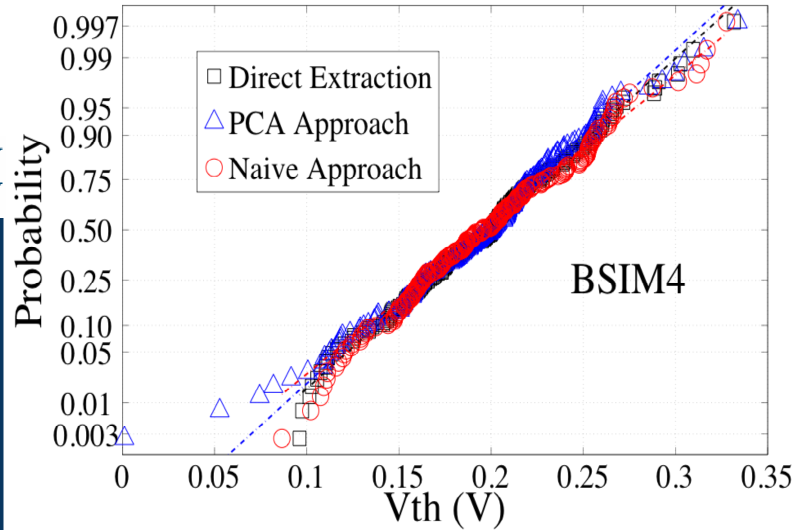
Statistical compact model parameter correlations

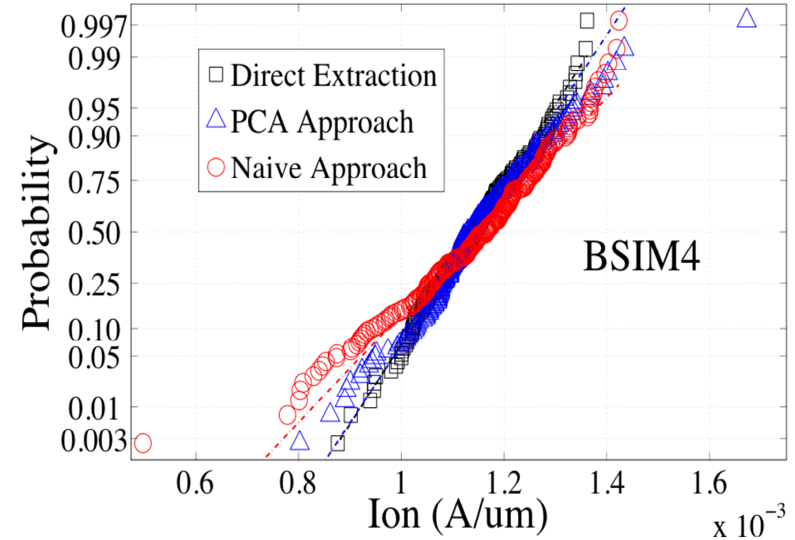


Naïve approach vs. PCA



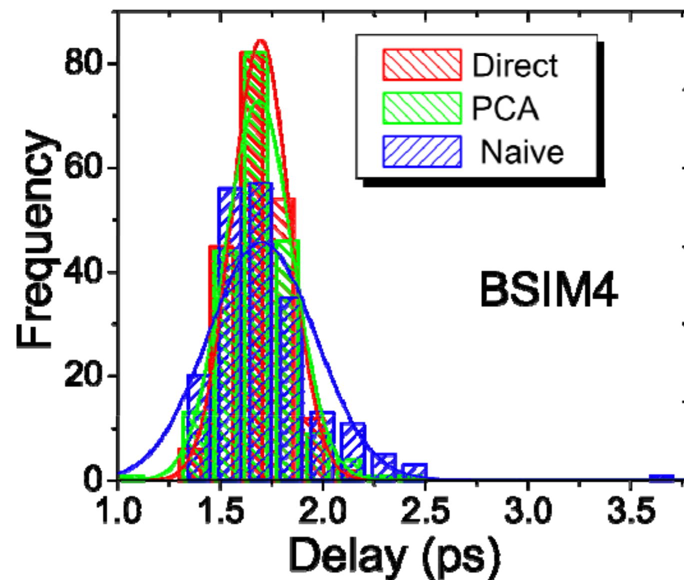
Naïve approach vs. PCA

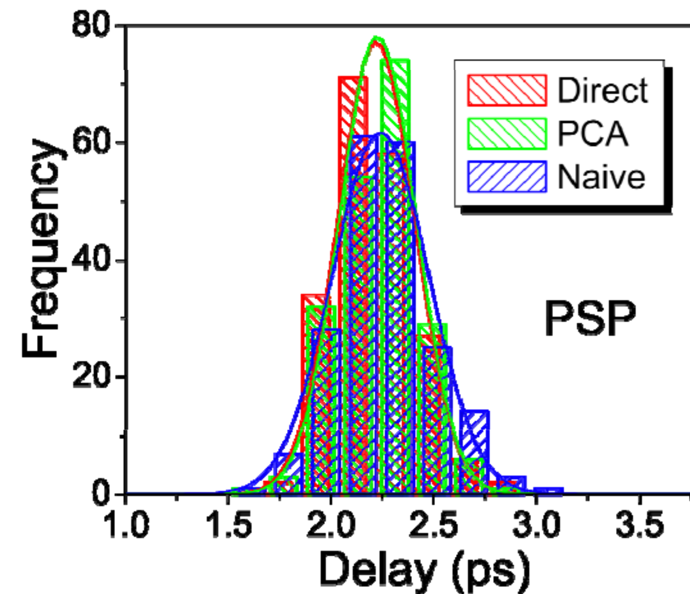




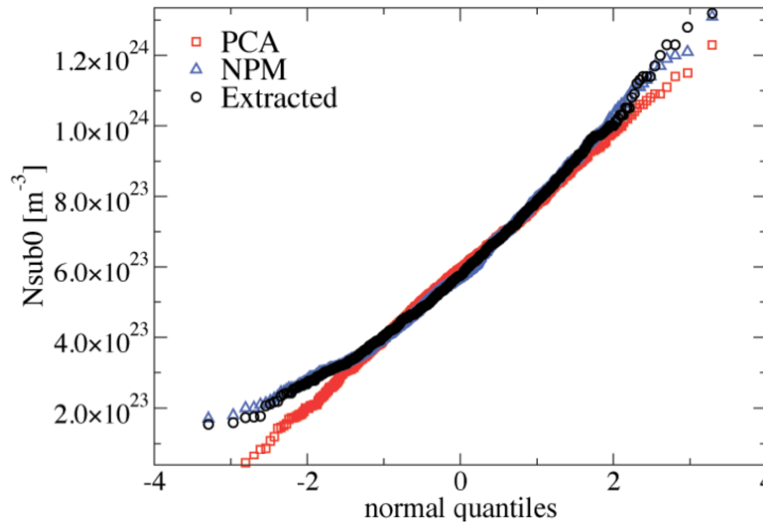
Naïve 85%, PCA 15%

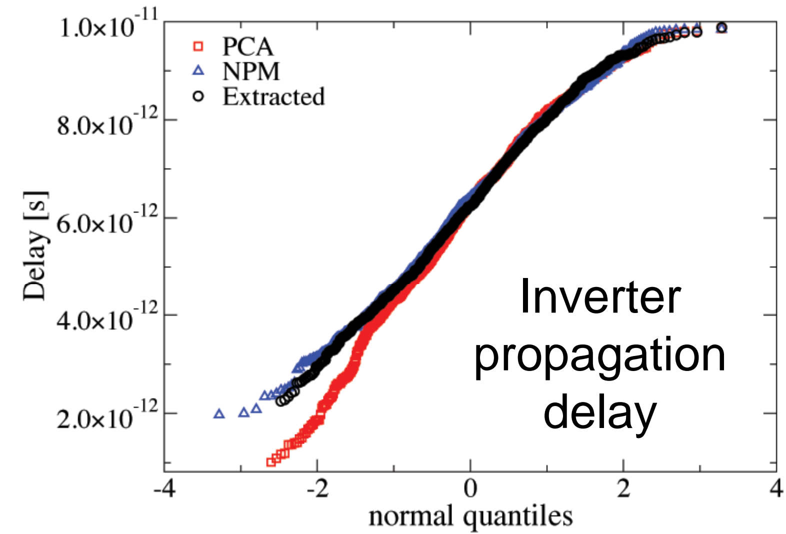
Naïve 25%, PCA 5%

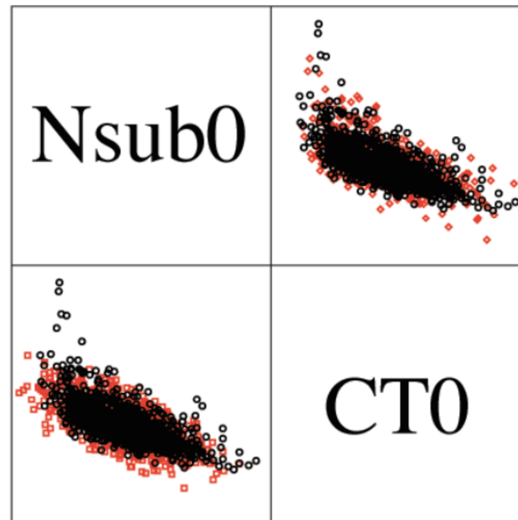


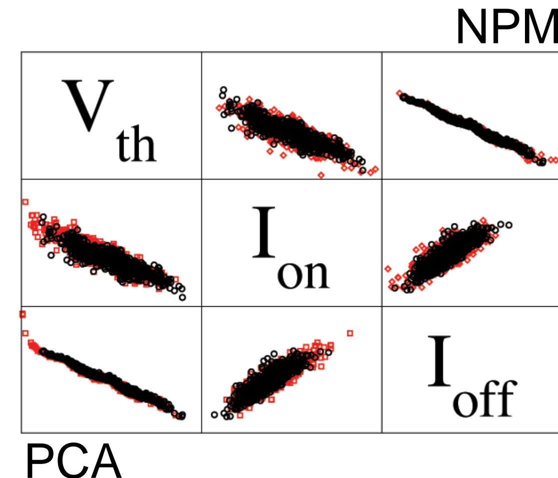


Statistical Nonlinear Power Method (NPM)









Summary

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- Statistical circuit simulation
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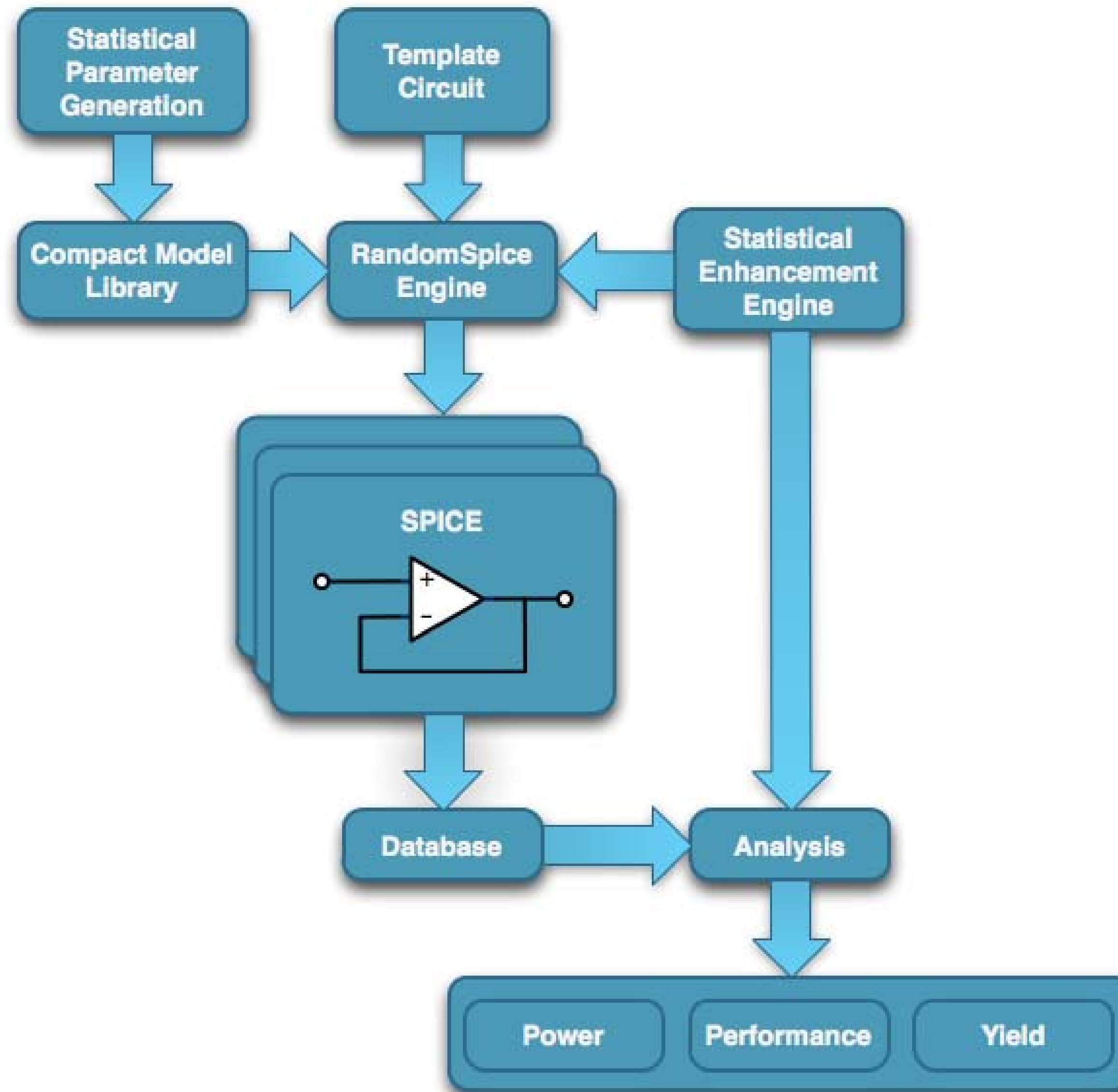
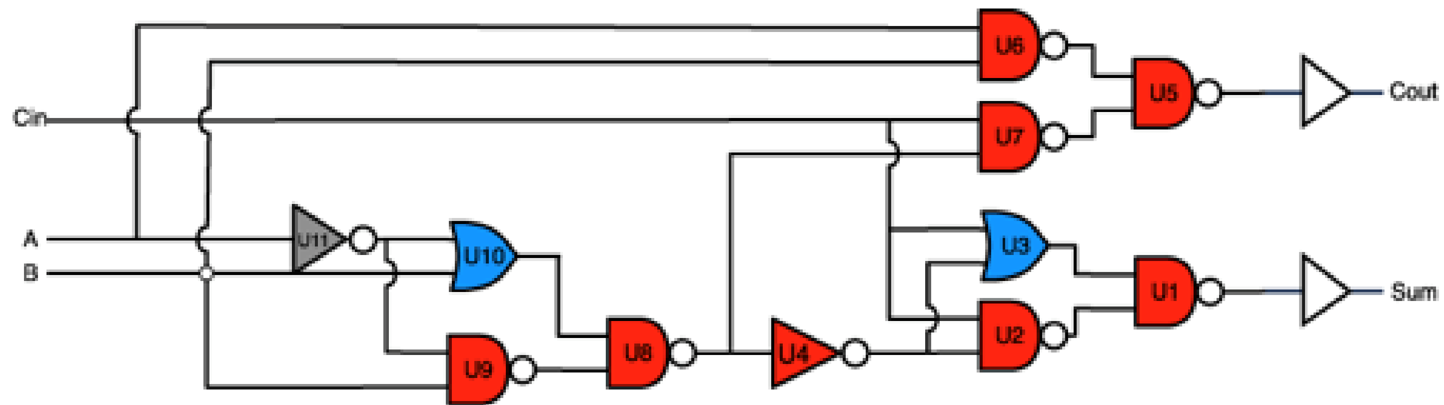
RandomSpice™

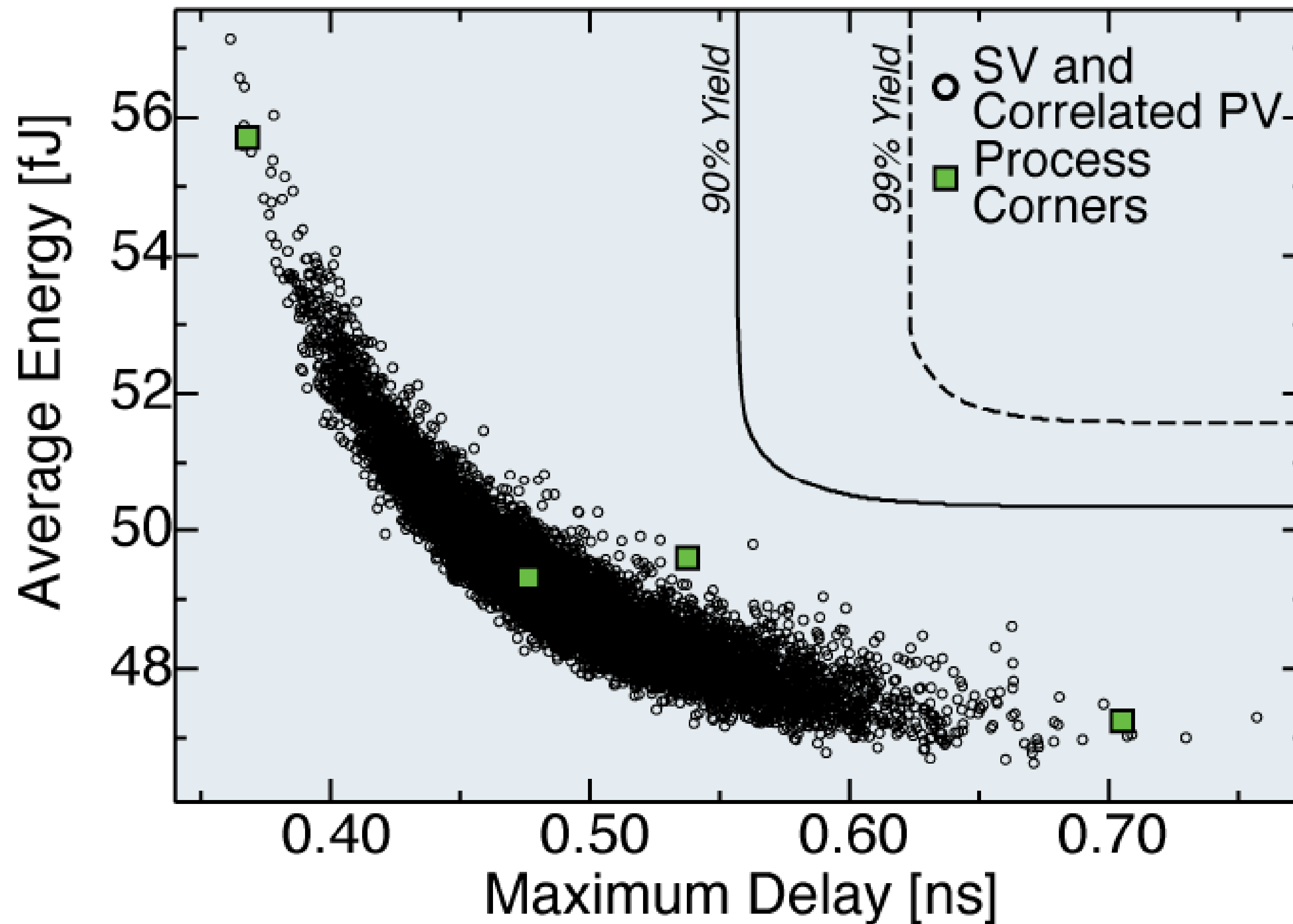


Simple adder example



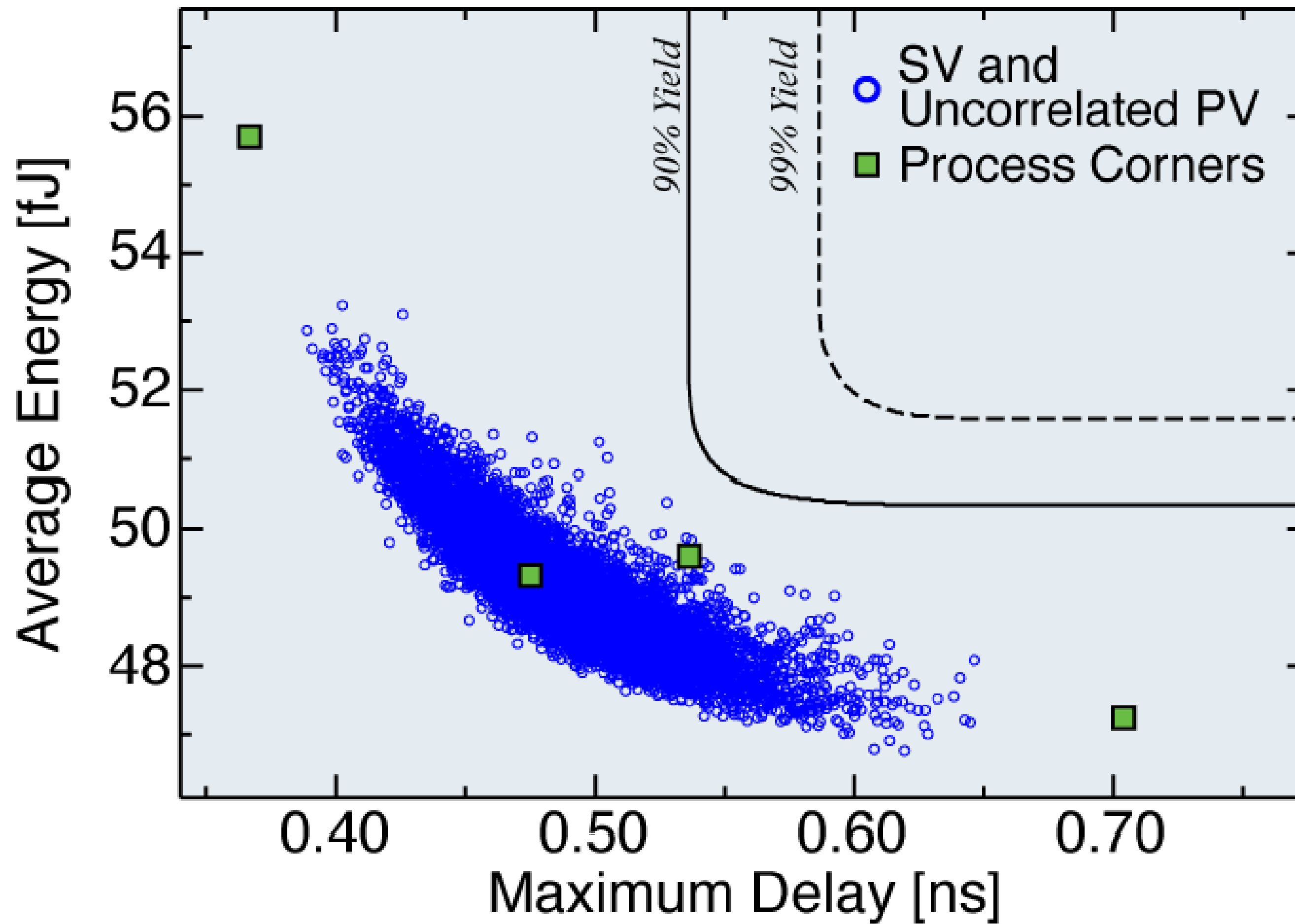
Representative for medium length critical path

Statistical vs. corner analysis



Correlated process variability + statistical variability

Statistical vs. corner analysis



Uncorrelated process variability + statistical variability

Statistical vs. corner analysis

90% Yield
99% Yield
Statistical Only
Process Corners
Average Energy [fJ]
56
54
52
50
48
0.40
0.50
0.60
0.70
Maximum Delay [ns]

Purely statistical variability

Statistical vs. corner analysis

90% Yield
99% Yield
Average Energy [fJ]
Maximum Delay [ns]
60
57
54
51
48
45
0.40
0.50
0.60
0.70
0.80
0.90

Correlated process variability +
3 level of statistical variability

Voltage scaling – yield prediction

Average Energy Per Transition [J]

70 f
65 f
60 f
55 f
50 f
45 f
40 f

400 p
600 p
800 p
1 n

Maximum Delay [s]

No Supply Scaling
AVS 4.2% [50mV]
AVS 8.4% [100mV]
AVS 12.6% [150mV]

90% Yield

95% Yield

Voltage scaling – yield prediction

Average Energy Per Transition [J]

70 f
65 f
60 f
55 f
50 f
45 f

400 p
600 p
800 p
1 n

Maximum Delay [s]

Summary

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- Conclusions

Conclusions

- Statistical variability has to be taken very seriously at 32 nm technology generation.
- Statistical reliability, enhanced by statistical variability is becoming an important issue.
- Statistical compact model techniques are necessary to support statistical design.
- Statistical circuit simulation will allow performance-power-yield tare off.

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