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Practical Process Variation Design Environments for Yield Maximization

James Victory, Juan Cordovez

Simulation and Characterization of Statistical CMOS Variability and Reliability Workshop
September 9, 2010

Outline

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1. Yield Impact on the Bottom Line
2. Overcoming Challenges Common to Statistical/Corner Models
3. Flexible Design Environments for Efficient Circuit Design
4. Split Lot Treatment: Design for Manufacturing Yield
5. Summary

Outline

A 65nm GPS SoC Case Study:
Yield Improvement Impact on Bottom Line

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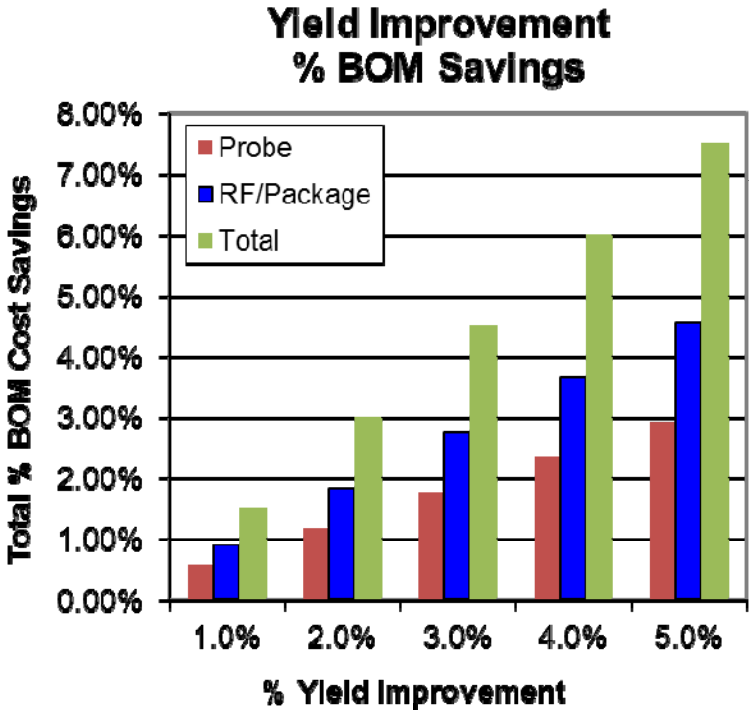
Lost Yield Impact on BOM = Lower GDPW + Higher Test Costs + Higher Package Costs

compounding yield loss effects

BOM Cost Analysis	
Die W (mm)	4.4
Die H (mm)	4.4
mm2 Die Area Total	19.36
Gross Die/Wafer (300 mm)	3358
Estimated Die Cost	$0.74
Fab Process Yield	95%
Probe Yield	**85%**
Probe Cost (2s @7c)	$0.14
Probe Yield Cost	$0.21
Package Cost	$0.40
RF Yield	**85%**
Mechanical Yield	99%
Final RF Test Cost (3s @5c)	$0.15
RF Yield Cost	$0.27
Baseband Yield	95%
Final BB Test Cost (2s @6c)	$0.12
BB Yield Cost	$0.10
Bake, Pack, Ship	$0.06
Parts Shipped per wafer	2146
Total Device Cost	$2.19



Small Yield Improvement Generates Large** Cost Savings

**Highly dependent on application and market

Goal of Yield Maximization: Reduce Over and Under Design

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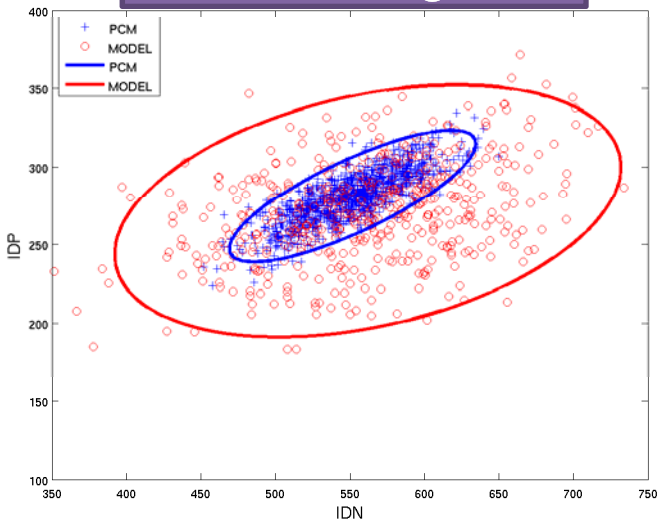
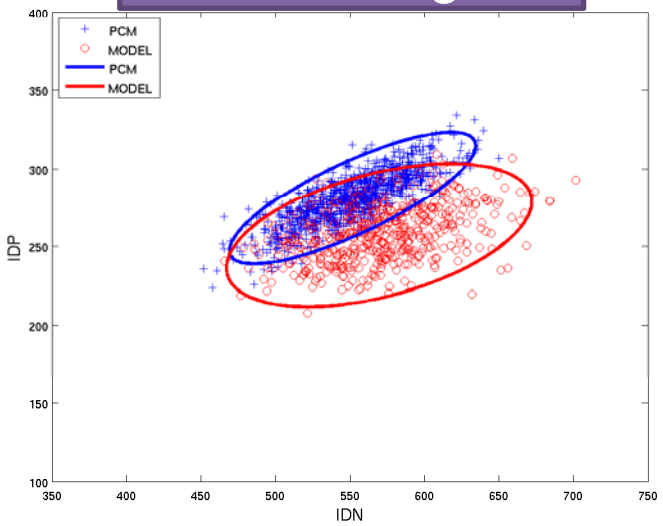
Over design



Under design



Model overestimates process variation and fails to capture inter-device correlations

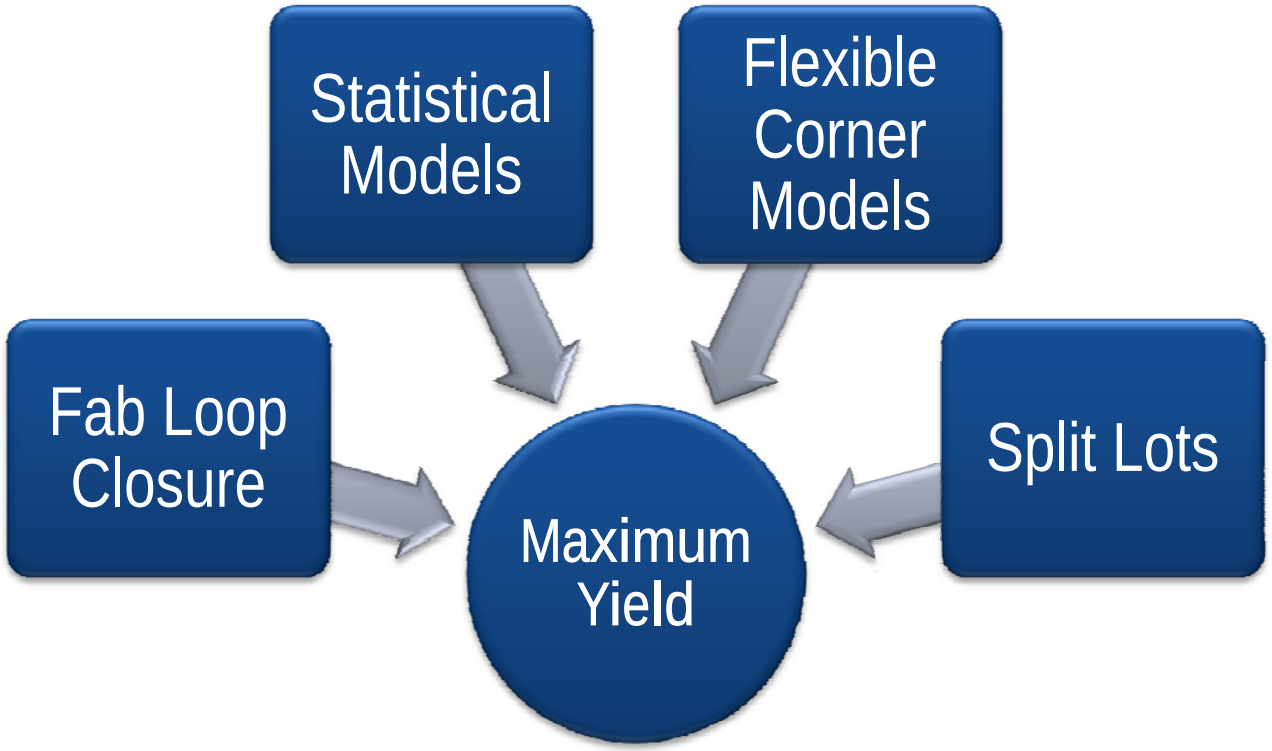
- Designers struggle to meet specification compliance, increasing development cycle times
- Designers resort to inefficient methods to compensate variation, derating specs, increasing die size, etc...
- Suboptimal mass production device performance

Model is offset from fab specification means, distributions, & correlations

- Designers unable to simulate actual fab performance, collapsing yield and reliability.
- Nonfunctional Silicon
- Delays in product readiness
- Suboptimal mass production device performance

Comprehensive Yield Maximization

Requires More than Conventional Corner and Statistical Models



Pillars of Design for Yield Maximization

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Accurate

- Deploy physical extraction techniques such as BPV, and capture correlation
- Statistical process control data interrogation, understand limitations
- Deploy Fab loop closure to eliminate over and under design

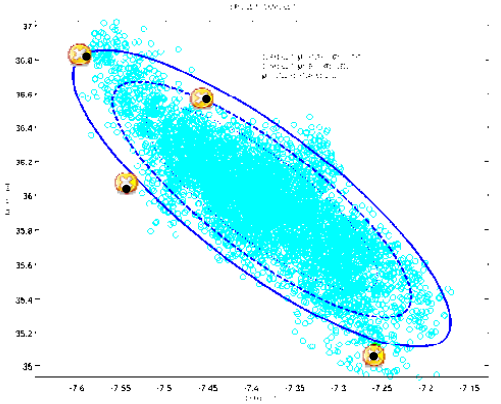
$$\sigma^2_{\delta EGi} = \sum_k \left(\frac{\partial EGi}{\partial PGk} \right)^2 \sigma^2_{\delta PGk}$$

Flexible

- More than just worst case corners which limit exploration of entire process variation space
- More than just Monte Carlo which is an expensive way to find root causes of design sensitivity
- Give the designer the power to explore the entire process variation space, effeciently

Accessible

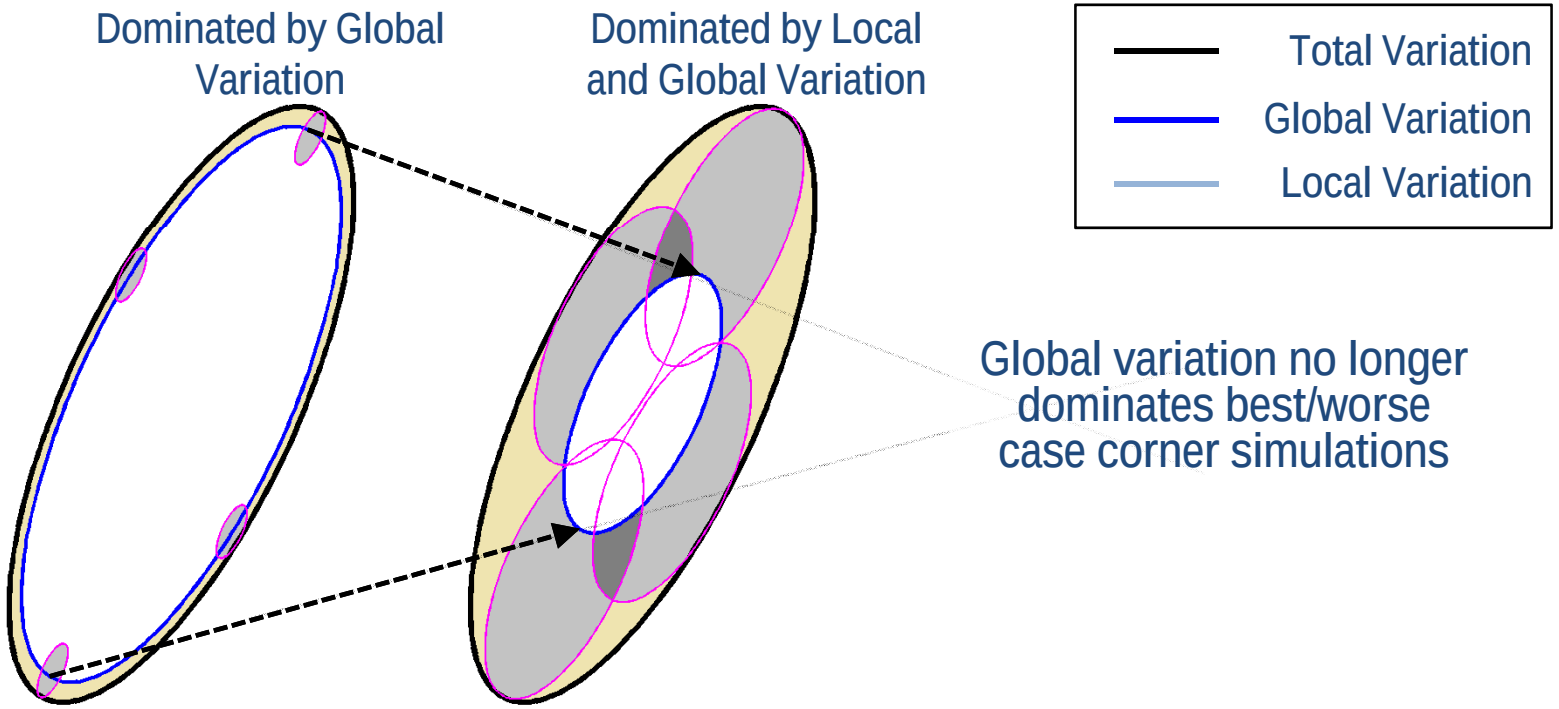
- Designer intuitive implementation in PDK environments
- Direct links to fab data for real time tracking
- Relevant to all designs including RF, analog, power



Outline

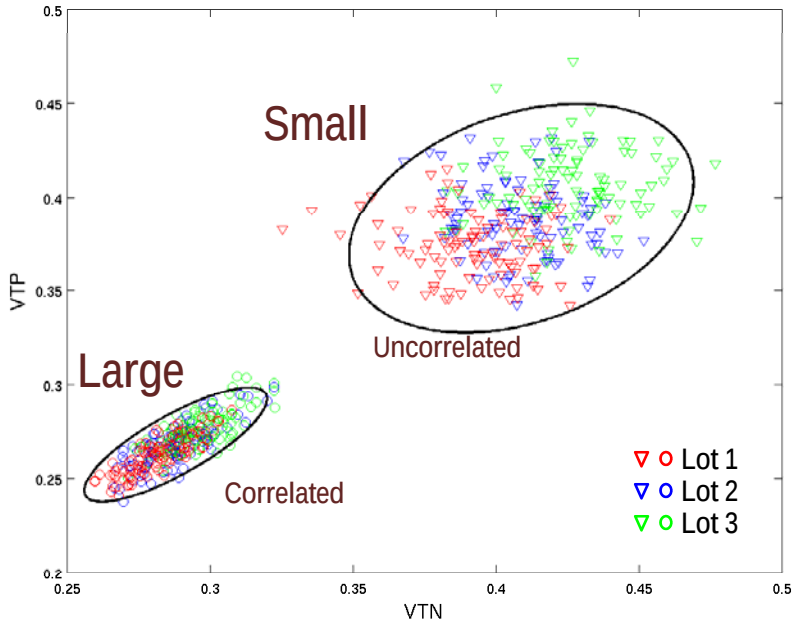
Local and Global PCM Variation: The Nanoscale Challenge

- PCM data is no longer dominated by global *correlated* variation.
- Large local uncorrelated variation is apparent in PCM data in particular for minimum geometries (effects are graded over the geometry range).
- Model extraction based on PCM is complicated by presence of correlated and uncorrelated effects for the same physical parameter.



Local and Global PCM Variation: How to Capture in Models

- Statistical model generation requires 3 step process
  1. Extract local mismatch variation (PL) using BPV from conventional mismatch data (EL)
  2. Substract local variation from total PCM variation (EG)
  3. Extract global variation (PG)



Local Mismatch

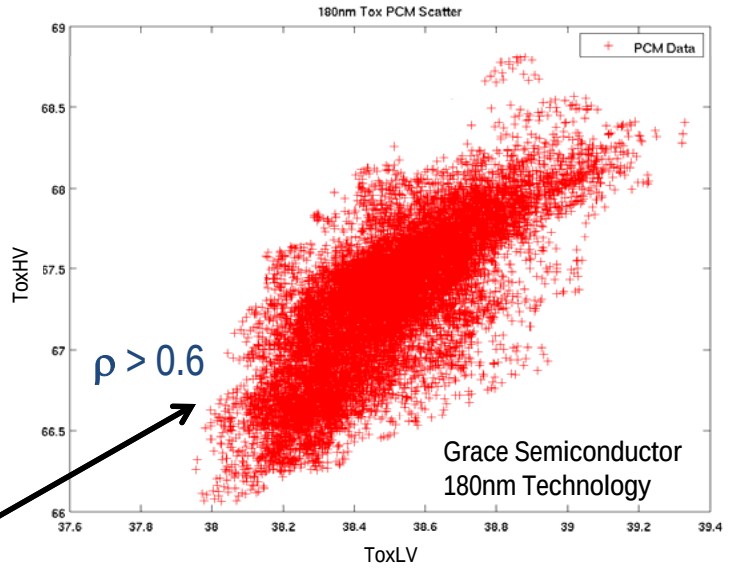
$$\sigma^2_{\delta ELi} = \sum_k \left(\frac{\partial ELi}{\partial PLk} \right)^2 \sigma^2_{\delta PLk}$$

Global

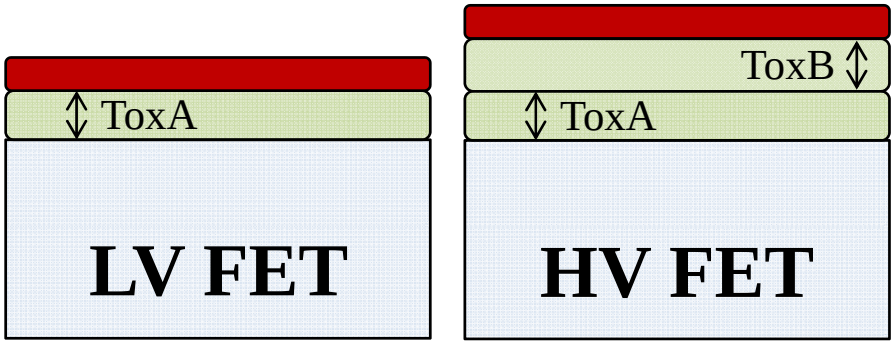
$$\sigma^2_{\delta EGi} - \sigma^2_{\delta PL} = \sum_k \left(\frac{\partial EGi}{\partial PGk} \right)^2 \sigma^2_{\delta PGk}$$

Overlooked/Hidden Correlations: Tox Case Study

- Process variation induces electrical performance correlation across multiple device types
- Certain correlations are often over looked in models such as thin and thick gate oxide, salicide, ILD, and others.
- Accurate modeling achieved through isolation of root uncorrelated physical parameters and mapping into affected device models



Largely Uncorrelated Process Parameters
ToxA and ToxB
ToxA Induces LV and HV FET Tox Correlation



$$\sigma^2_{ToxA} = \sigma^2_{ToxLVpcm}$$

$$\sigma^2_{ToxA} + \sigma^2_{ToxB} = \sigma^2_{ToxHVpcm}$$

$$\sigma^2_{ToxB} = \sigma^2_{ToxHVpcm} - \sigma^2_{ToxA}$$

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3 **Flexible Design Environments for Efficient Circuit Design**

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Fab Loop Closure

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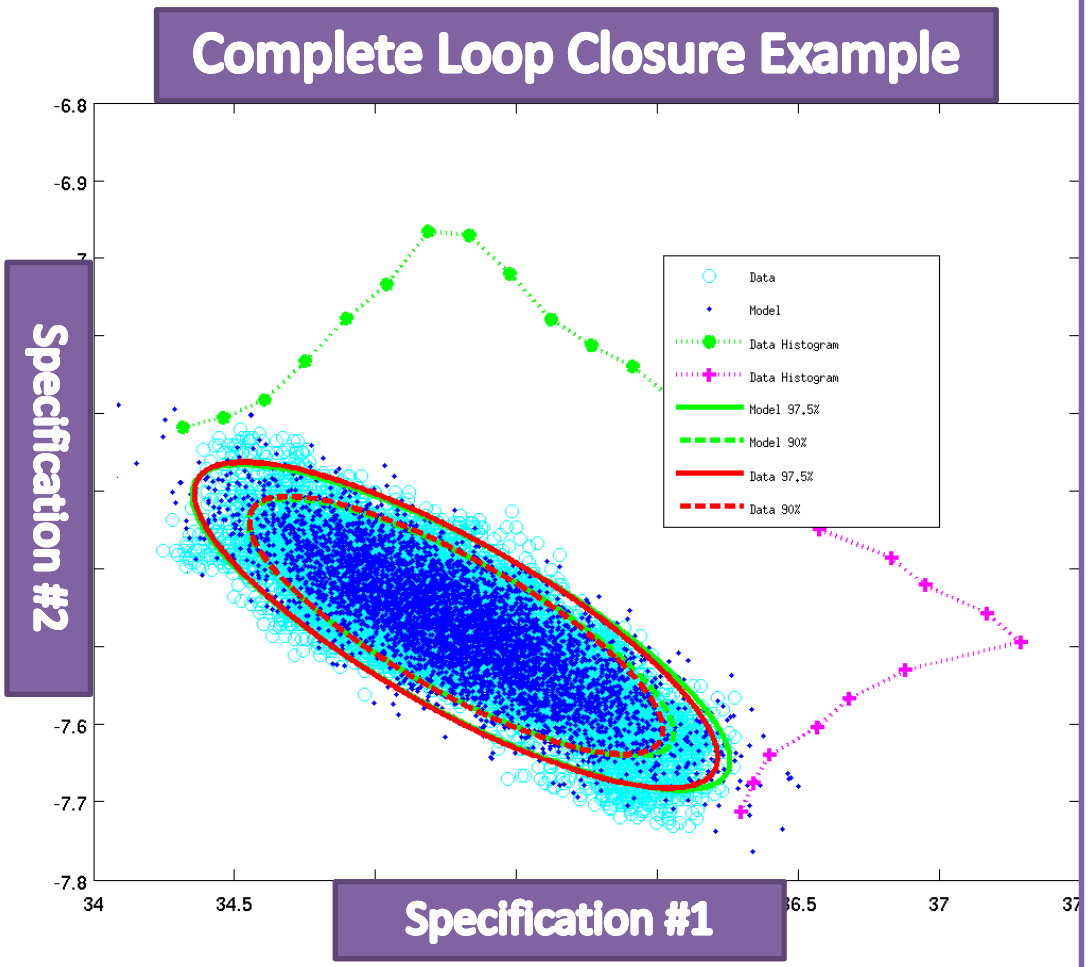
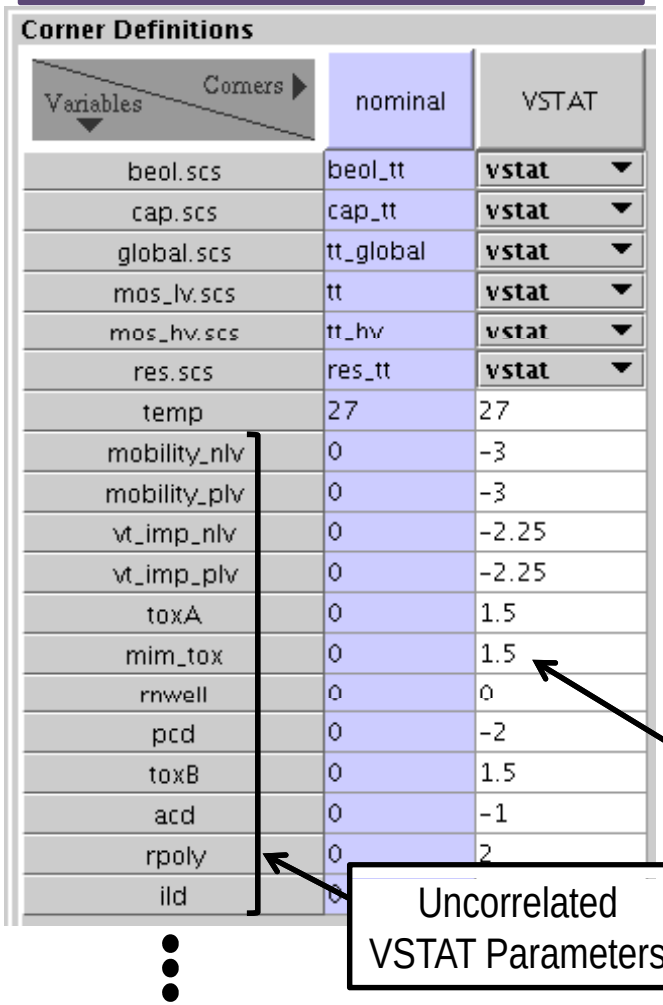


What is Fab Loop Closure?

- Critical component of statistical model generation
- Methodology to guarantee fab to model alignment of means, σ, and correlation across specifications
- Identifies device correlation induced by shared process parameters and subsequent effects on electrical performance
- Hidden inter and intra device correlations accurately captured
- Critical protection against fab to model performance drifts over time
- Minimizes wasteful over design and under design
- Deployed as automated web system

Flexibly Explore Process Variation Space: Sentinel VSTAT Simulation Environment

VSTAT GUI Example



- User defined parameter modulations
- Available as design environment variables for parametric sweeping

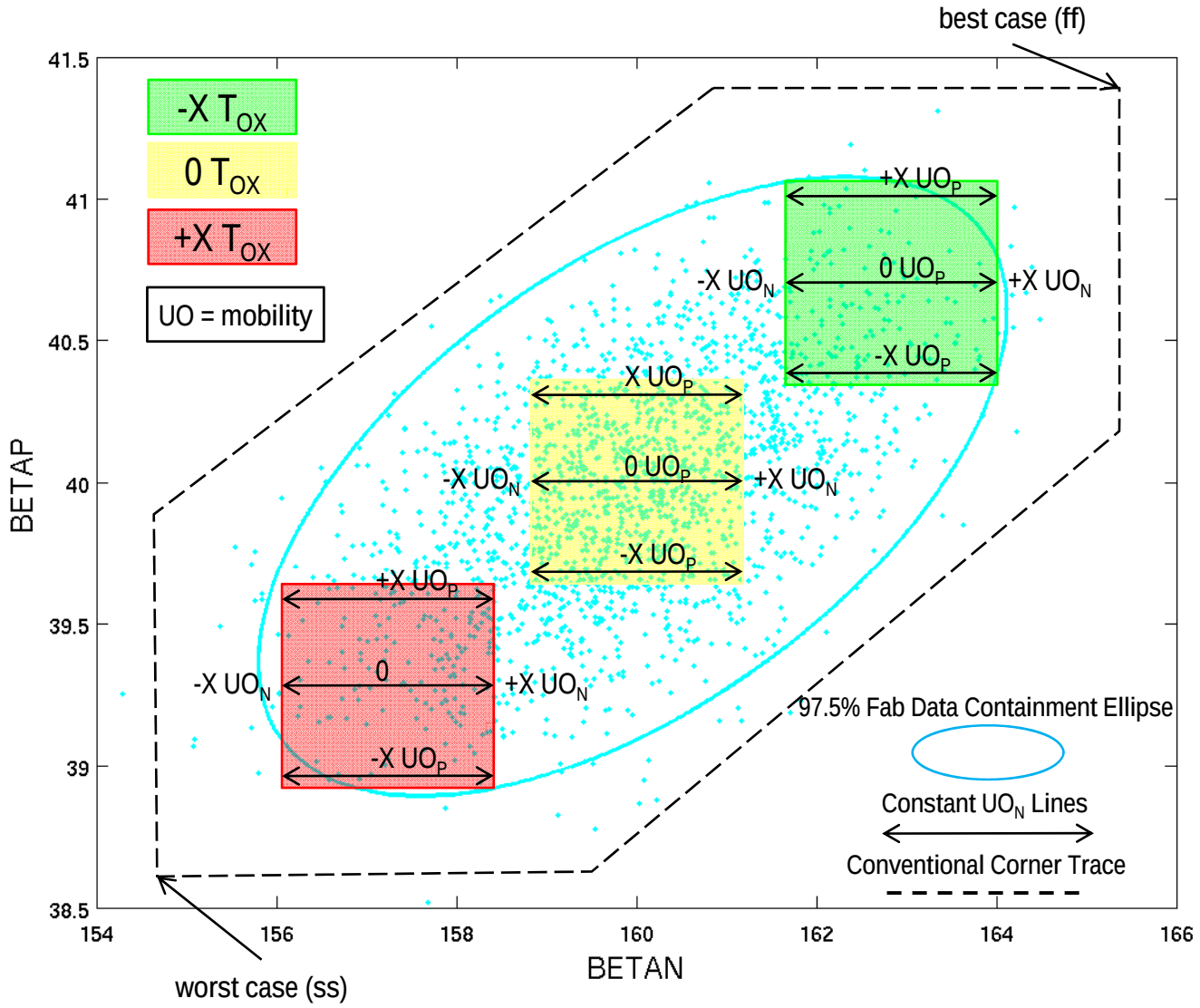
What is VSTAT?

- A flexible corner model environment that enables parametric modulation of critical uncorrelated process parameters continuously and independently

Why is VSTAT beneficial?

- Removes barriers presented by fixed corners and monte carlo statistical models.
- Empowers designers to flexibly and efficiently explore circuit sensitivities across the entire process variation space.

Flexibly Explore Process Variation Space: VSTAT Example



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Overcoming SPLIT Lot Limitations: Sentinel VirtuaLOT*

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SPLIT Lots

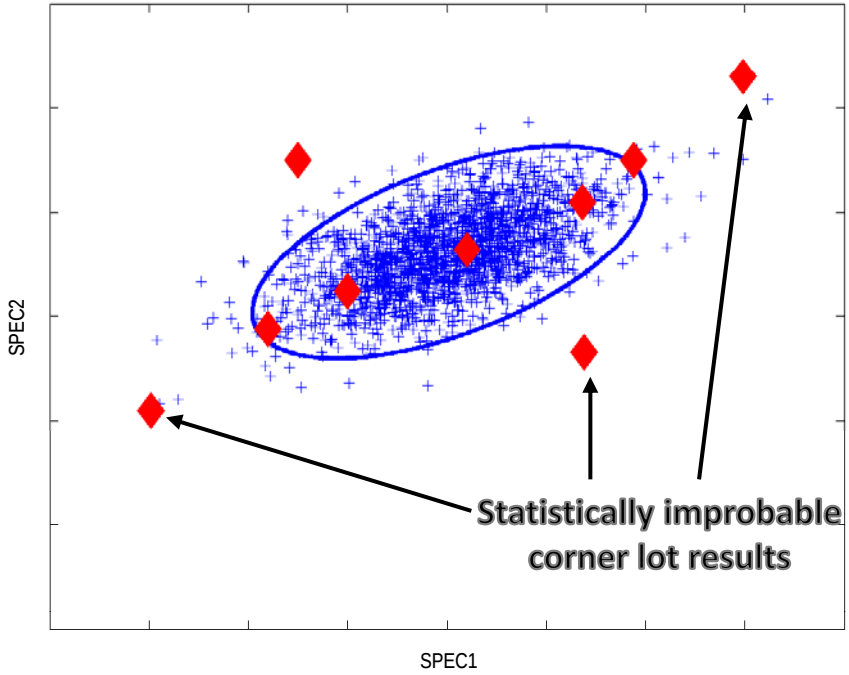
- Impose fixed process variation to test design robustness to process variation
- All conditions realistically cannot be explored.
- Conditions produce silicon with statistically improbable results, forcing designers to waste time and design performance to "comply".

VirtuaLOT

- Pre-fabrication simulation of SPLIT Lots
- Provides insight into circuit sensitivities to determine priority split conditions
- Reduces fabrication of statistically improbable silicon split lots

	Split Parameters (SP)																	
	Gate Oxide Thickness (TOX)			Poly Silicon Critical Dimension (CD_{poly})			Active Area Critical Dimension (CD_{AA})			N-type Implant MOSFET Doping (N_{NFET})			P-type Implant MOSFET Doping (N_{PFET})			Poly Silicon Doping (N_{poly})		
	Split Parameter Levels (SP)																	
	H	N	L	H	N	L	H	N	L	H	N	L	H	N	L	H	N	L
Split 1		x			x			x			x			x			x	
Split 2			x			x			x			x			x			x
Split 3	x			x			x			x			x			x		
Split 4	x			x					x			x			x			x
Split 5			x		x		x			x			x			x		

N^{SP} produces 729 SPLITs!



*Patent Pending

VirtualLOT
PDK/Model Implementation

VirtuaLOT GUI Example

Sentinel VirtuaLOT: Corner Lot Split Conditions

Process Module	Split Condition	Selection
Active	With Dummy Fill	○
	Without Dummy Fill	◉
Gate Oxide	POR +1%	○
	POR	◉
	POR -1%	○
PCH3 Vt	POR +6%	○
	POR	◉
	POR -6%	○
PCH Vt	POR +6%	○
	POR	◉
	POR -6%	○
NCH3 Vt	POR +6%	○
	POR	◉
	POR -6%	○
NCH Vt	POR +6%	○
	POR	◉
	POR -6%	○
Poly CD	POR -0.01um (F)	○
	POR (N)	◉
	POR +0.01um (S)	○

POR: Process of Record

Generate VirtuaLOT Models

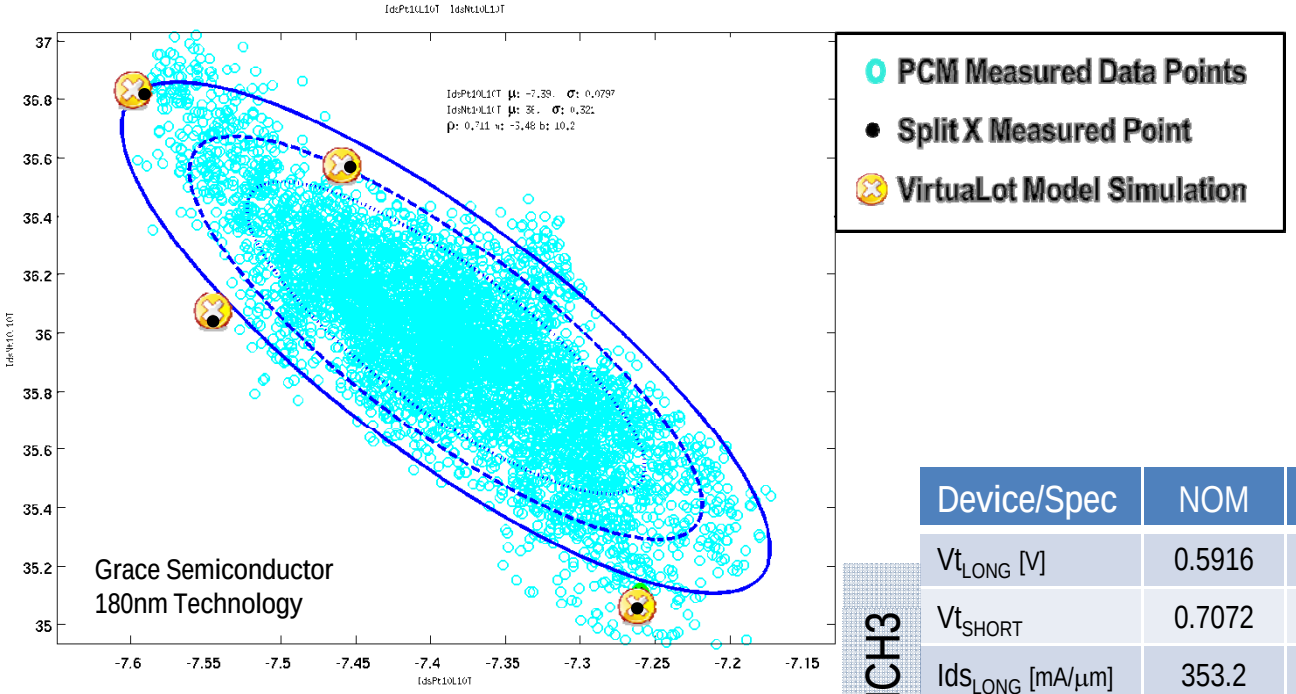
Map into
Process Parameters

```
section VLOT_DELTAS_SPLIT_1

Parameters
VLOT_Dnpoly=-0.15
VLOT_Dcd_poly=3.3e-9
VLOT_Dsti=-0.13e-7
VLOT_Dtox=-1.5e-10
VLOT_Dcdaa=-1.1e-9
VLOT_Dnnfet=-0.12
VLOT_Dppfet=-0.12

endsectionVLOT_DELTAS_SPLIT_1
```

Map into
Model Equations

```
subckt poly_resistor (P N G) parameters L=10u W=2u
+ tpoly=0.5e-6
+ npoly=1.65e19
+ rend=0.3
+ rho_poly=1/(Q*tpoly*upoly*npoly(1+VLOT_Dnpoly))
+ dw_poly=-1*(cd_poly+VLOT_Dcd_poly)
+ Rpoly=rho_poly*L/(W-dw_poly)*rend/(W-dw_poly)

R1 (P N) resistor r=Rpoly tc1=tc1_poly tc2=tc2_poly
ends poly_resistor
```

VirtualLOT Silicon Validation



	Device/Spec	NOM	WAT	VLOT	Error [%]
NCH3	Vt_{LONG} [V]	0.5916	0.7000	0.7000	0.000
	Vt_{SHORT}	0.7072	0.7180	0.7177	0.046
	Ids_{LONG} [mA/µm]	353.2	351.2	351.1	0.003
	Ids_{SHORT}	591.6	586.1	586.2	0.024
PCH3	Vt_{LONG}	-0.7420	-0.7500	-0.7500	0.000
	Vt_{SHORT}	-0.6759	-0.6880	-0.6879	-0.013
	Ids_{LONG}	-738.6	-726.0	-726.1	-0.005
	Ids_{SHORT}	-293.6	-282.0	-282.2	0.110

Summary

- Understanding improved yield impact on the bottom line, over and under design concepts sheds light on the real prize
- Maximizing yield requires more than just fixed corner and Monte Carlo statistical models which may present barriers to understanding design sensitivity to process variation
- Designers need flexible statistical design platforms that allow them to efficiently design for circuit sensitivity to process variation
- Advanced platforms like VSTAT and VirtuaLOT achieve this goal

Acknowledgments

Grace Semiconductor

Providing portions of statistical data in presentation where noted

Colin McAndrew, Freescale Semiconductor

Discussions on Statistical Modeling Techniques

References:

C.C. McAndrew, “Statistical Modeling for Circuit Simulation”, Proceedings of the Fourth International Symposium on Quality Electronic Design (ISQED’03)

C.C. McAndrew and Patrick Drenann, “Device Correlation: Modeling using Uncorrelated Parameters, Characterization Using Ratios and Differences”, Proc. Workshop on Compact Modeling WCM, 2006

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