Workshop on
Simulation and Characterization of Statistical CMOS
Variability and Reliability

9. September, 2010, Bologna

Compact Modeling of the MOSFET Performance Distribution for Statistical Circuit Simulation

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About Compact Models

Device Characteristics ⟷ **Compact Model** ⟷ Circuit Simulation

- Analytical Equations
- Parameter Extraction

Variation of Circuit Performances

- Single Transistor Variations ←
- Layout Dependent Variations
- Interconnect Variations

Goal of Compact Models

predict statistical variation of circuit performances
without statistical investigations

Contents

1. Compact MOSFET Modeling: HiSIM

2. Variation Extraction
   - DC measurements (inter-chip variation)
   - basic analog circuits (intra-chip variation)

3. Methodology Incorporating Circuit Simulation

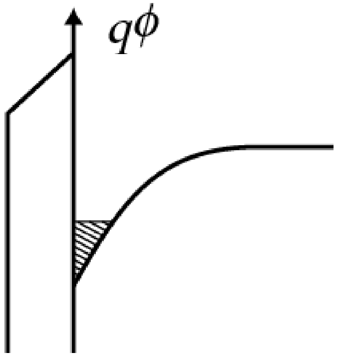
Basic Device Equations

-Poisson:

$$\nabla^2\phi = -\frac{q}{\varepsilon_{\mathrm{Si}}}(N_{\mathrm{D}}-N_{\mathrm{A}}+p-n)$$

$$n = n_{\mathrm{i}}\exp\frac{q(\phi-\phi_{\mathrm{n}})}{kT}$$

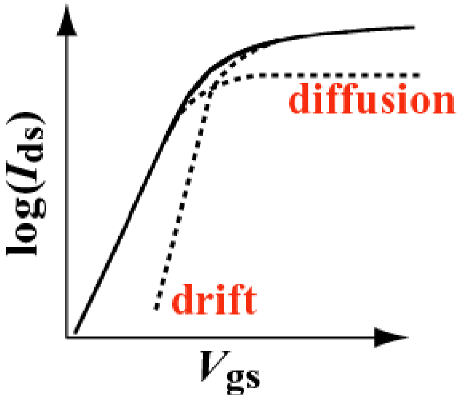
$$p = n_{\mathrm{i}}\exp\frac{q(\phi_{\mathrm{p}}-\phi)}{kT}$$



-Current Density:

$$j_{\mathrm{n}} = q\mu_{\mathrm{n}}n\frac{\phi}{y} + qD_{\mathrm{n}}\nabla n$$

$$j_{\mathrm{p}} = q\mu_{\mathrm{p}}p\frac{\phi}{y} - qD_{\mathrm{p}}\nabla p$$



-Continuity: $I(\mathrm{t}) = I_0(\mathrm{t}) + \frac{\mathrm{d}Q}{\mathrm{d}t}$

(solved by circuit simulator)

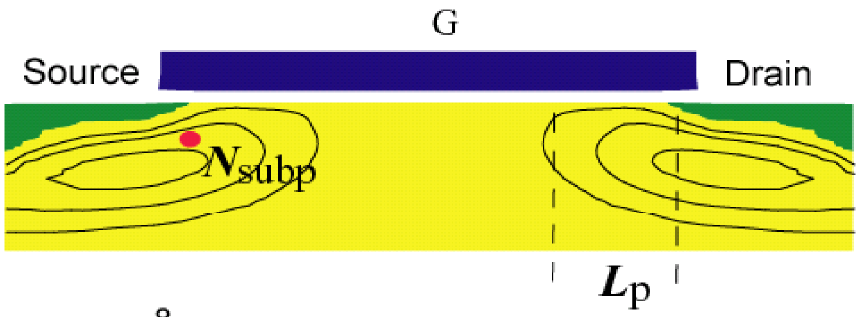
-Quantum Mechanical Effect

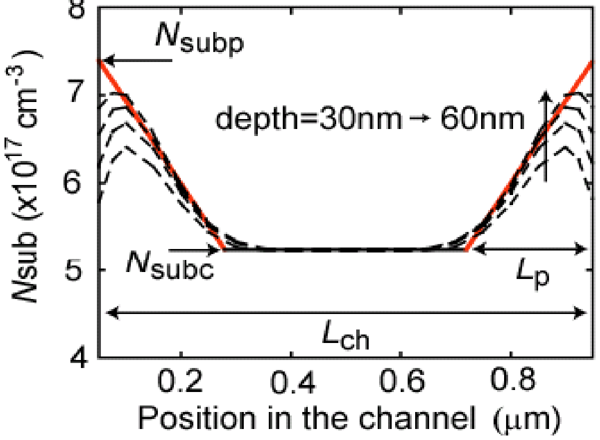
-Ballistic Effect

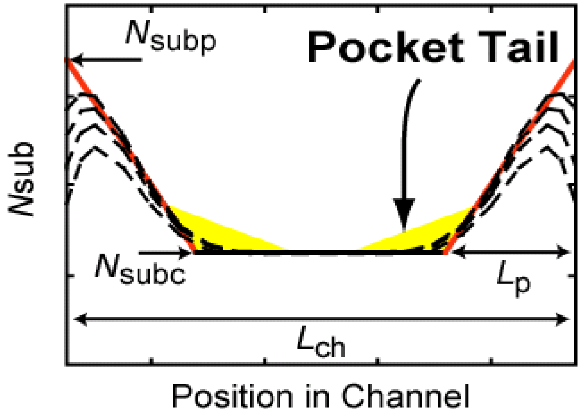
Surface-Potential-Based Model

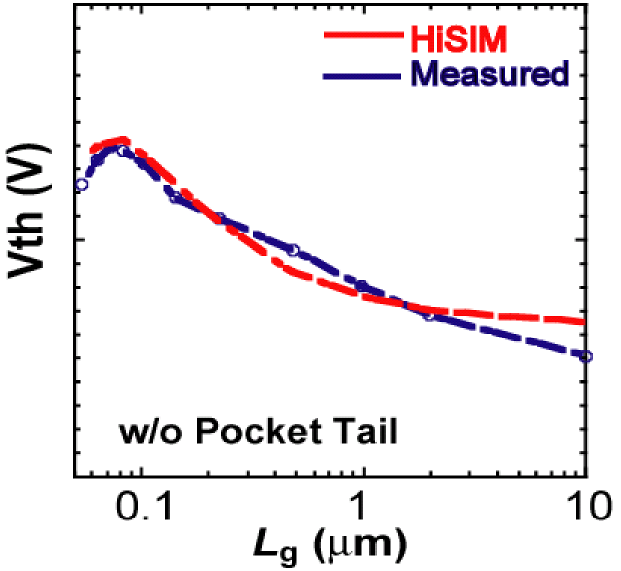
- Based on the Poisson equation
- No fitting parameter for subthreshold region
- Reflect device-parameter (Nsub, Tox etc.) dependence

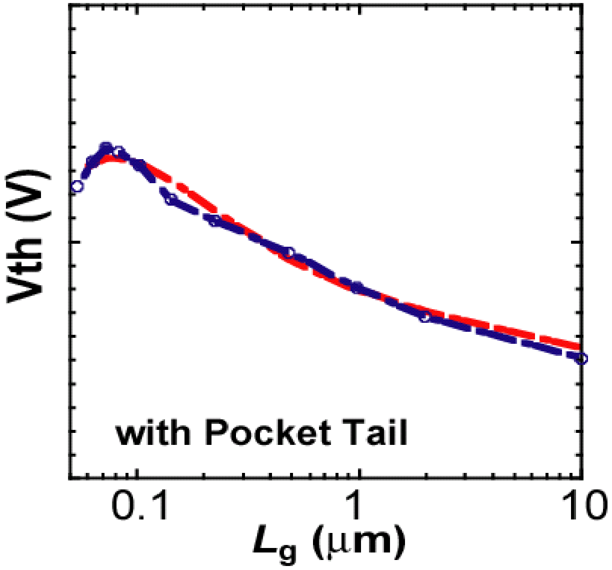
Pocket Implantation



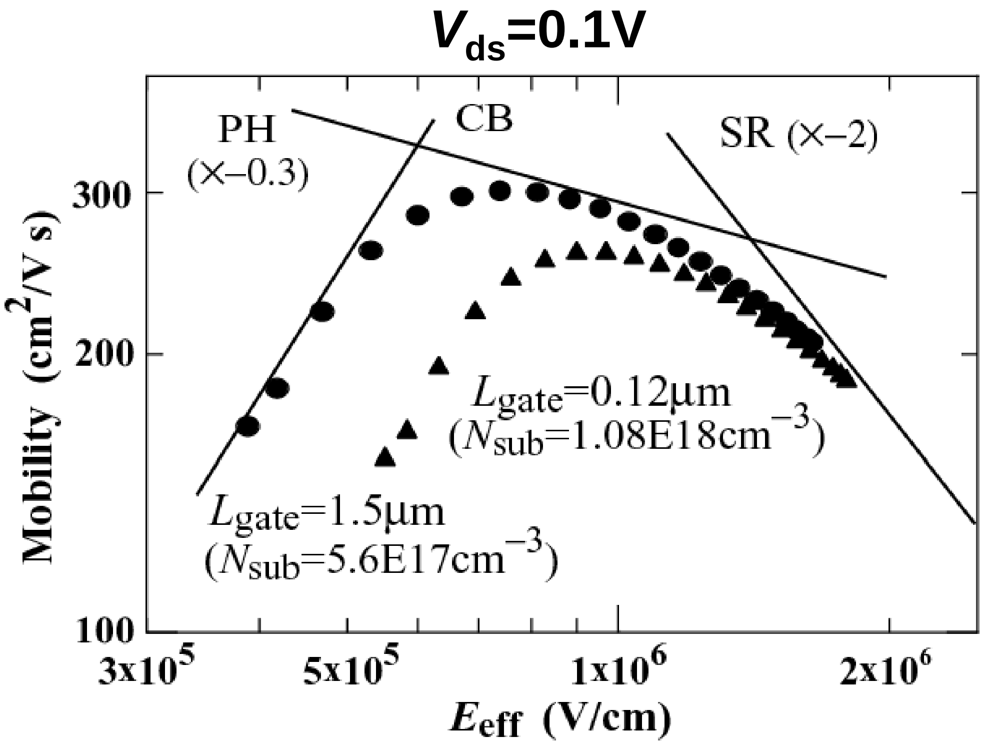








Universal Mobility



$$\frac{1}{\mu_0} = \frac{1}{\mu_{CB}} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}}$$

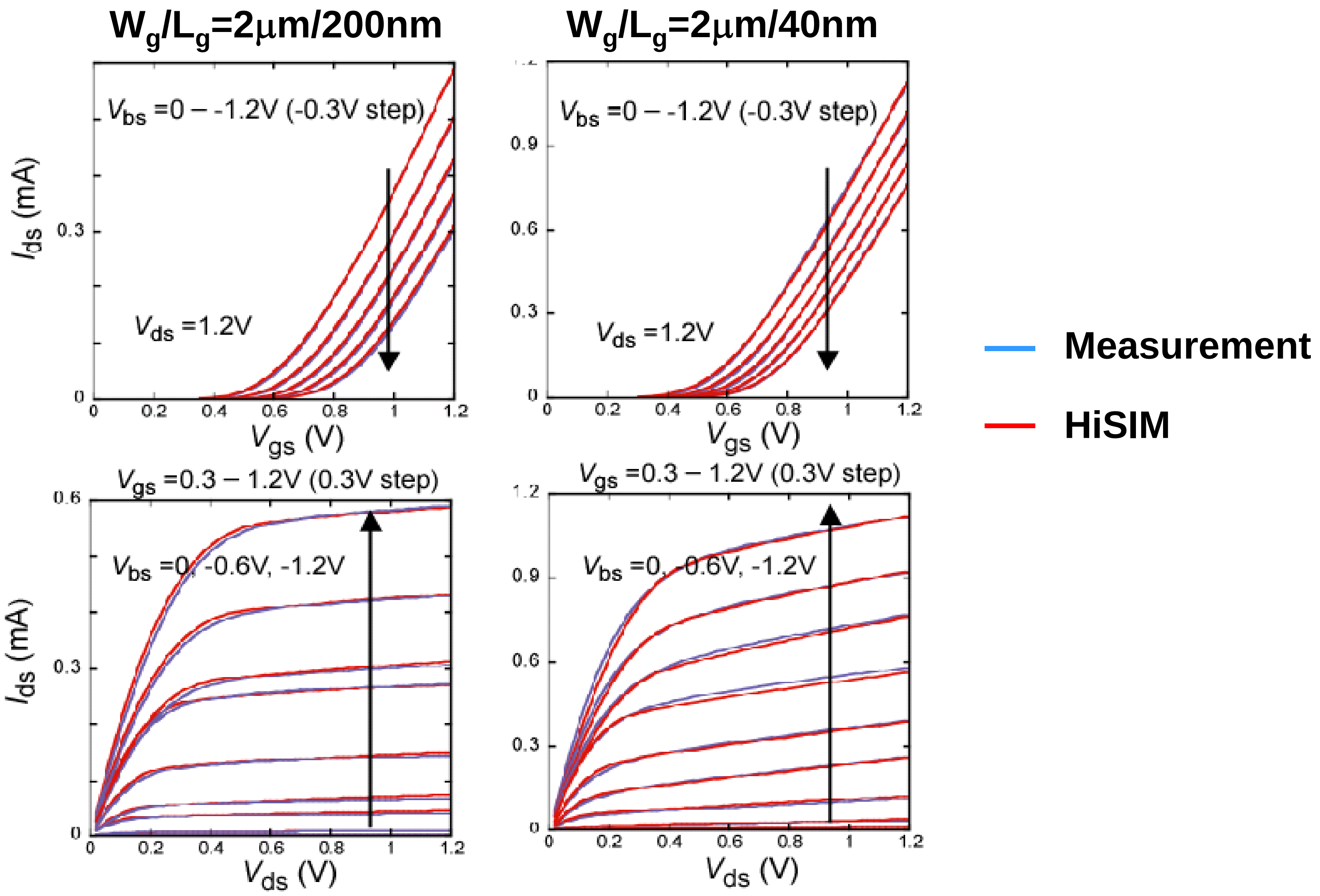
- $\mu_{CB} = CB0 + CB1 \dfrac{\boxed{Q_i}}{q \times 10^{11}}$
- $\mu_{PH} = \dfrac{PH0}{(T/300\mathrm{K})^{PHTMP} \times E_{eff}^{\,PH1}}$
- $\mu_{SR} = \dfrac{SR0}{E_{eff}^{\,SR1}}$

$$E_{eff} = \frac{1}{\varepsilon_{Si}}(NDEP \times \boxed{Q_b} + NINV \times \boxed{Q_i})$$

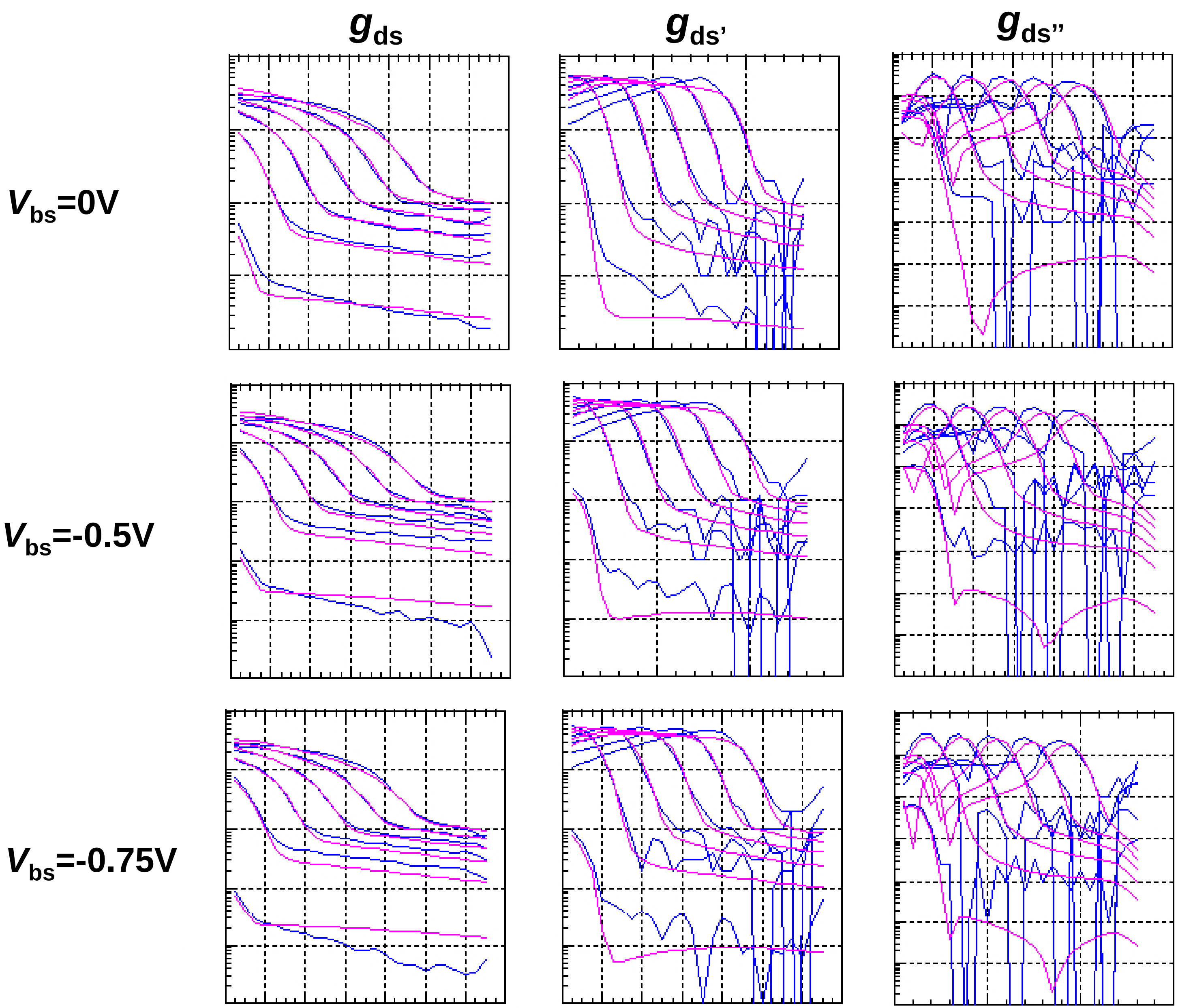
$PH1 = 0.3$
$SR1 = 2.0$
$NDEP = 1.0$
$NINV = 0.5$

impurity-concentration variation
↓
carrier-concentration variation
↓
carrier-mobility variation
↓
current variation

Model Ability: 45nm Technology



Higher order derivatives of I_d-V_d



g_{ds} g_{ds}' g_{ds}''

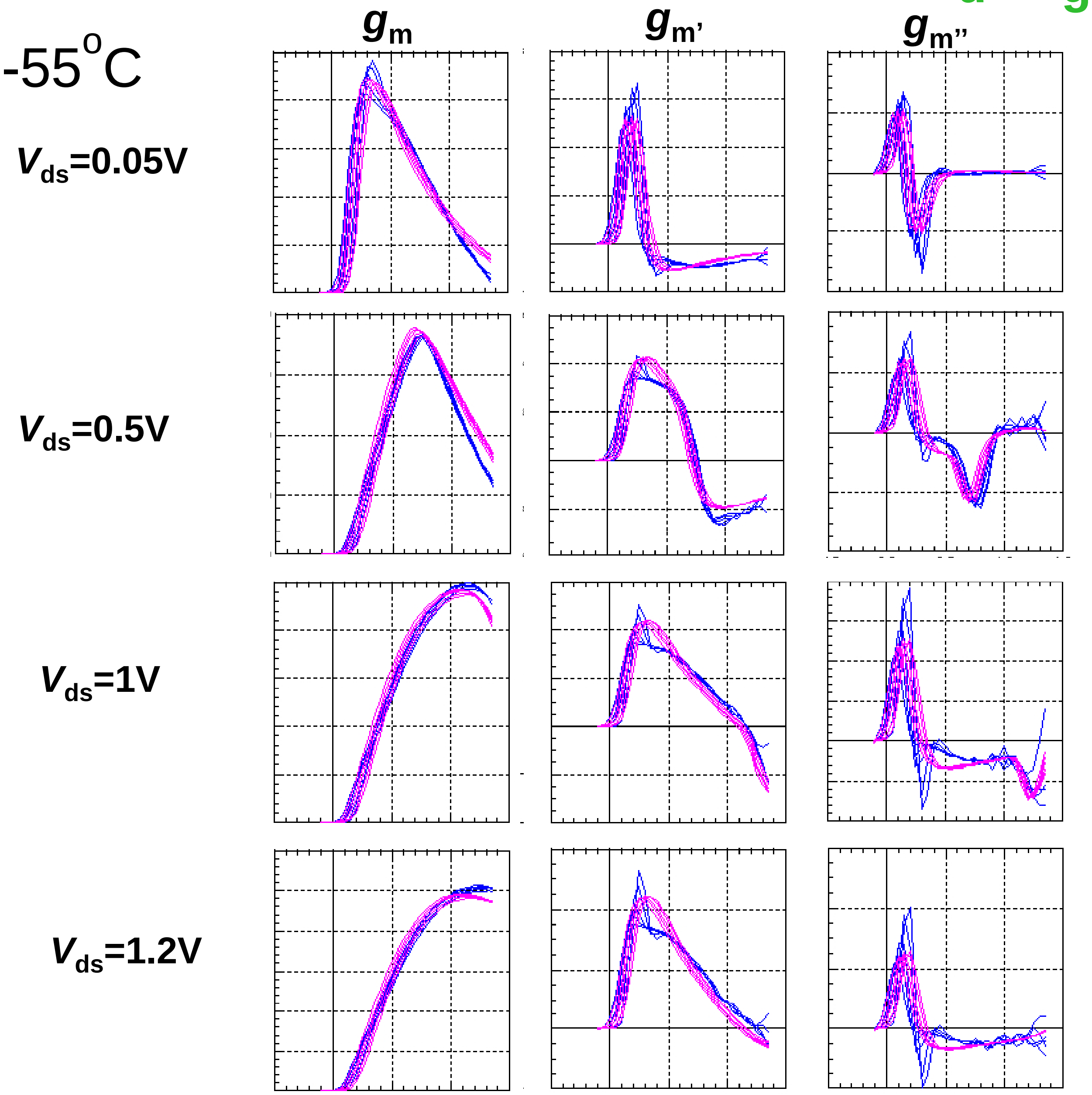
V_{bs}=0V

V_{bs}=-0.5V

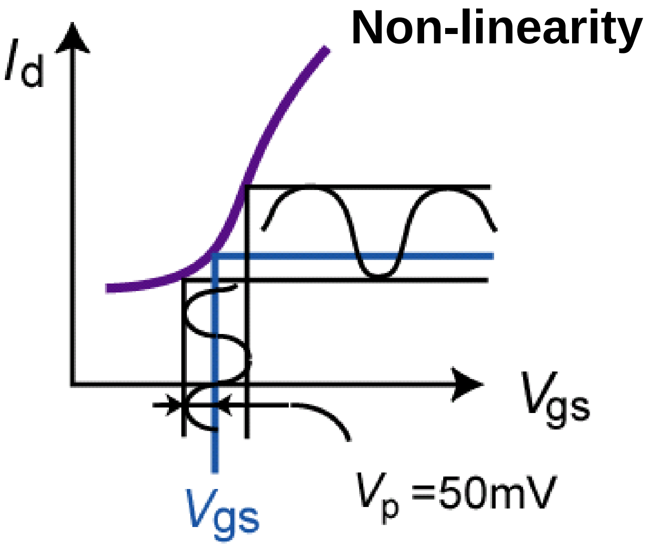
V_{bs}=-0.75V

Higher order derivatives of I_d-V_g

Temp = -55^{o}C



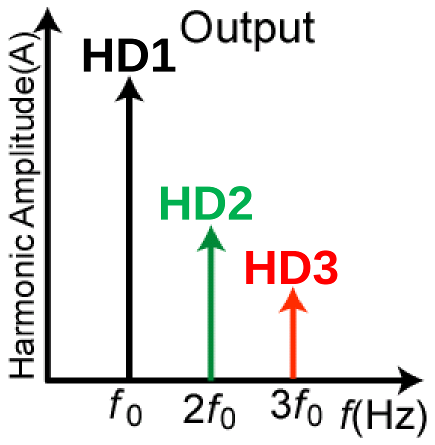
Harmonic Distortions: Model-Ability Check

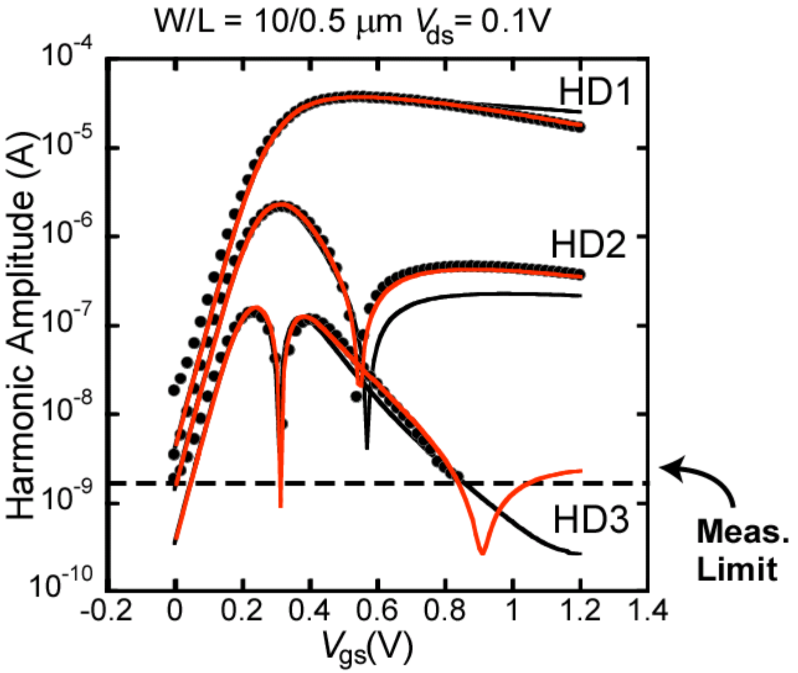


V_p =50mV

f_0=1kHz

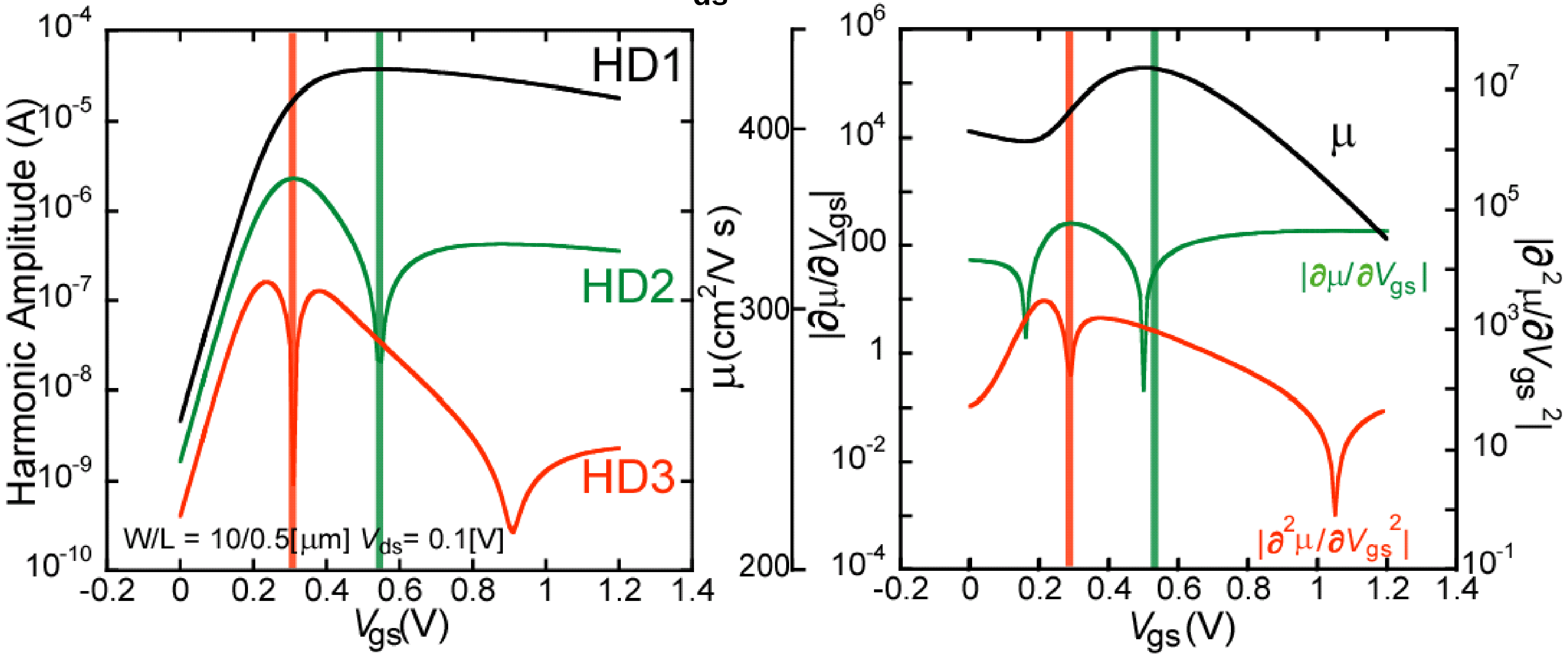
$V(t)=V_{gs}+\sin(2\pi f_0 t)$





Comparison with Mobility

V_{ds}=0.1V



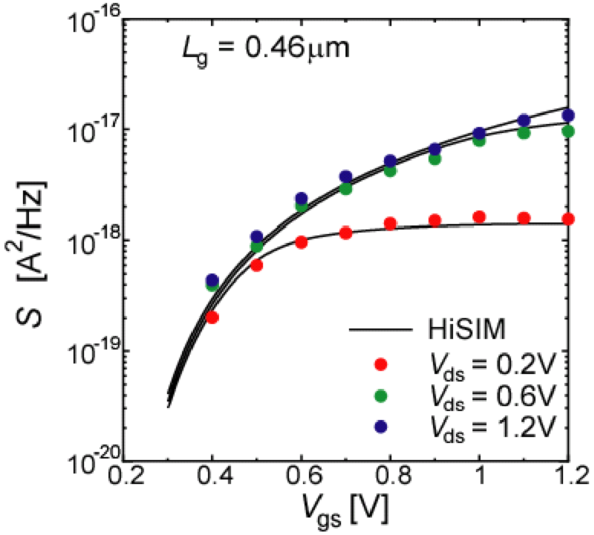
$$\mathrm{HD1} \approx \left| V_P \frac{\partial I_{ds}}{\partial V_{gs}} \right| \qquad \mathrm{HD2} \approx \left| -\frac{1}{4} V_P^2 \frac{\partial^2 I_{ds}}{\partial V_{gs}^2} \right| \qquad \mathrm{HD3} \approx \left| -\frac{1}{24} V_P^3 \frac{\partial^3 I_{ds}}{\partial V_{gs}^3} \right|$$

Mobility determines the harmonic distortion characteristics.

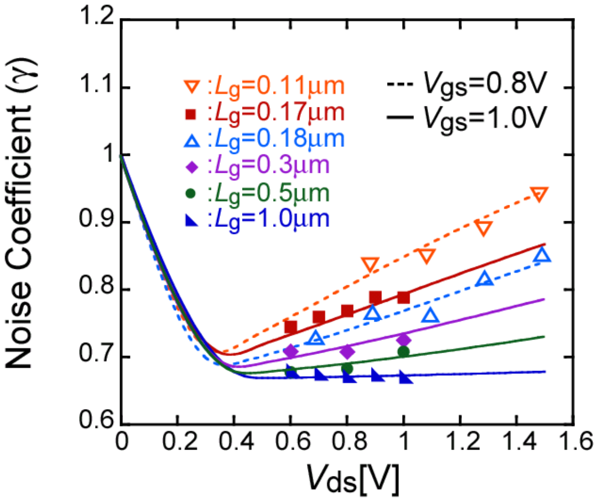
D. Navarro et al., Proc. SISPAD, p. 259, 2004.

Characteristics Important for RF Applications

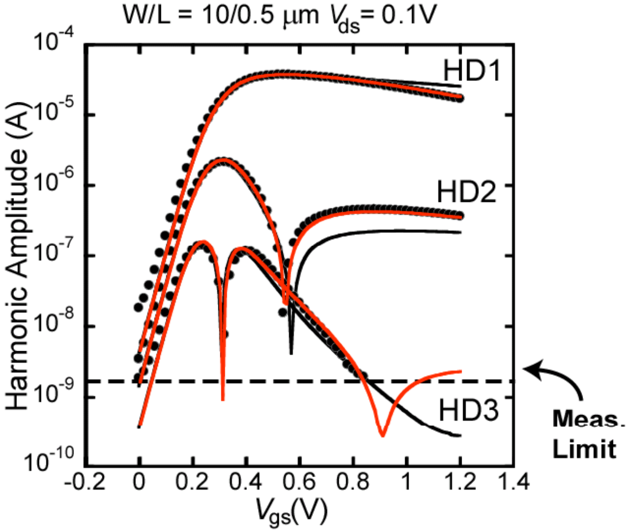
1/*f* Noise



Thermal Noise



Harmonic Distortion



- ➢ **Integrating *n*, μ along the channel derives analytical descriptions.**
- ➢ **No additional model parameters are required.**
- ➢ **Features are determined only by *I-V* characteristics.**

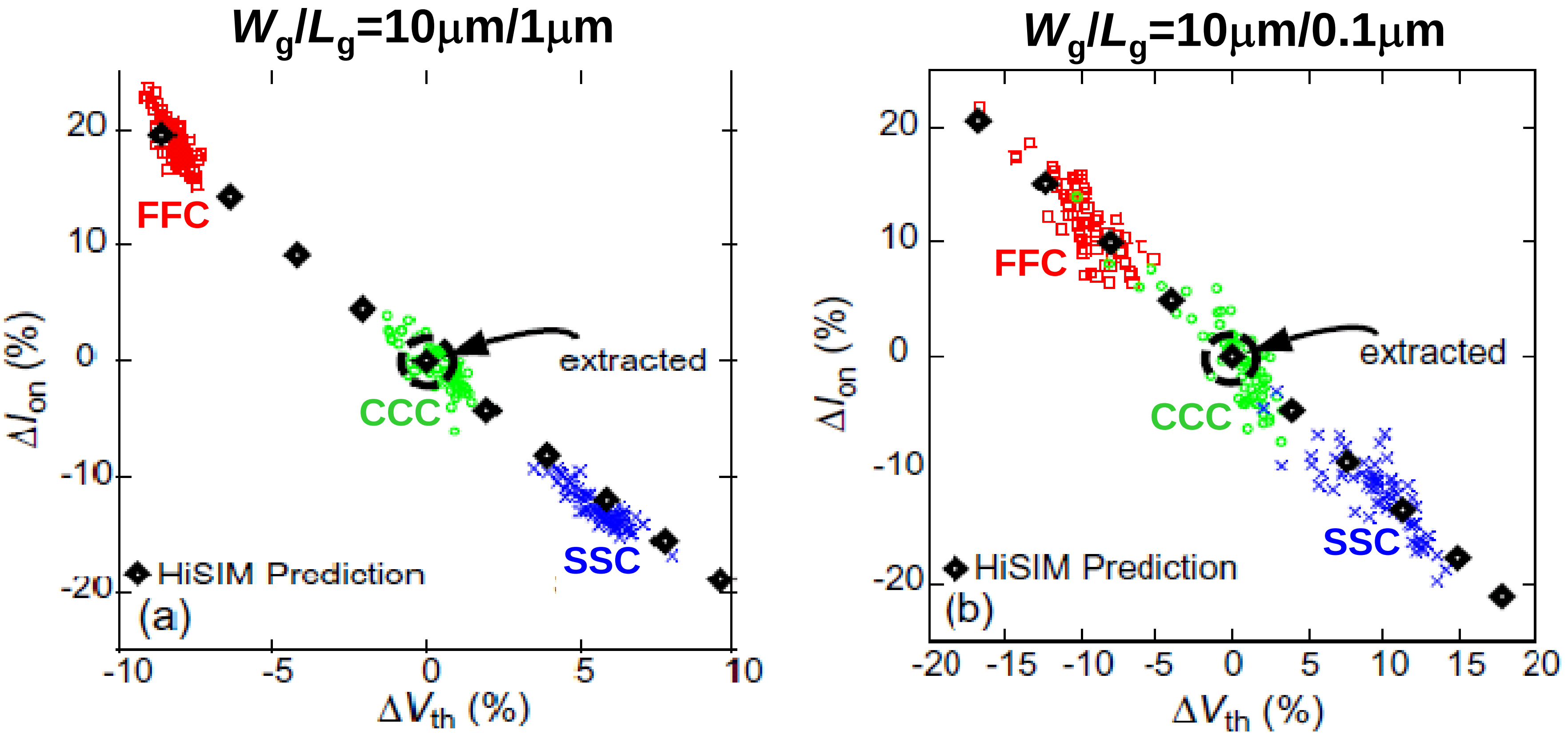
Surface-potential distribution along the channel is the key.

M. Miura-Mattausch, SISPAD 2005.

2. Variation Extraction

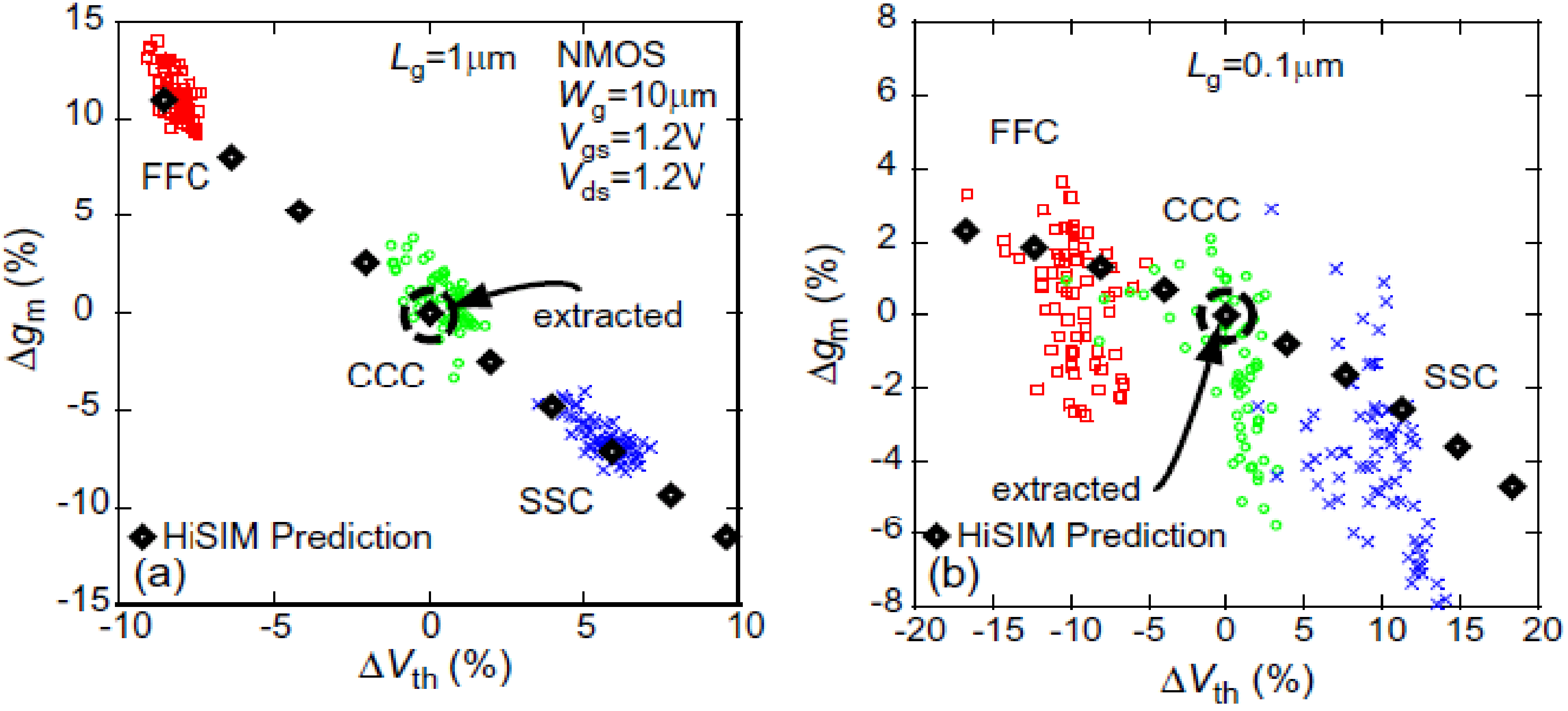
- DC measurements (inter-chip variation)
- basic analog circuits (intra-chip variation)

Extraction for Nominal Chip

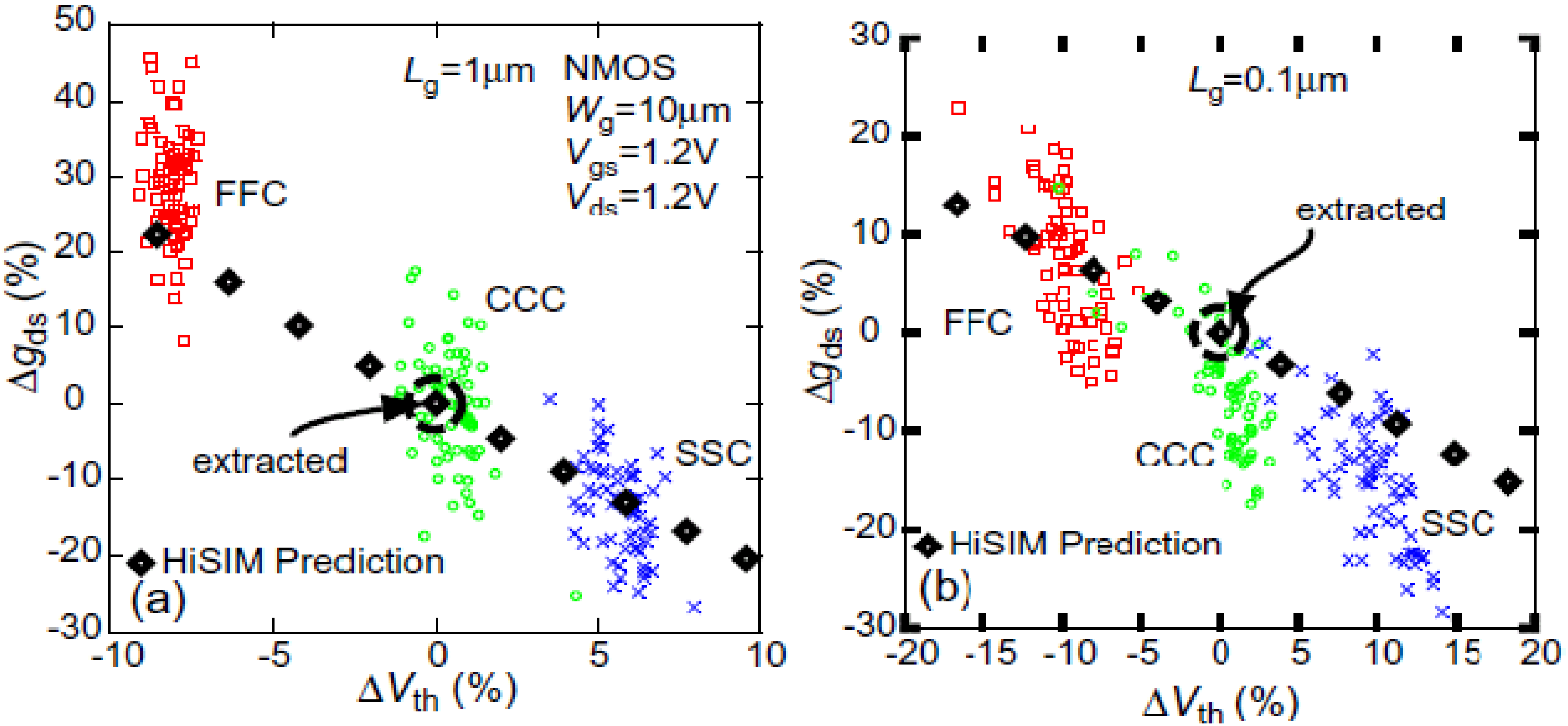


predictability of N_{sub} variation

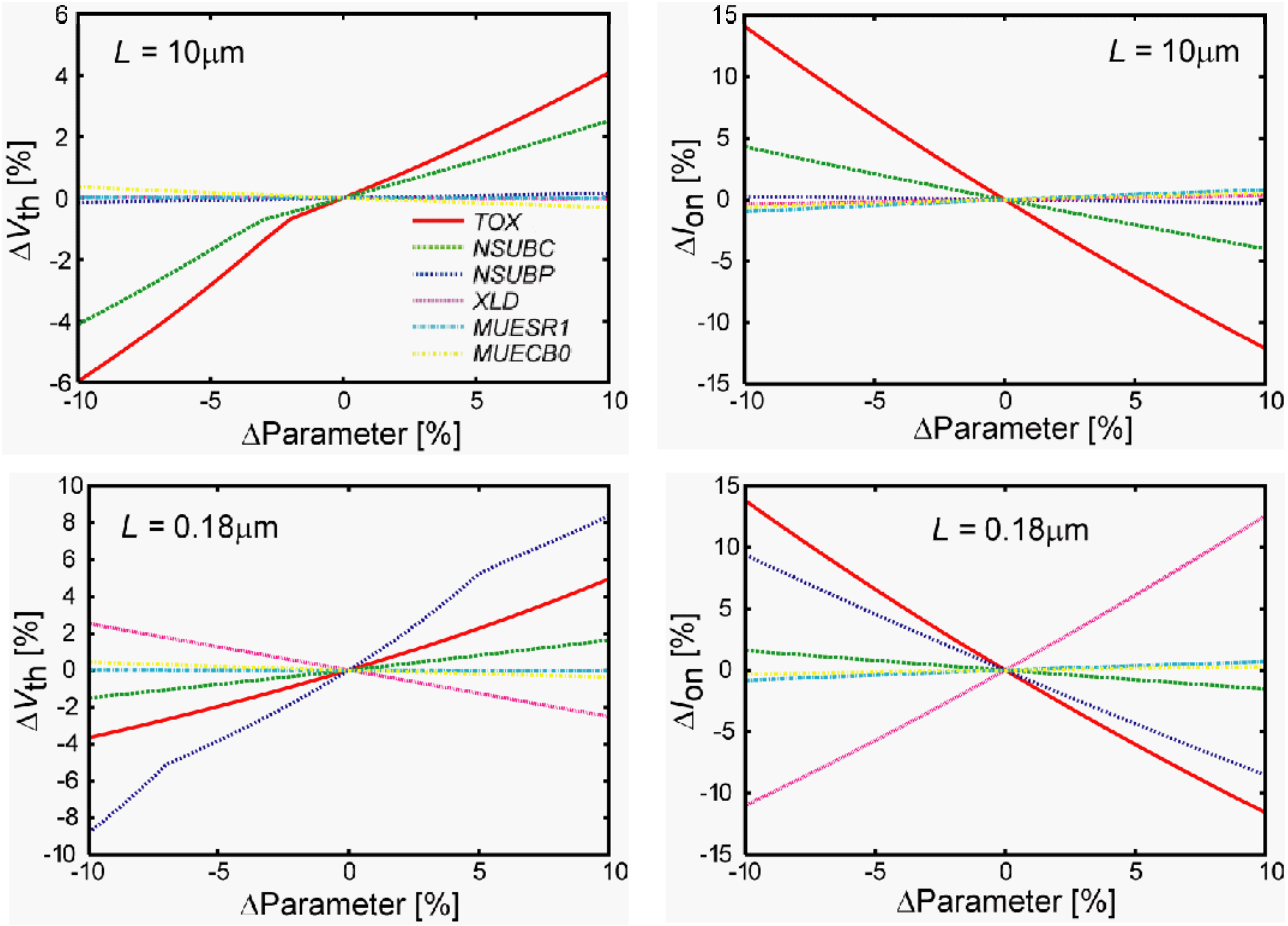
Prediction of N_{sub} Variation: g_m



Prediction of N_{sub} Variation: g_{ds}



Sensitivity Analysis of Model Parameters



Number of model parameters for capturing the V_{th} and I_{on} variation is limited.

Parameter Extraction for Inter-Chip Variation

Tox: oxide thickness ← usually small

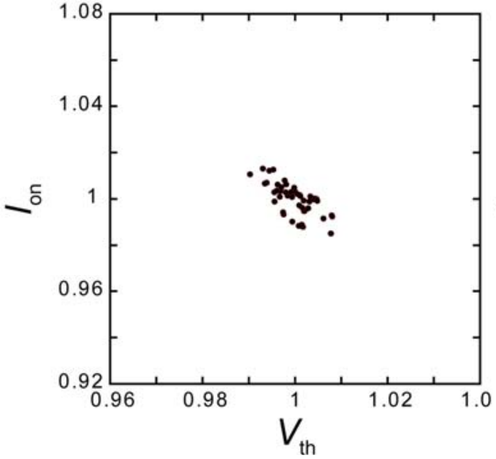
NSUBC: substrate impurity concentration

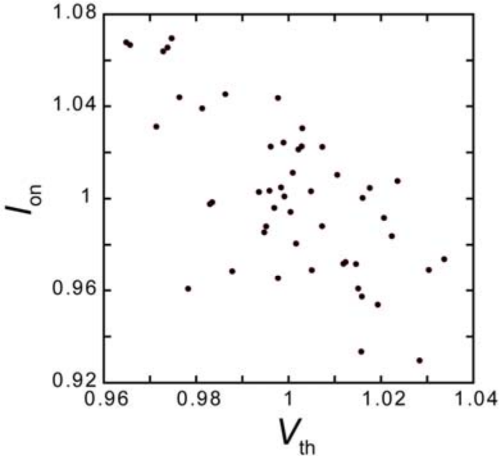
NSUBP: pocket impurity concentration

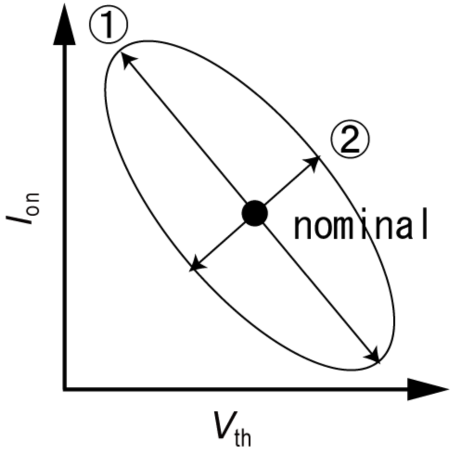
XLD: overlap length

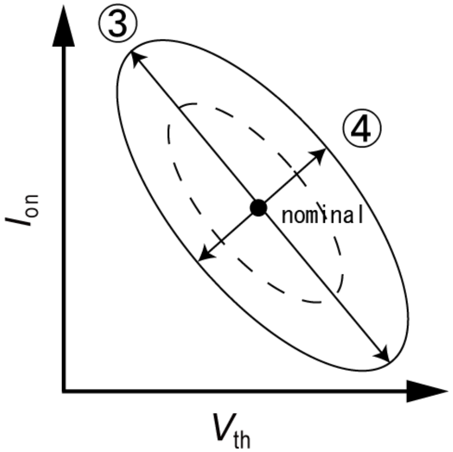
MUESR1: surface-roughness scattering

Extraction Method for Microscopic Variations


long channel

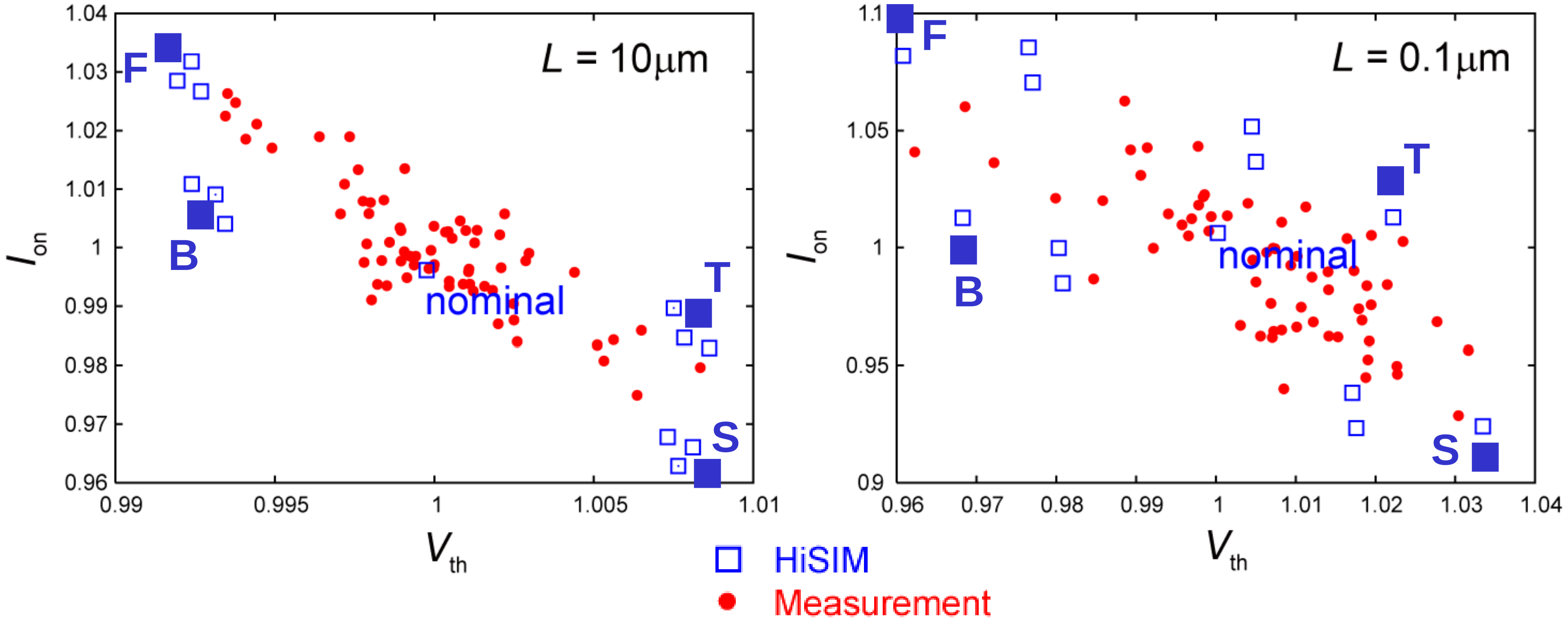

short channel


long channel

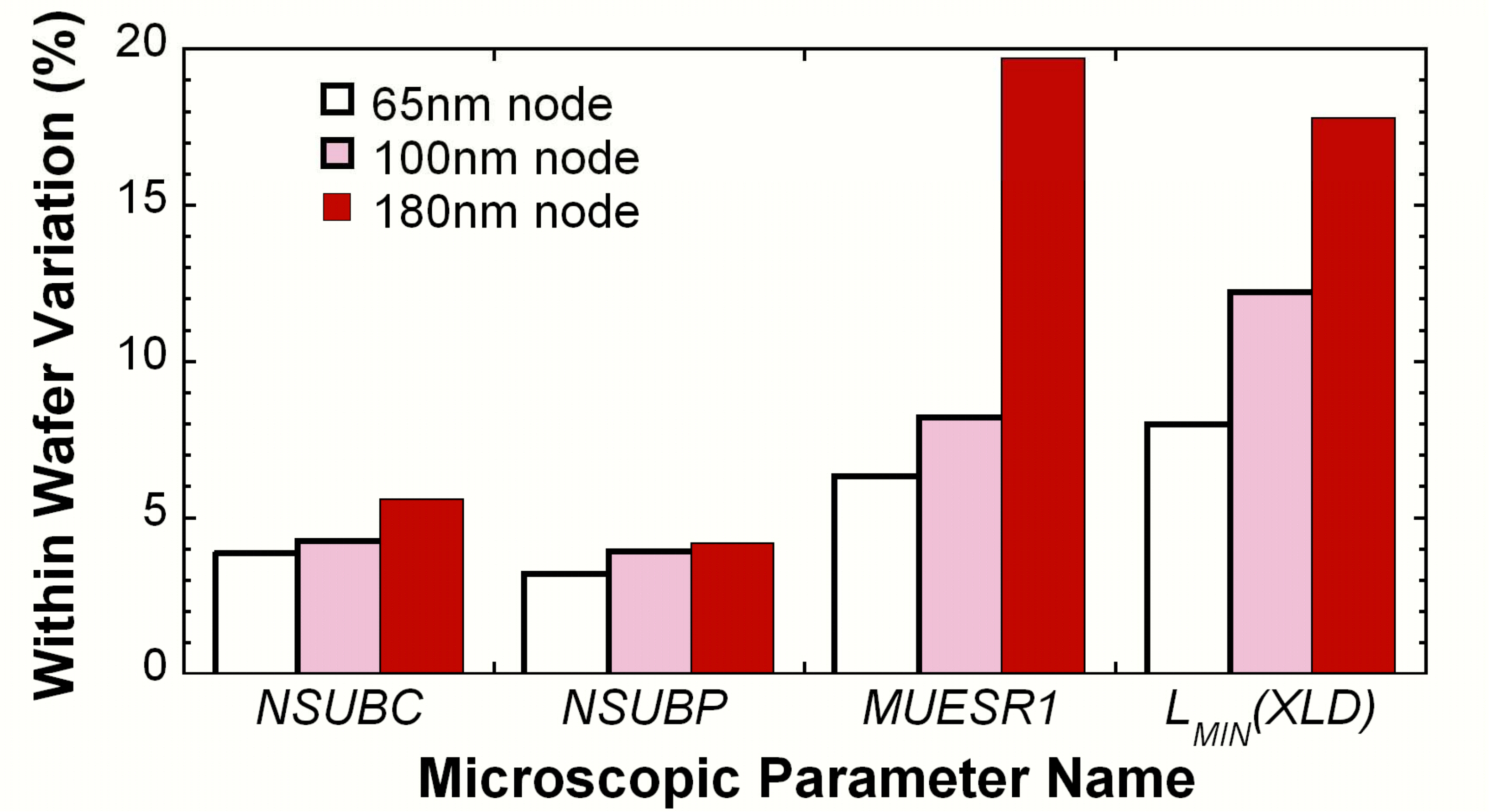

short channel

Step	Device	Parameter	Direction
1	Long	*NSUBC*	①
2		*MUESR1*	②
3	Short	*NSUBP*	③
4		*XLD*	④

With 4 parameters 16 (2^4) combinations of variation boundaries are possible.


L = 10μm
1.04
1.03
1.02
1.01
1
0.99
0.98
0.97
0.96
I_{on}
0.99
0.995
1
1.005
1.01
V_{th}
F
B
T
S
nominal
L = 0.1μm
1.1
1.05
1
0.95
0.9
I_{on}
0.96
0.97
0.98
0.99
1
1.01
1.02
1.03
1.04
V_{th}
F
B
T
S
nominal
□ HiSIM
● Measurement

Variations in Different Generations



Improvements:

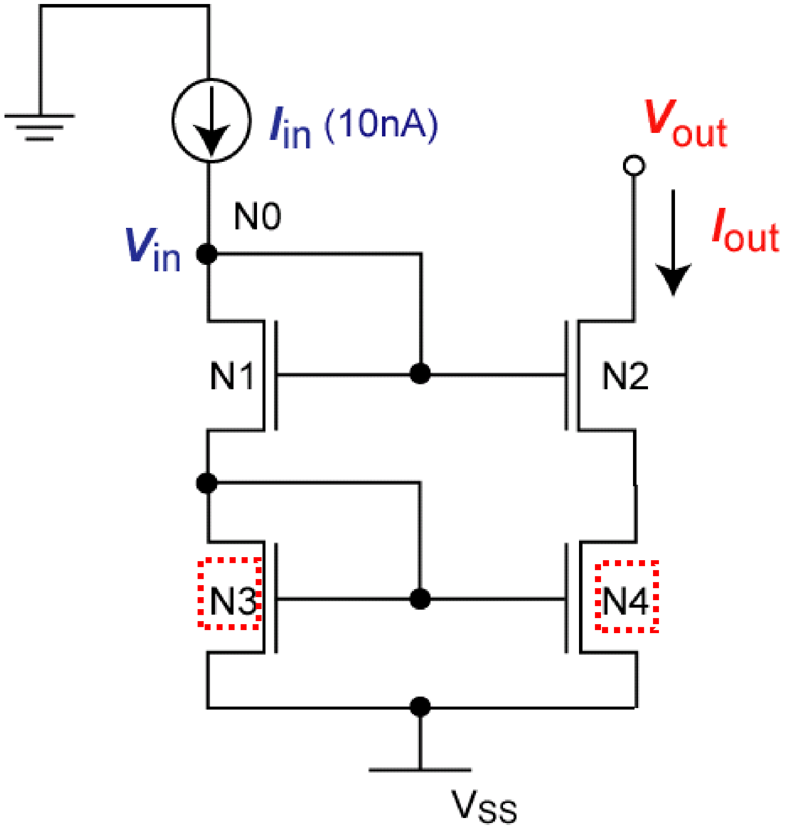
- gate-stack related: MUESR1 (70%)
- lithography related: L_{MIN}(XLD) (55%)
- doping related: NSUBC (30%), NSUBP (25%)

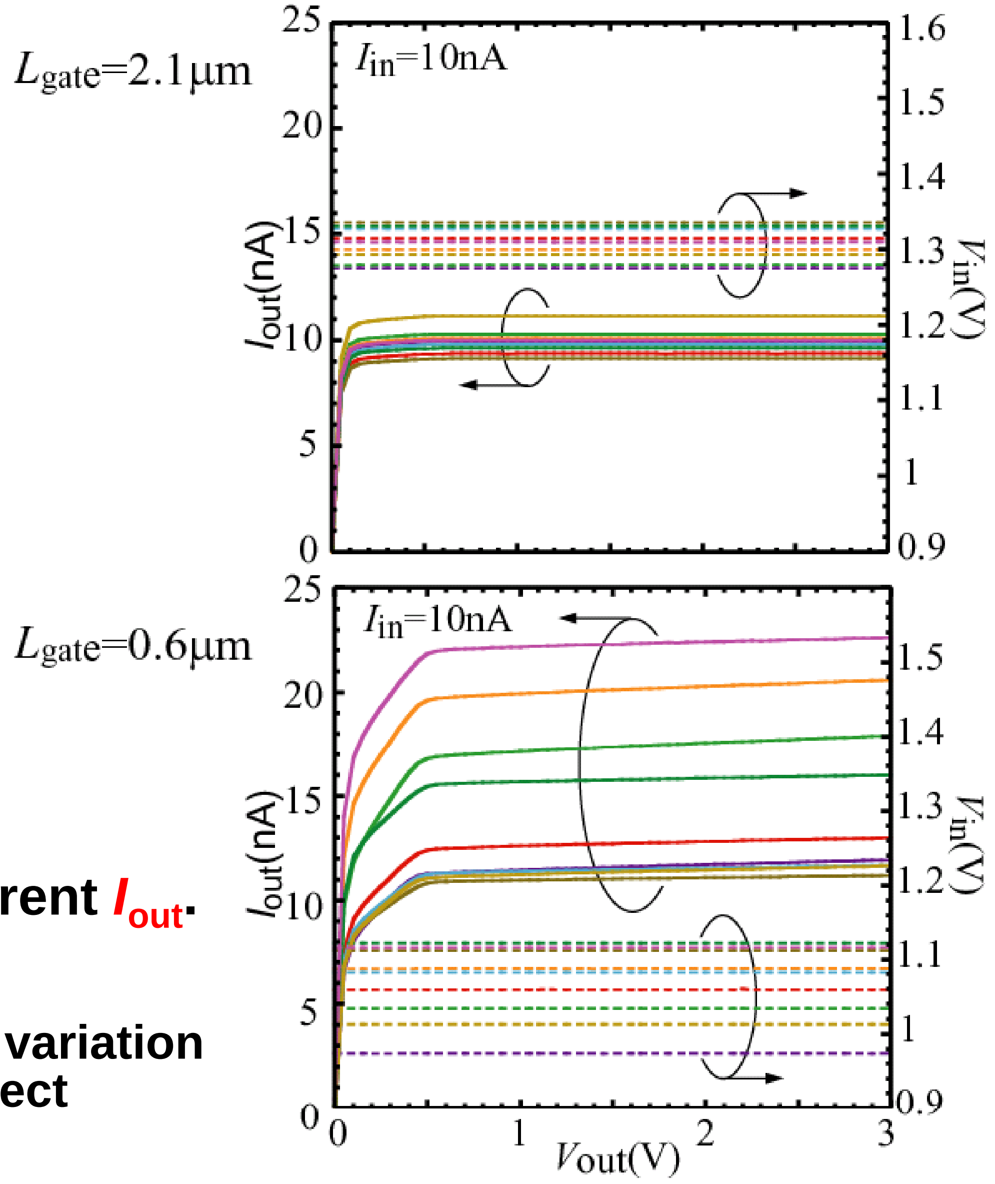
H. J. Mattausch et al., IEEE EDL, 30, 873, 2009.

Parameter Extraction for Intra-Chip Variation

- Cascode-Current Source
- Differential-Amplifier-Stage with Feed-back Coupling

Cascode-Current Source





Function: provide a constant current I_{out}.

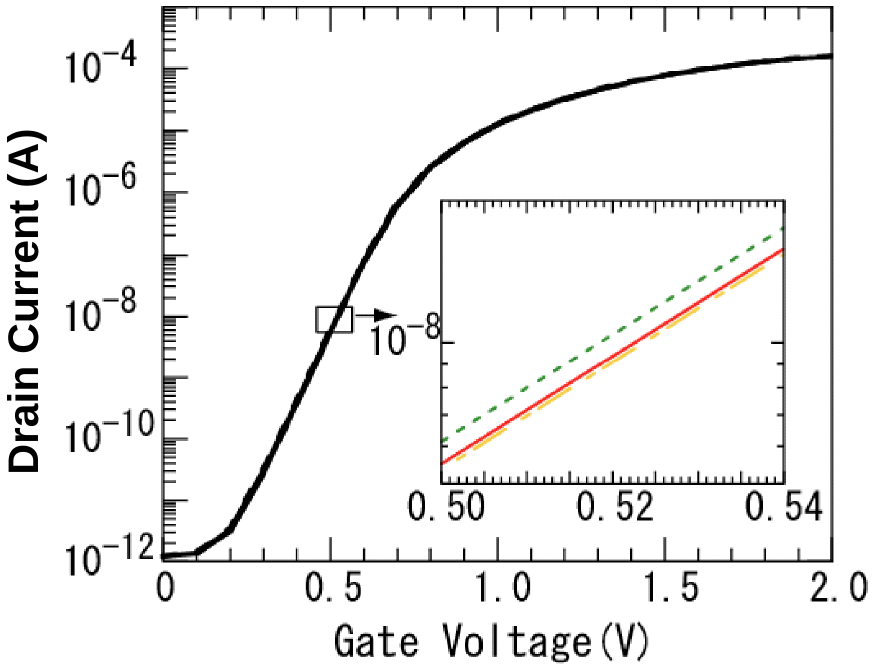
Condition: I_{in}=10nA

- **enhanced technology variation**
- **exclude resistance effect**

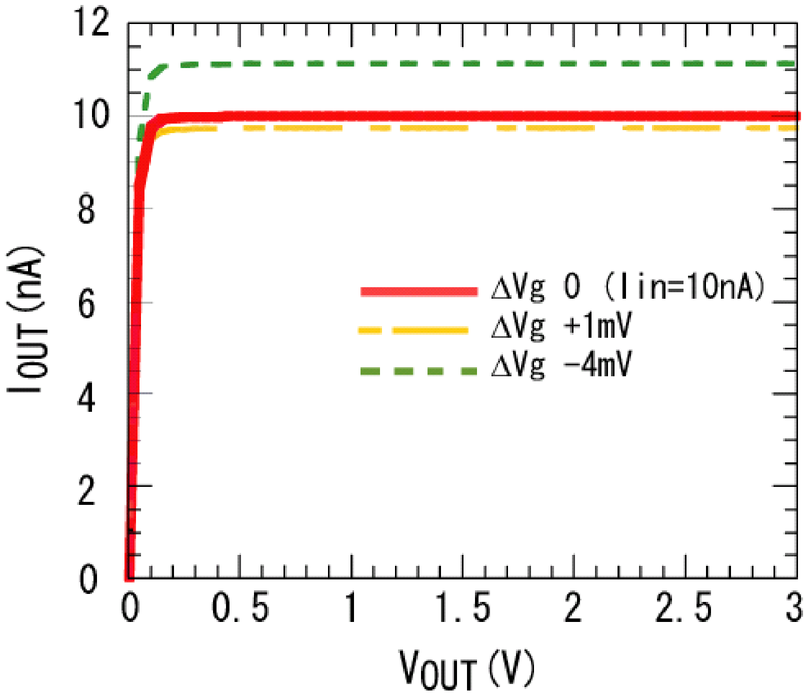
D. Miyawaki et al., APS-DAC, p. 39, 2001.

Origin of I_{out} Variation

Inter-Chip Variation

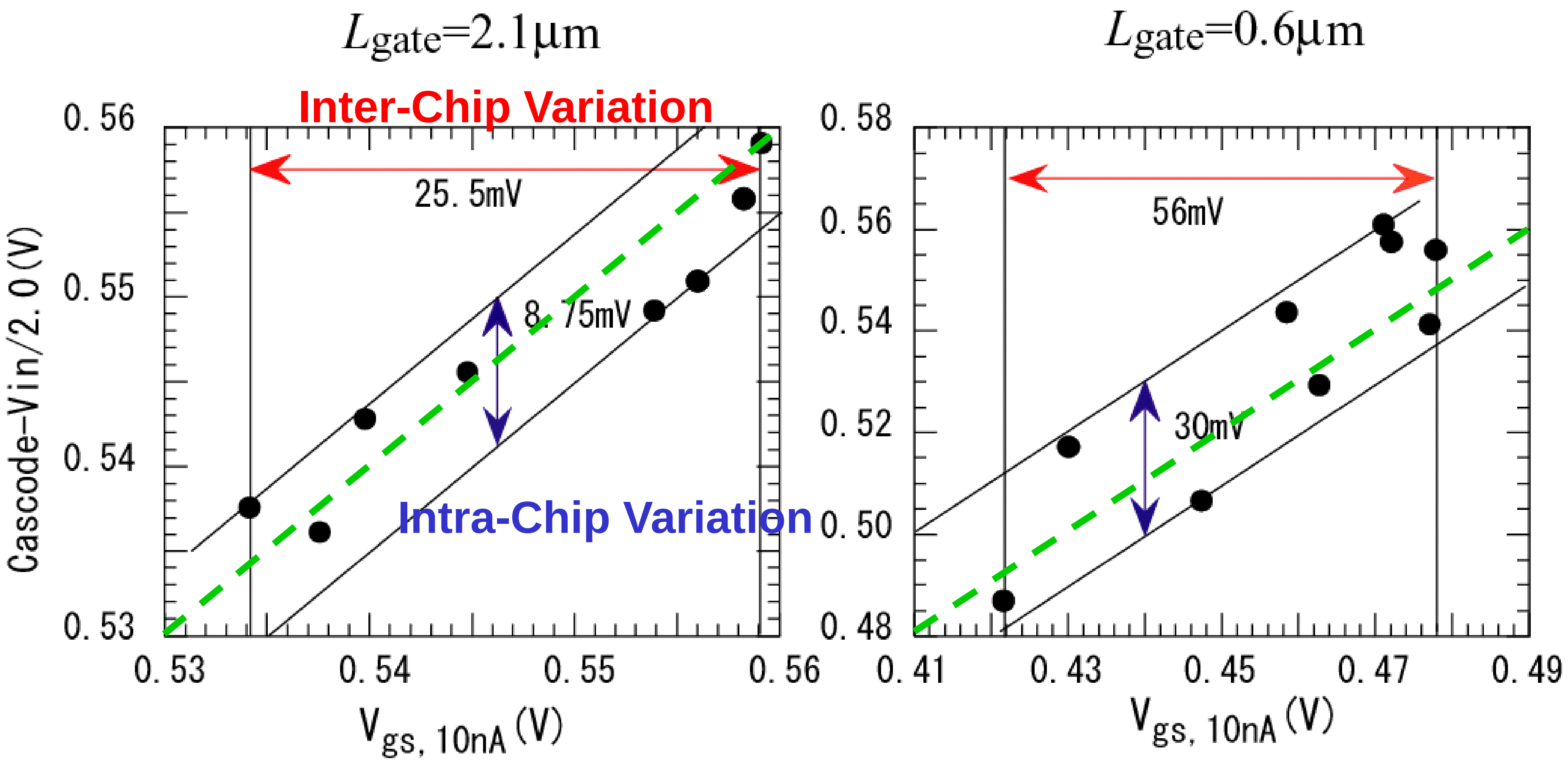


N3 is fixed and N4 is varied.



Mismatch between N3 and N4 is responsible for I_{out} variation.

Extraction of Intra-Chip Variation



L_{gate}=2.1μm

L_{gate}=0.6μm

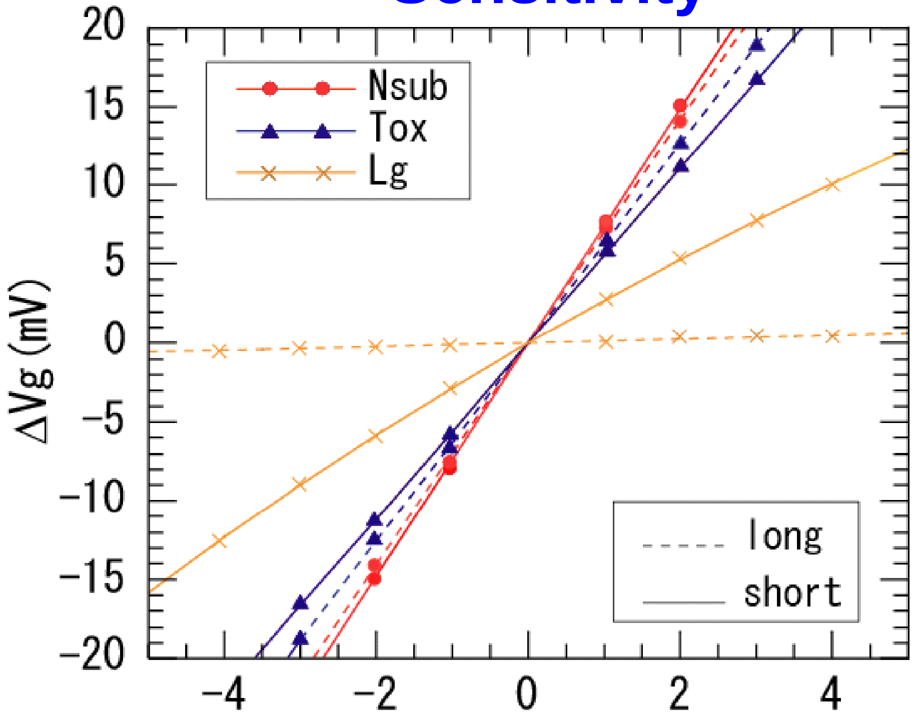
Inter-Chip Variation

Intra-Chip Variation

Extraction Results

	2.1μm	0.6μm
Inter	25.5mV	56mV
Intra	8.75mV	30mV

Sensitivity

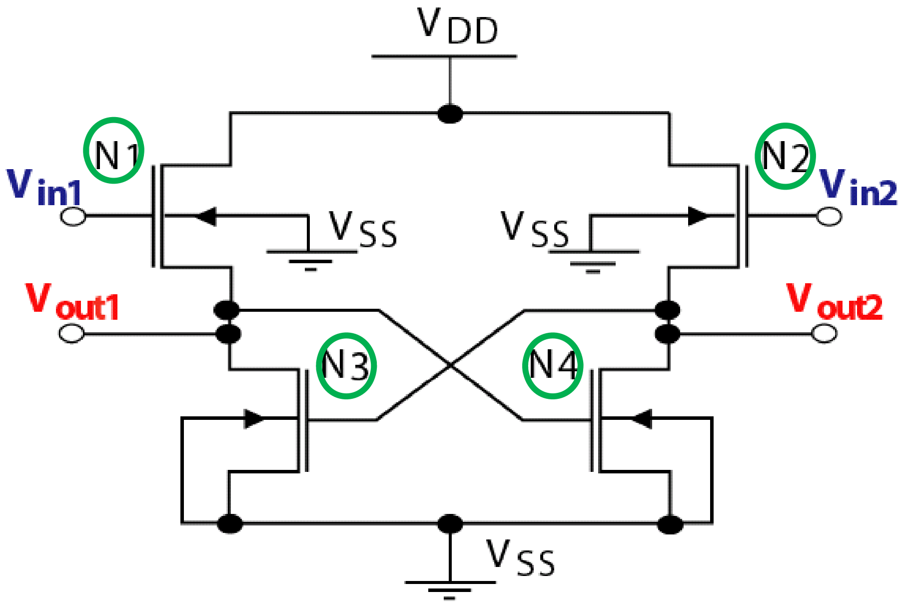


deviation [%]

Sensitivity Analysis
(intra-chip variation → random)

	ΔN_{sub}	ΔL_{gate}/0.6μm	T_{ox}
Inter	-1.2% / -7%	6.7% / -3.3%	1.4% / 0.7%
Intra	1%	3.8%	0

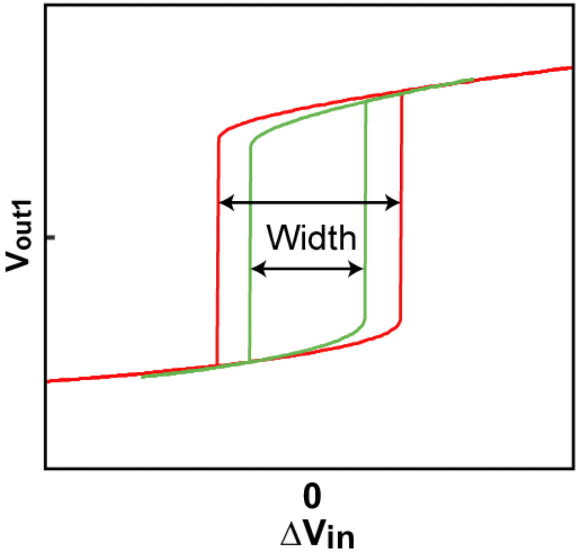
Differential-Amplifier-Stage with Feed-back Coupling

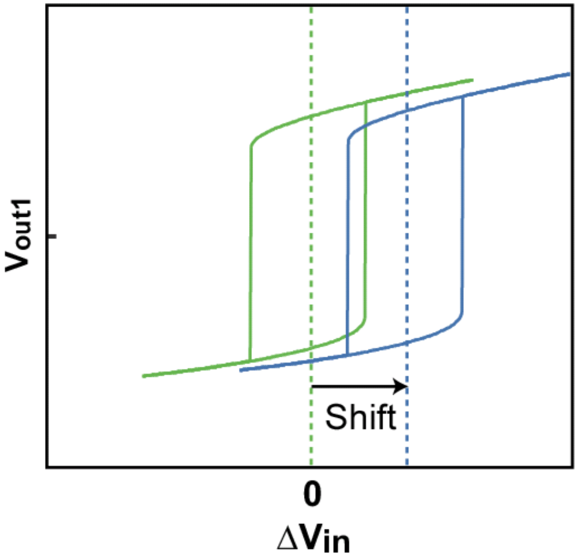


Function: to amplify *Vin* to *Vout*

S. Matsumoto et al., CICC, p. 357, 2001.

4 devices same variations → inter; 4 devices different variations → intra





ΔVin= Vin1-Vin2

Obtained Results

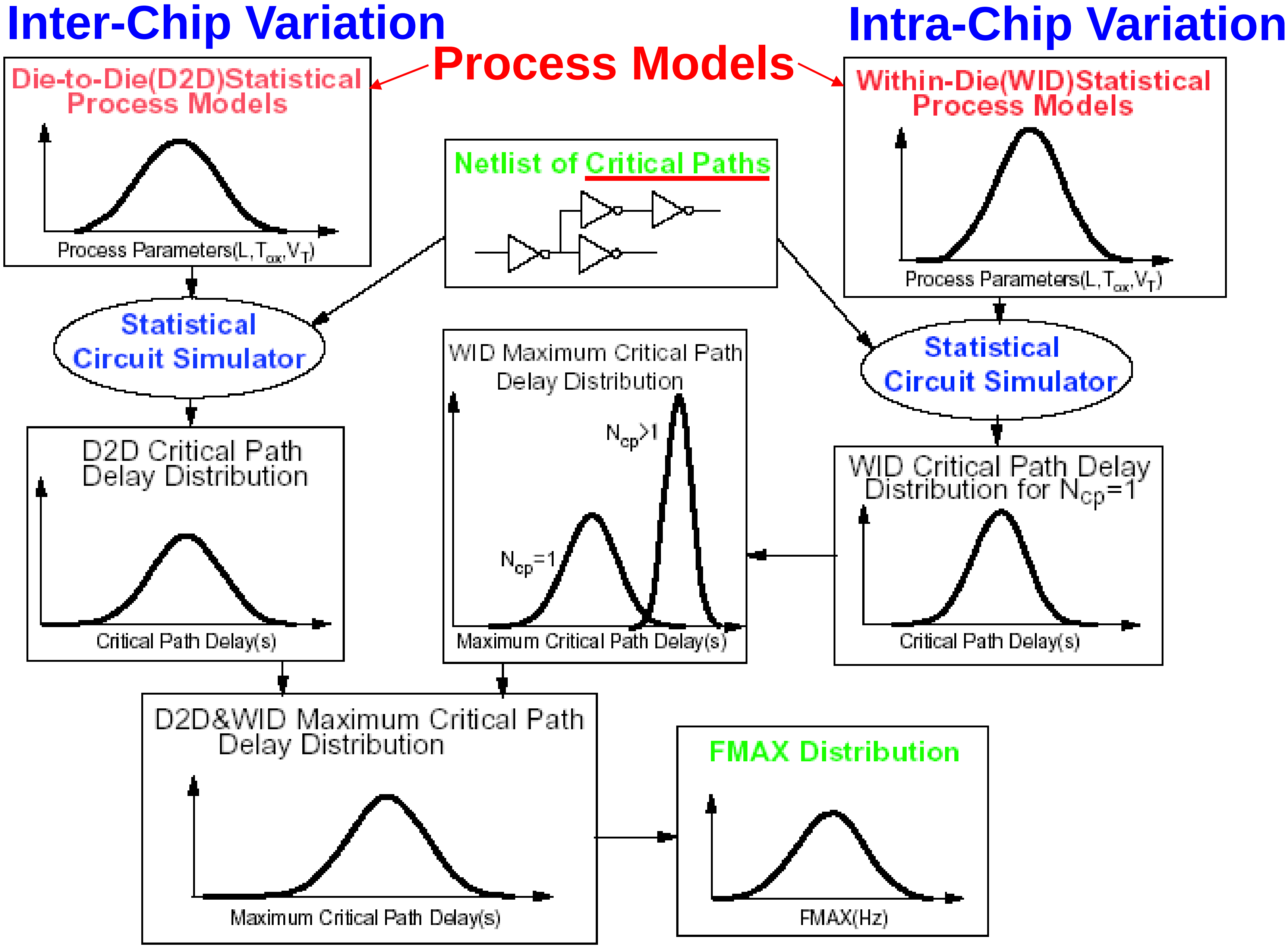
Cascode-Current Source

	ΔN_{sub}	$\Delta L_{gate}/0.6\mu m$
Inter	7%	6.7%
Intra	1%	3.8%

Differential-Amplifier-Stage with Feed-Back-Coupling

	ΔN_{sub}	$\Delta L_{gate}/0.6\mu m$
Inter	5.9%	6.2%
Intra	2.3%	3.2%

3. Methodology Incorporating Circuit Simulation



Inter-Chip Variation

Intra-Chip Variation

Process Models

Die-to-Die(D2D)Statistical Process Models

Within-Die(WID)Statistical Process Models

Netlist of Critical Paths

Statistical Circuit Simulator

Statistical Circuit Simulator

D2D Critical Path Delay Distribution

WID Maximum Critical Path Delay Distribution

WID Critical Path Delay Distribution for $N_{cp}=1$

D2D&WID Maximum Critical Path Delay Distribution

FMAX Distribution

K. A. Bowman et al., IEEE J. SSC, 37, 183, 2002.

Approach

Number of responsible model parameters for variation are small.

↓

- **For variation combinations, Monte Carlo simulation**

- **For circuit-performance simulation**
    1. **analytical description**
    2. **SPICE simulation**

- **For intra-chip variation**
    1. **Monte Carlo simulation**
    2. **consider two boundaries (best, worst)**

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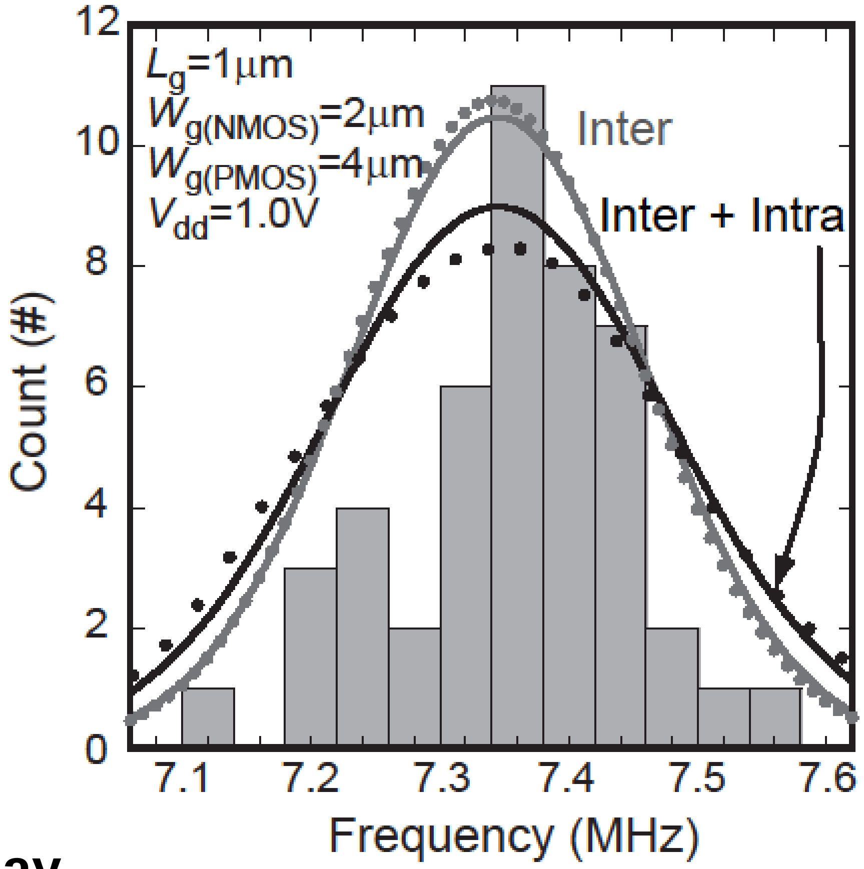
Distribution of Circuit Performances

(Monte Carlo Simulation with 10000 Samples)

51-Stage Ringoscillator



Dots: analytical equation for delay

Monte Carlo simulation for both inter/intra-chip variations

Lines: SPICE simulation with HiSIM2

(inter: Monte Carlo; intra: best+worst assume random variation)

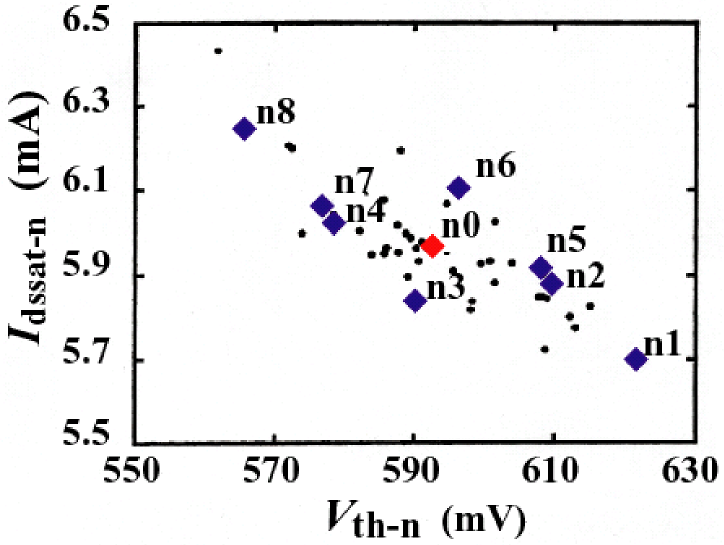
Summary

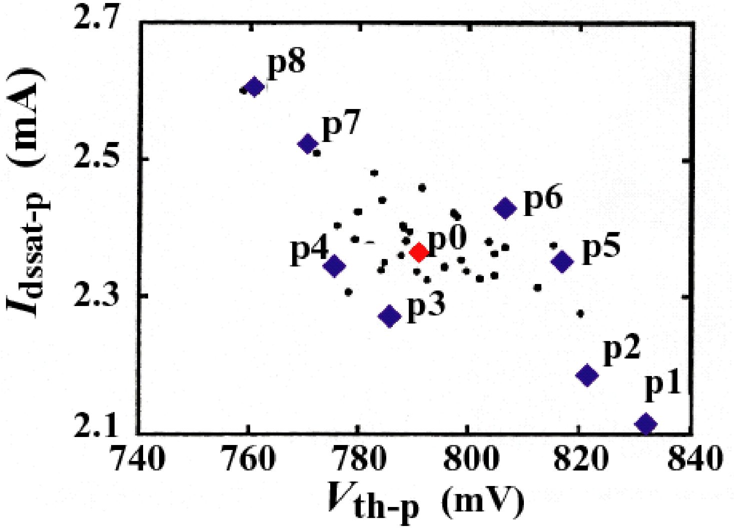
- ✓ Compact modeling based on surface-potential description provides accurate and fast statistical simulation.

- ✓ Accurate parameter extraction is the key for accurate prediction of circuit performance.

- ✓ Statistical circuit simulation is getting realistic.

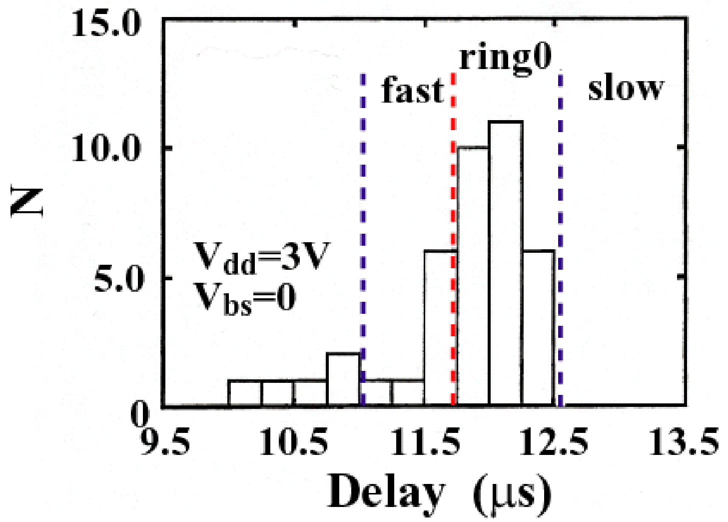
測定されるデバイスレベルのばらつき





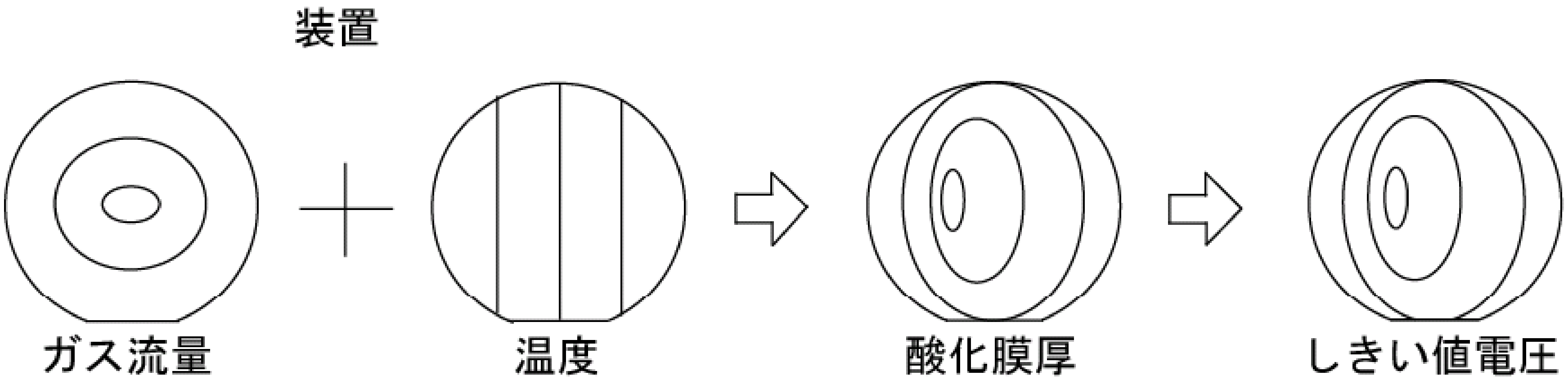
測定される回路レベルのばらつき

	ΔL	$\Delta N_{sub,n}$	$\Delta N_{sub,p}$	ΔT_{ox}
1	2σ	2σ	-2σ	2σ
2	2σ	2σ	-2σ	-2σ
3	2σ	-2σ	2σ	2σ
4	2σ	-2σ	2σ	-2σ
5	-2σ	2σ	-2σ	2σ
6	-2σ	2σ	-2σ	-2σ
7	-2σ	-2σ	2σ	2σ
8	-2σ	-2σ	2σ	-2σ

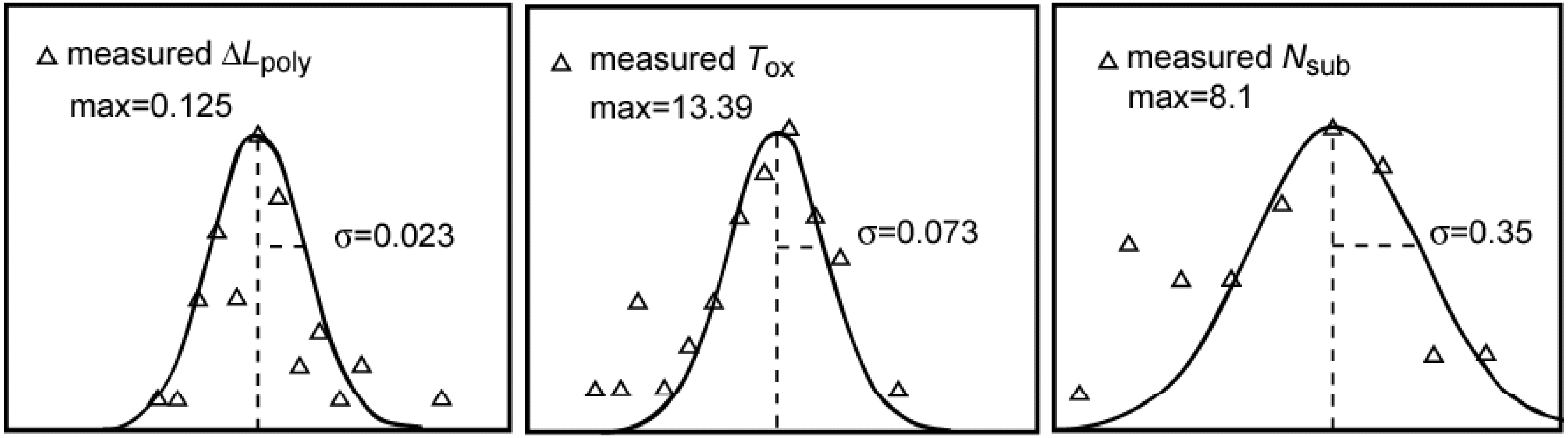


O. Prigge et al., IEICE, E82-C, p. 9107, 1999.

Inter-Chipばらつき

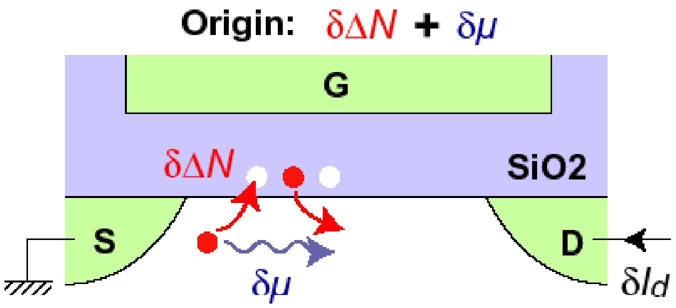


Wafer上のばらつき:In-Line測定からの抽出

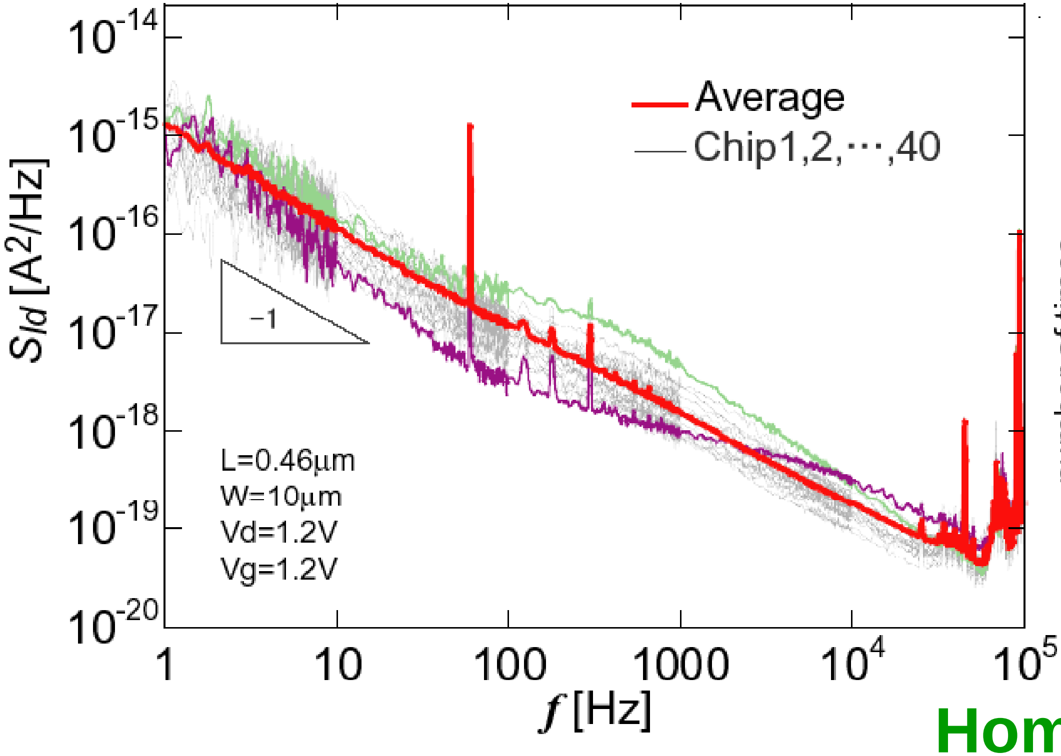


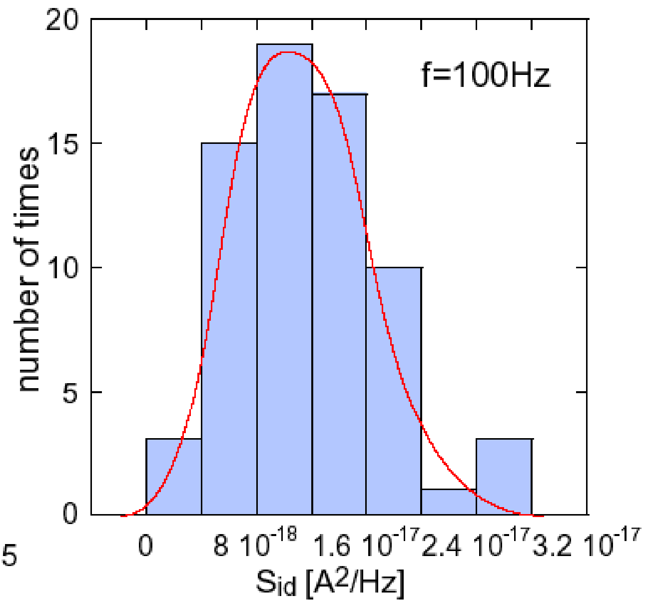
1/fノイズ特性

1/fノイズの起源



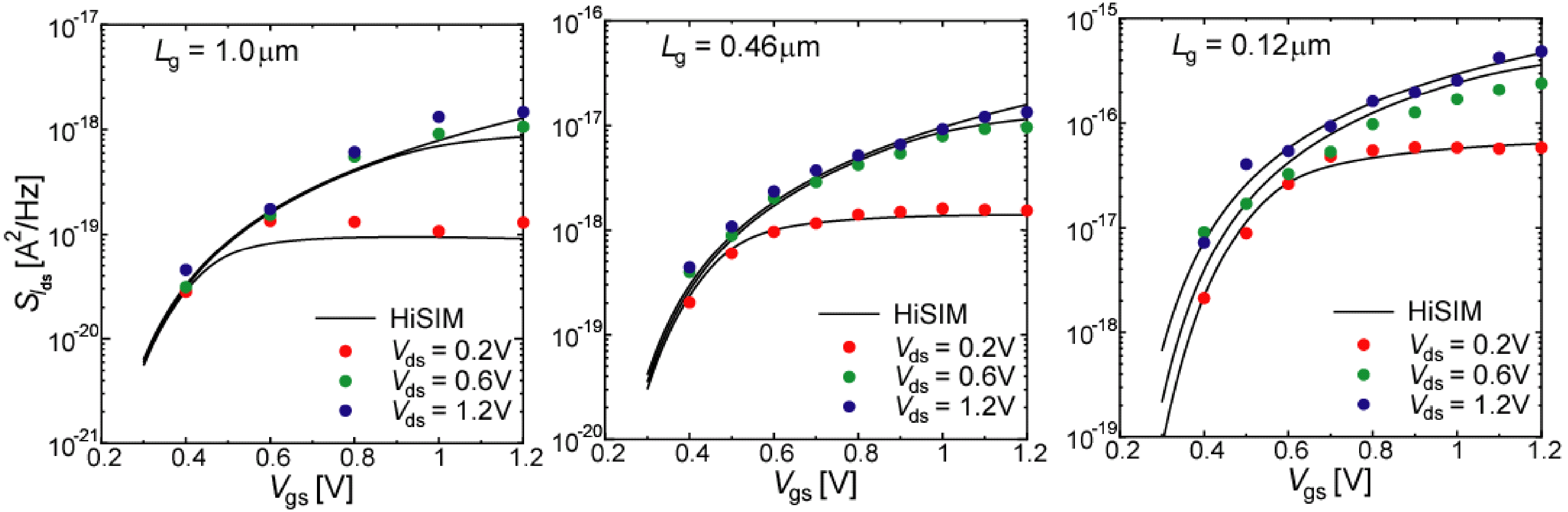
Statistics on a Wafer





Homogeneous Distribution

Comparison with Measurements



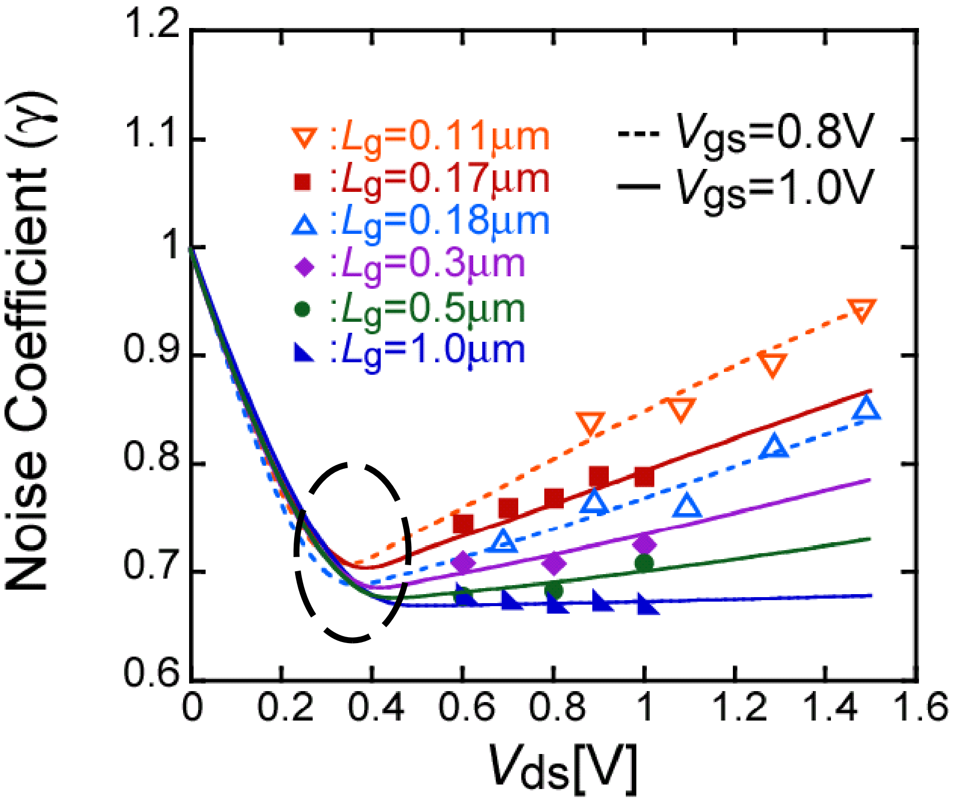
- N_{trap} is fitted to measurements.
- If technology is mature, N_{trap} is nearly universal.

➢ ***I*-*V* characteristics determine 1/*f* noise characteristics.**

➢ **1/*f* noise is predictable.**

S. Matsumoto et al., IEIEC T E, E88-C, p. 247, 2005.

Comparison with Measurements



Lines: Simulation (HiSIM)
Symbols: Measurements

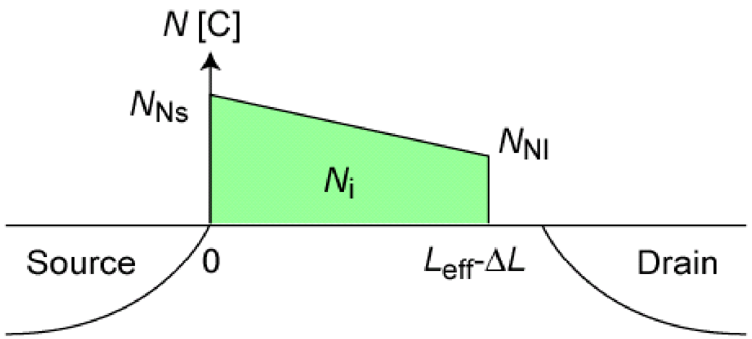
- **First γ Reduction and Increase in the Saturation Region**
- **No Drastic Increase of γ**
- **γ Minimum Increase from 2/3**

Origin of γ Increase → Potential Increase → Mobility Reduction

S. Hosokawa et al., Appl. Phys. Lett., p. 87, 2005.

Model Equation

$$S_{I_{ds}}(f) = \frac{W_g N_t}{q L_g^2 \eta f} kT \int_0^{L-\Delta L} \left(\frac{I_{ds}}{W_g}\right)^2 \left(\frac{1}{N(x)} \pm \alpha\mu\right)^2 dx$$



↓

$$S_{I_d}(f) = \frac{(L-\Delta L)}{L^2}\frac{I_{ds}^2}{W}\frac{N_t(E_f)}{q\eta f} kT \left\{ \frac{1}{(N_s+N^*)(N_1+N^*)} + \frac{2\alpha\mu}{N_1 - N_s}\log\left(\frac{N_1+N^*}{N_s+N^*}\right) + (\alpha\mu)^2 \right\}$$

$$N^* = \frac{C_{ox}+C_{dep}+CIT}{q\beta}$$

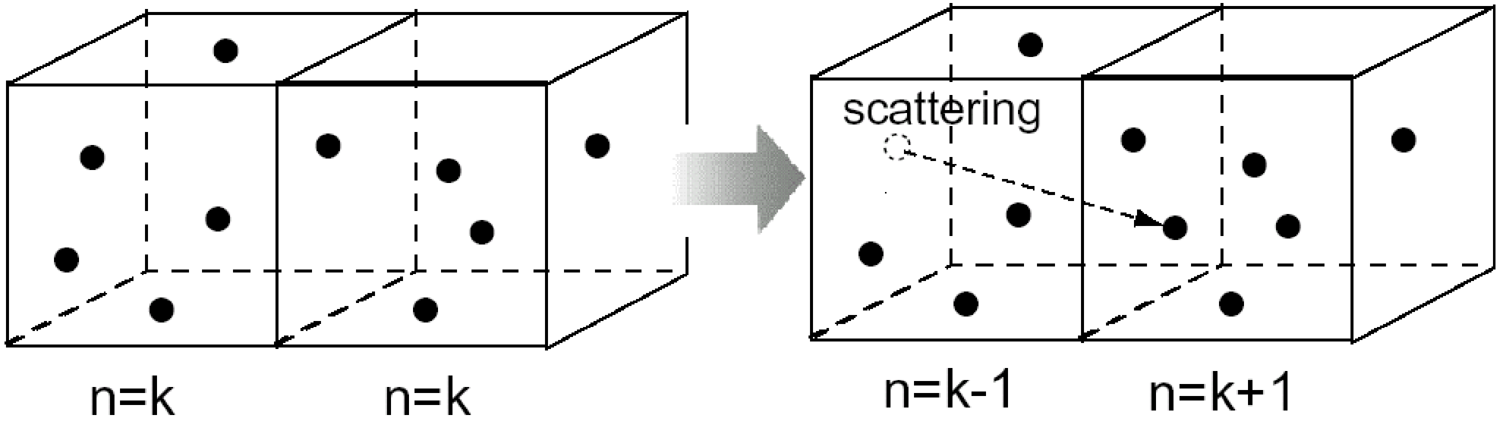
Model Parameters

Trap Density: $N_{trap} = N_t(E_f)/\eta \quad [eV^{-1}cm^{-3}][cm] = [eV^{-1}cm^{-2}]$

Scattering Coeff.: $\alpha \quad [Vs]$

Capacitance Change: $CIT \simeq 0$

Origin of the Thermal Noise



van der Ziel Equation based on Nyquist Theorem:

$$S_{\mathrm{id}} = \frac{4kT}{L_{\mathrm{eff}}{}^{2} I_{\mathrm{ds}}} \int g_{\mathrm{ds}}{}^{2}(y)dy$$

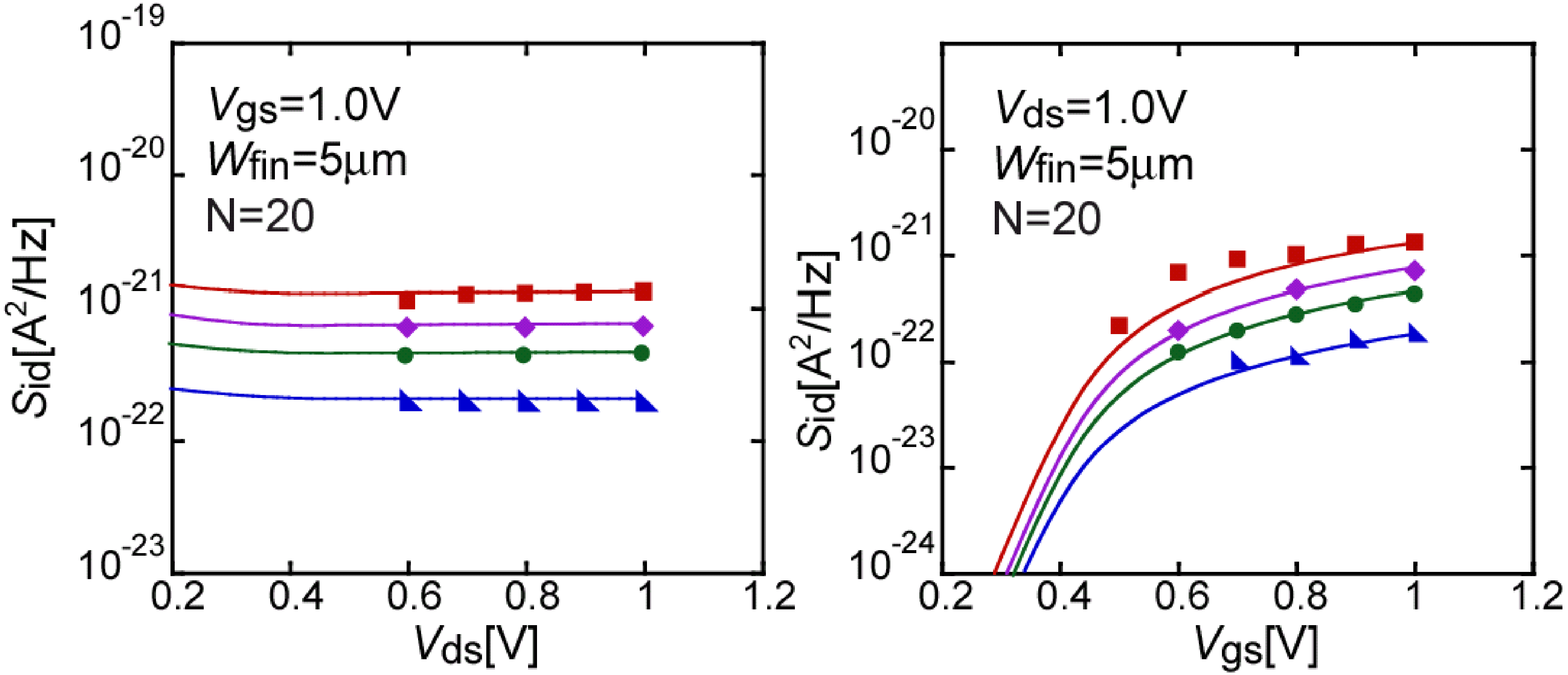
$$= 4kTg_{\mathrm{ds0}}\gamma$$

g_{ds}(y): Channel Conductance

g_{ds0}: at V_{ds}=0

γ: Noise Coefficient

Comparison with Measurements

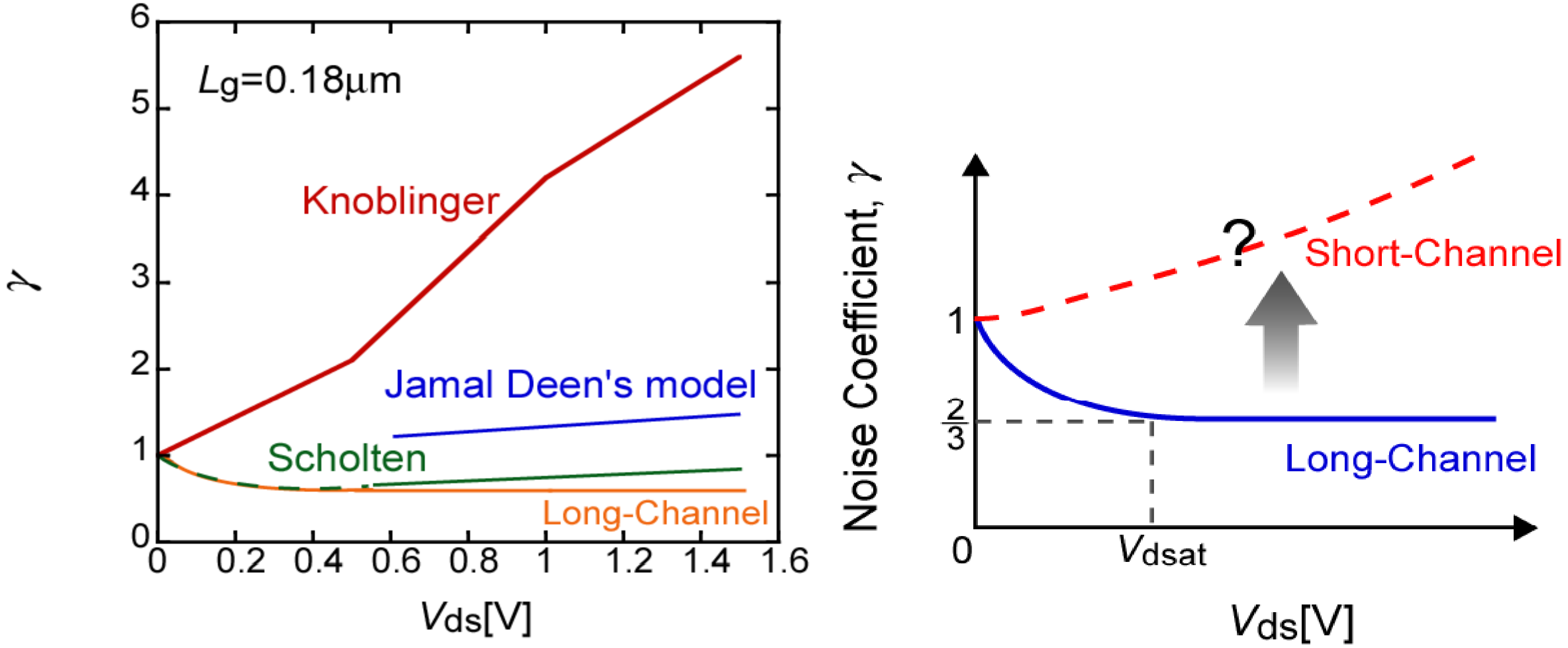


Lines: HiSIM

Symbols: Measurements

No Additional Model Parameters

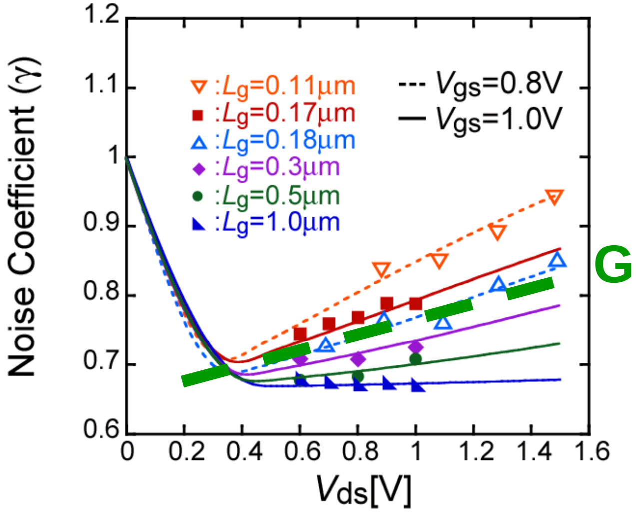
Noise Coefficient (γ) of Short Channels



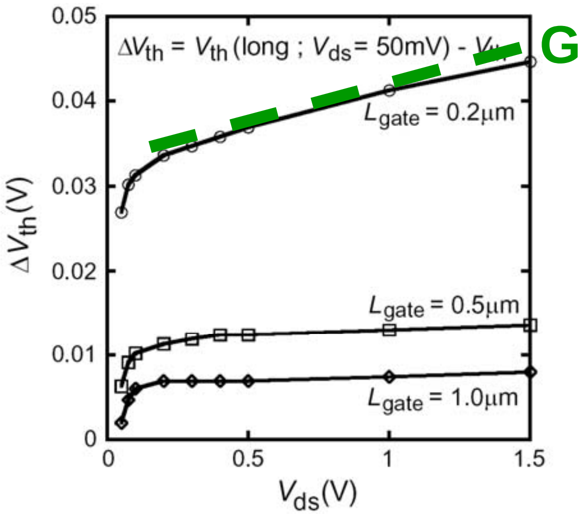
Different Explanations

- **Knoblinger et al. (2001): Hot Electron Contribution**
- **Jamal Deen et al. (2002): Channel Length Modulation**
- **Scholten et al. (2002): Velocity Saturation**

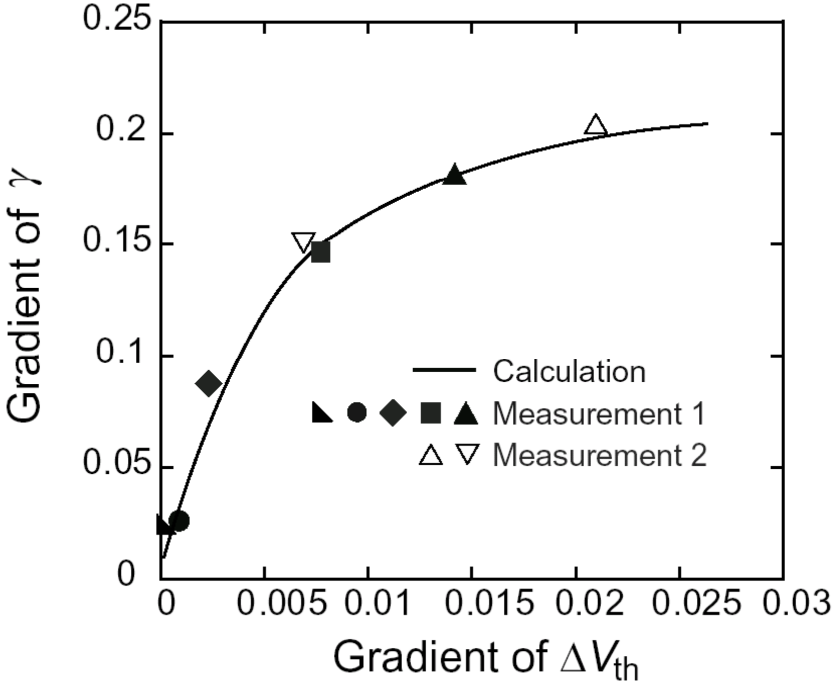
Comparison with V_{th} Shift



Grad. γ

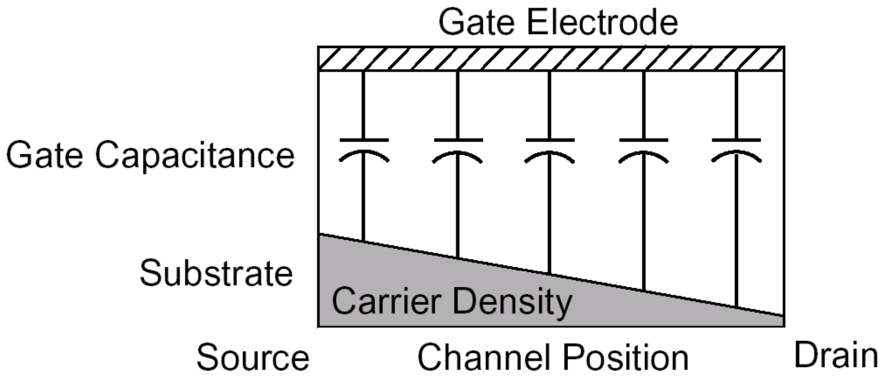


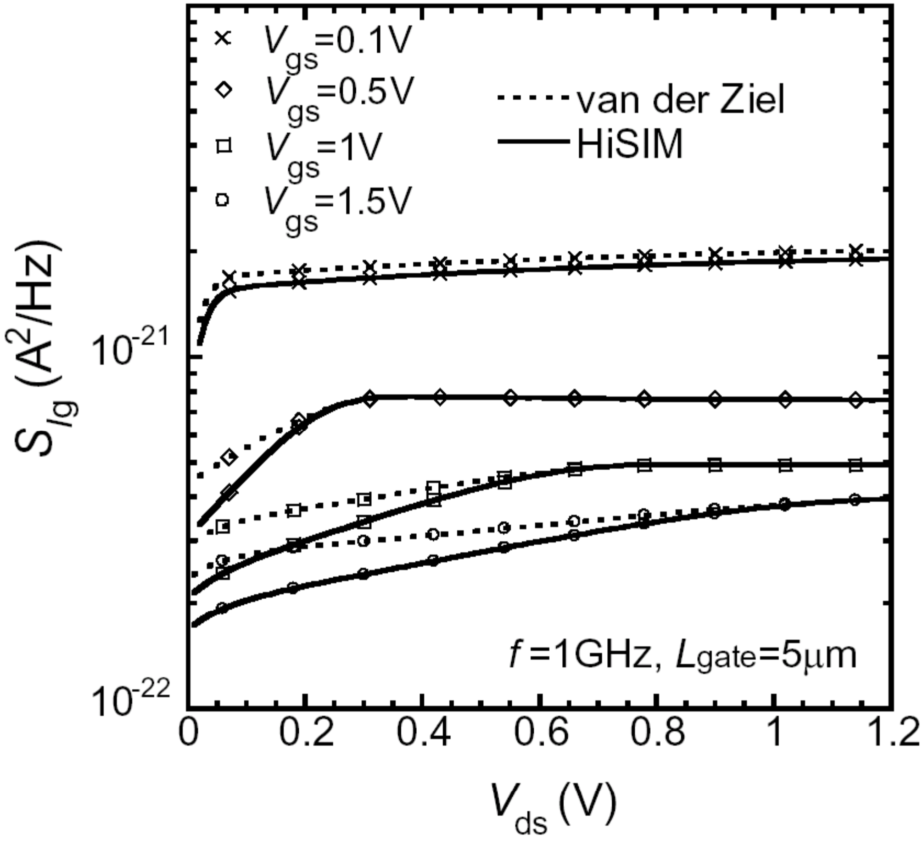
Grad. ΔV_{th}



Universal Relationship

Induced Gate Noise & Cross-Correlation Noise

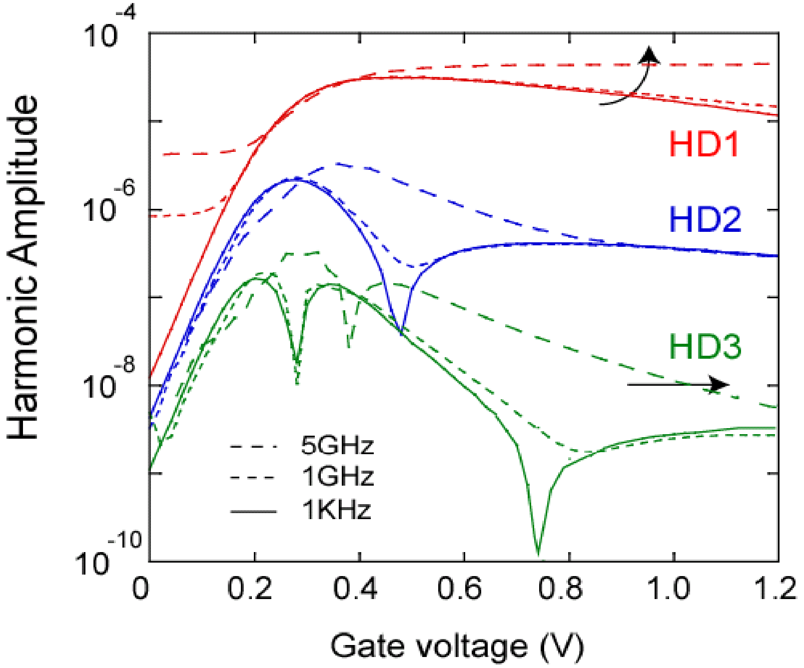


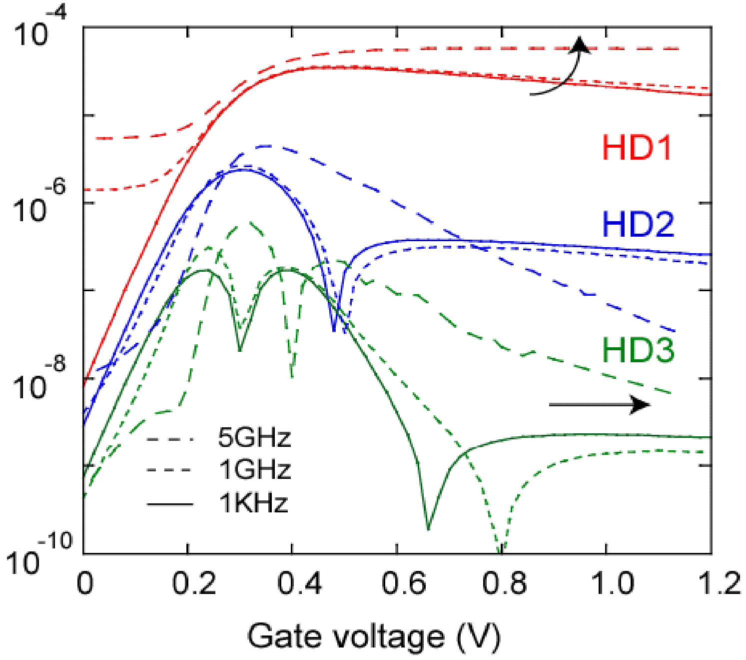


Potential distribution along the channel is responsible.
No Additional Model Parameters

T. Warabino et al., Proc. SISPAD, 2006.

Harmonic Distortion under High Frequency


HiSIM-NQS

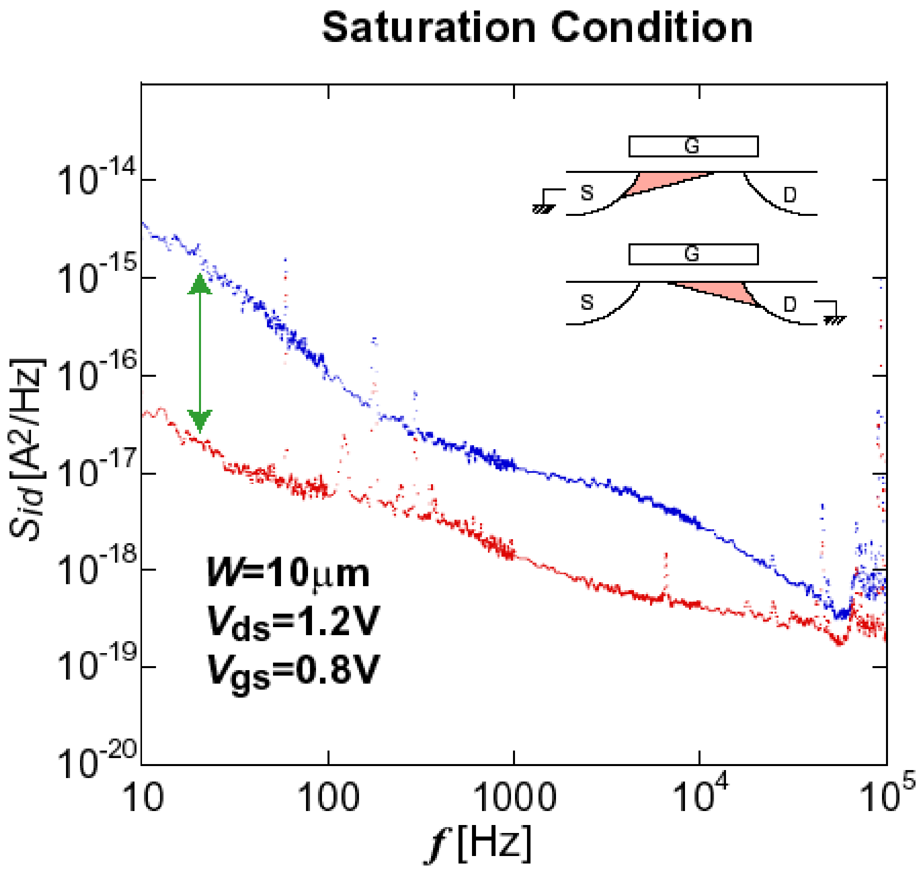

2D Device Simulator

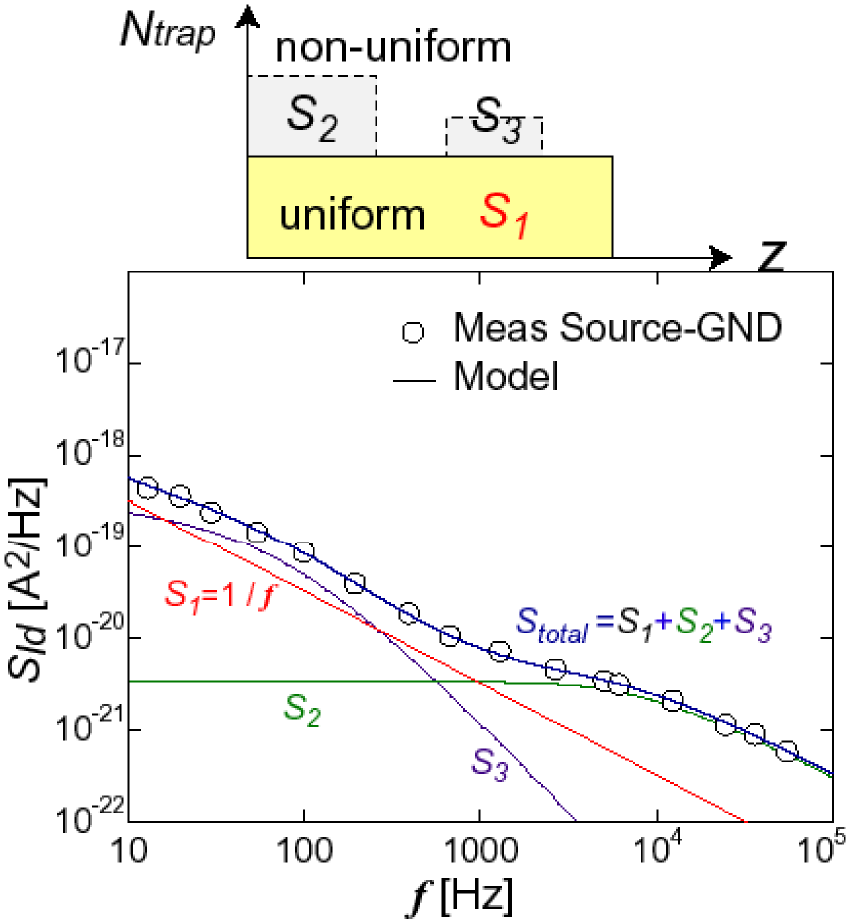
Carrier transit delay dominates the HD characteristics.

D. Navarro et al., IEEE T ED, Sept., 2006.

1/fノイズ特性からのずれ

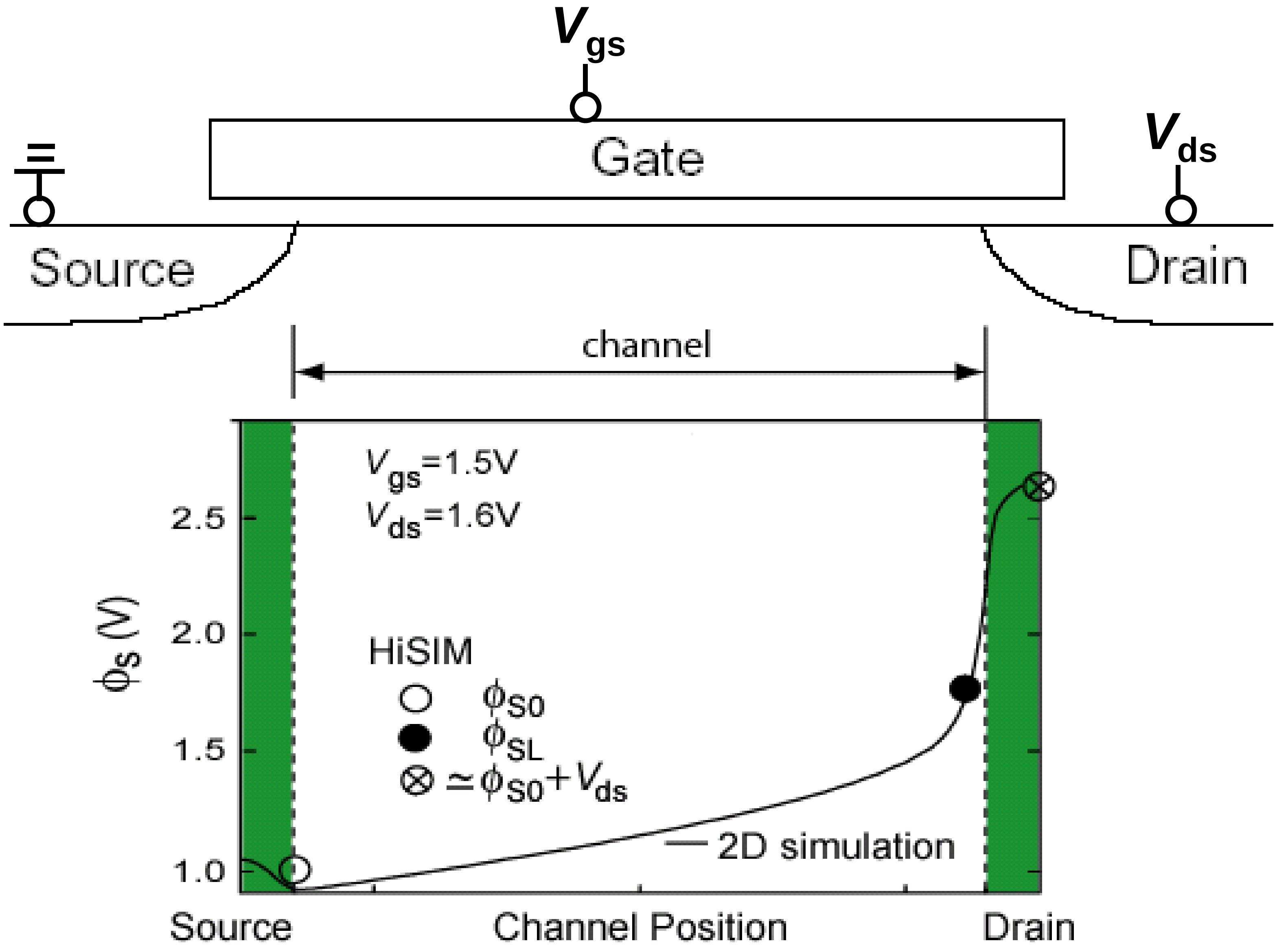
L_g=0.13μm (nMOSFET)





Intra-Chipばらつきの原因？

表面ポテンシャル


V_{gs}
Gate
V_{ds}
Source
Drain
channel
V_{gs}=1.5V
V_{ds}=1.6V
HiSIM
○ ϕ_{S0}
● ϕ_{SL}
⊗ $\simeq \phi_{S0}+V_{ds}$
— 2D simulation
2.5
2.0
1.5
1.0
ϕ_S (V)
Source
Channel Position
Drain