Statistical Reliability Effects

Scaling Trend, Modeling, and Characterization

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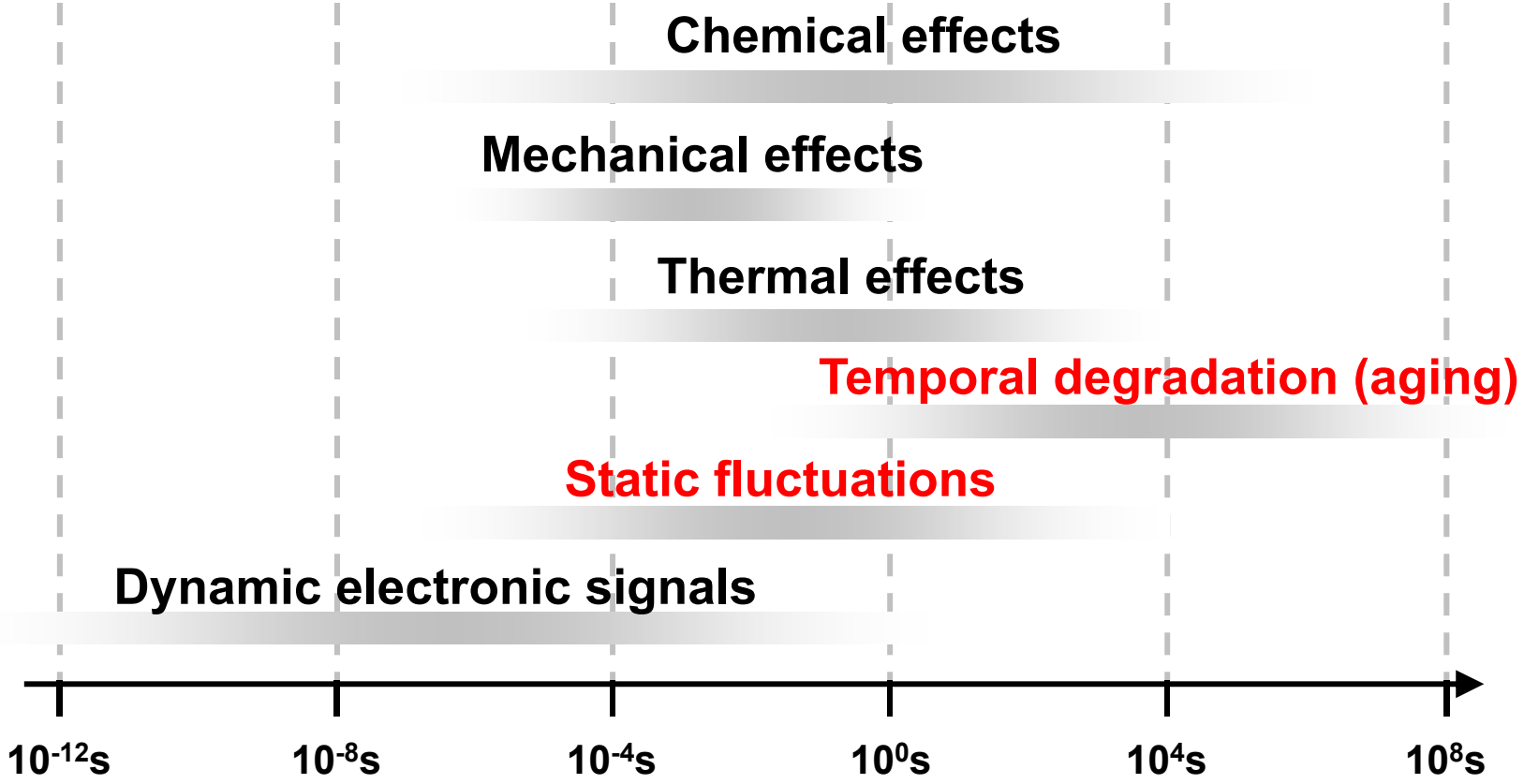
Increased Reliability Concerns

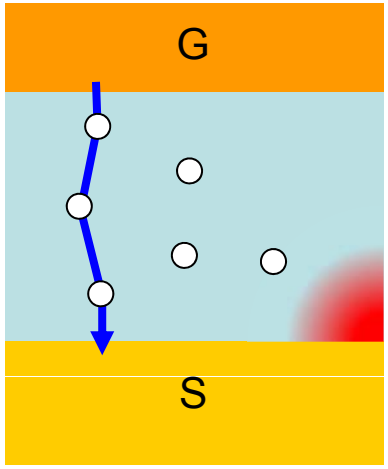
- An inevitable result of aggressive scaling
  - No convenient solution from CMOS technology!



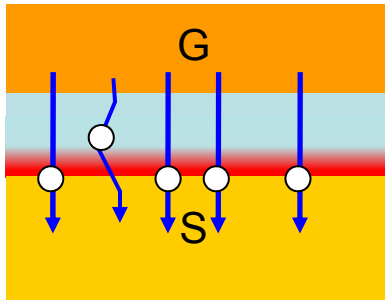
[M. Kole, BMAS 2007]

Changing Scenario with Thin T_{ox}

- Hot carrier effect
  - NMOS in the saturation region
  - Close to the drain
  - Related to the switching



- **Bias temperature instability**
  - NBTI for PMOS in the inversion mode (weaker PBTI in NMOS)
  - Uniform in the channel
  - Happens at the standby

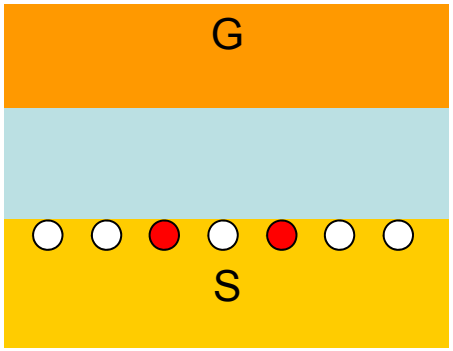


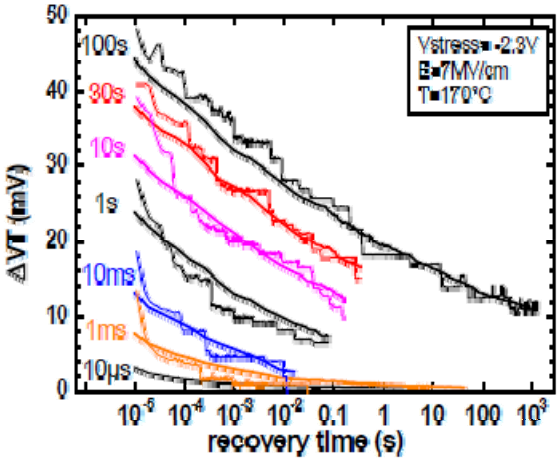
- Hard oxide breakdown
  - Sudden I_{gate} change, hard failure
  - Multiple oxide charges
  - A stochastic process

- **Soft oxide breakdown**
  - Gradual increase of I_{gate}
  - More with interface traps
  - Correlated with other aging effects

Impact on Reliability Analysis

- Atom level: Discrete, intrinsically statistical

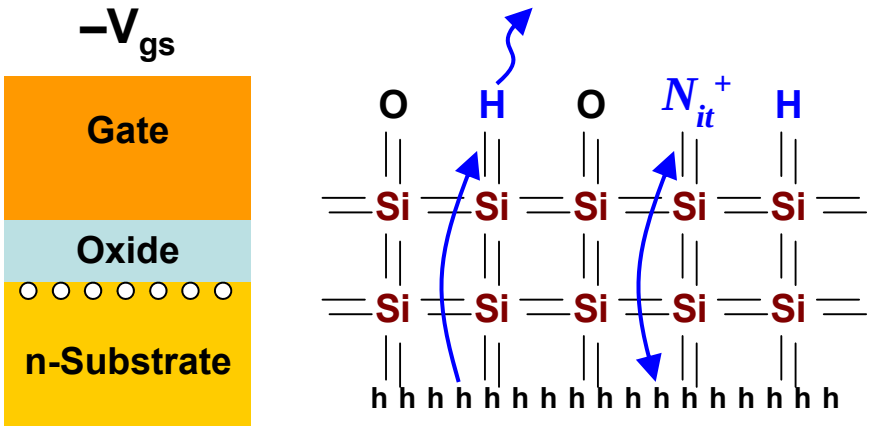


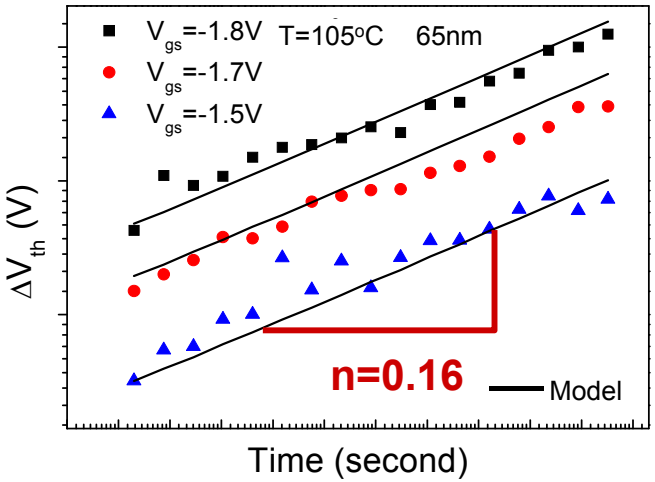


- **Device level**
  - Compact models of temporal parameter shift
  - Dependence on process variations
- **Circuit level**
  - Statistical interaction with dynamic operations
  - In-situ characterization techniques

[H. Reisinger, et al., IRPS 2010]

NBTI: Static Stress

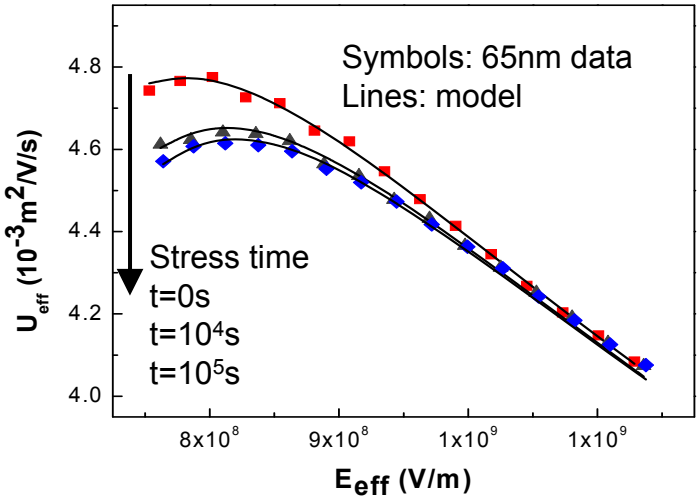




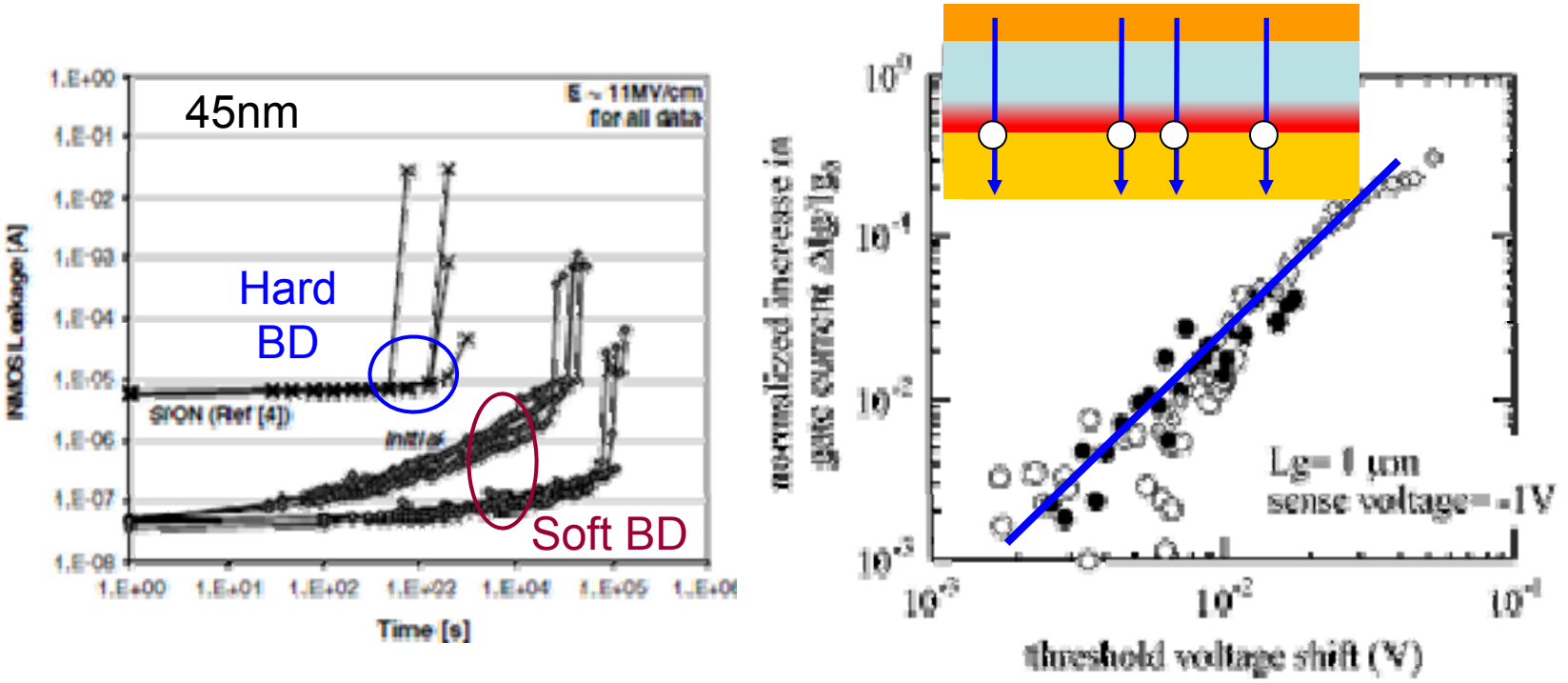
$$\Delta V_{th} = A\left[(1+\delta)t_{ox} + \sqrt{Ct}\right]^{2n}$$

$$A \to Q_i \exp\left(\frac{E_{ox}}{E_0}\right) \qquad C \to \exp\left(-\frac{E_a}{kT}\right)$$

- A mixture of trapping/detrapping and reaction/diffusion, affecting V_{th} and μ



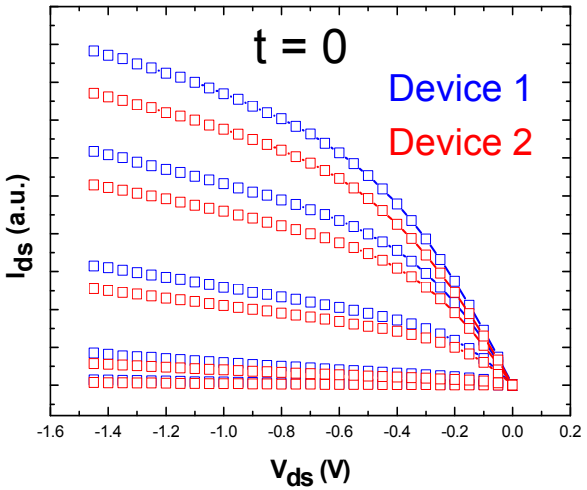
Correlation with TDDB?



- Direct tunneling dominates I_{gate} in a thin T_{ox} device
- Interface charges control both V_{th} shift and I_{gate} change
- Modeling of such correlation reduces design margin

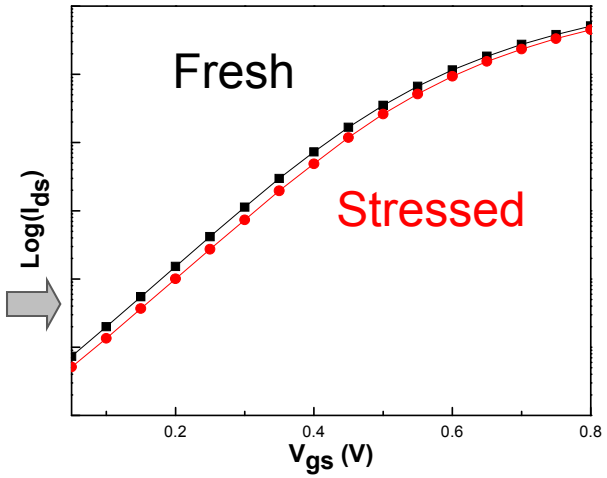
[J. Hicks, et al., Intel, 2008; S. Tsujikawa, TED 2006]

Statistical Silicon Validation



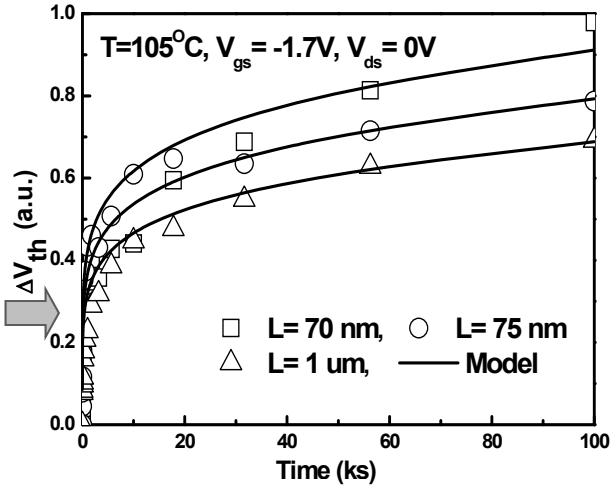
Decouple variations

(V_{th}, L, μ, etc.)



Extract the degradation

(V_{th} from $I_{leakage}$, μ from I_{linear})

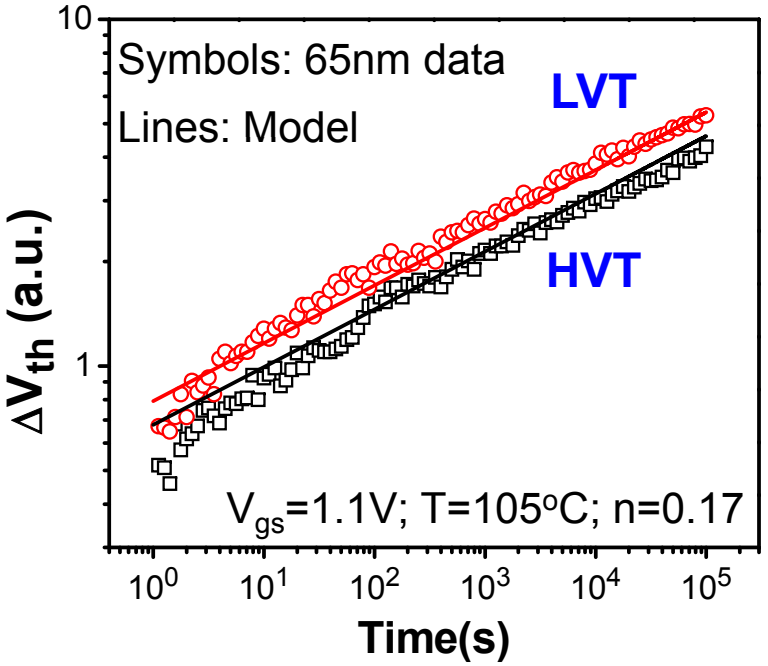


Reliability model

- Only 5-6 model parameters need to be extracted
- Reliability model is scalable with primary process and design parameters

Dependence on V_{th} Variation

	ΔV_{th} (t=0) (%)	ΔV_{th} (t=10^5s) (%)
1	**12.03**	**5.43**
2	2.85	3.51
3	-6.75	8.02
4	**-8.14**	**18.26**



$$\Delta V_{th} \propto Q_i \exp\left(E_{ox}/E_0\right)$$

$$Q_i \propto C_{ox}\left(V_{gs} - V_{th}\right)$$

$$E_{ox} \propto V_{gs}/T_{ox}$$

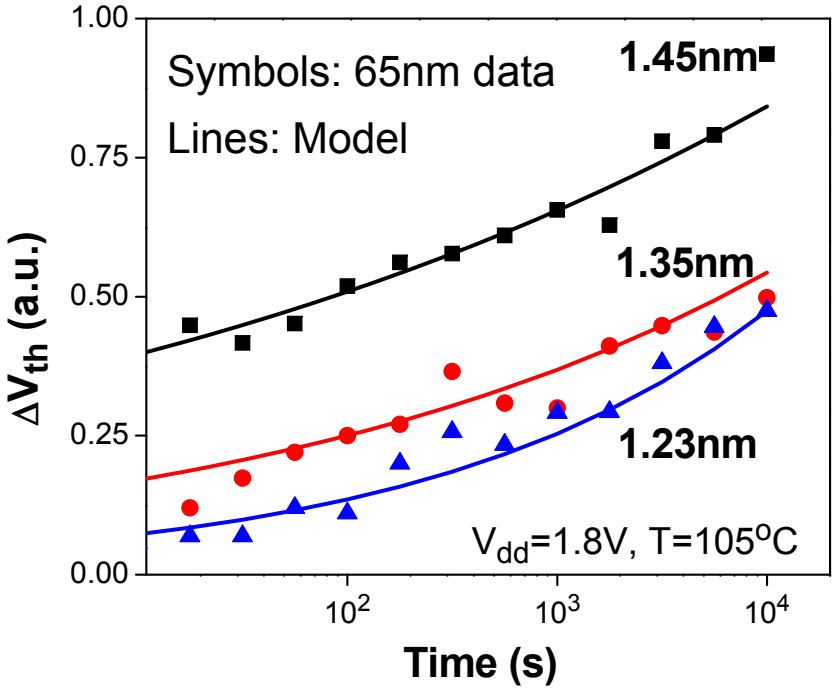
- Aging is a linear function of V_{th}
- It is **negatively correlated** with V_{th} shift, compensating initial process variations in V_{th}

Dependence on T_{ox} Variation

$$\Delta V_{th} \propto Q_i \exp\left(E_{ox}/E_0\right)$$

$$Q_i \propto C_{ox}\left(V_{gs} - V_{th}\right)$$

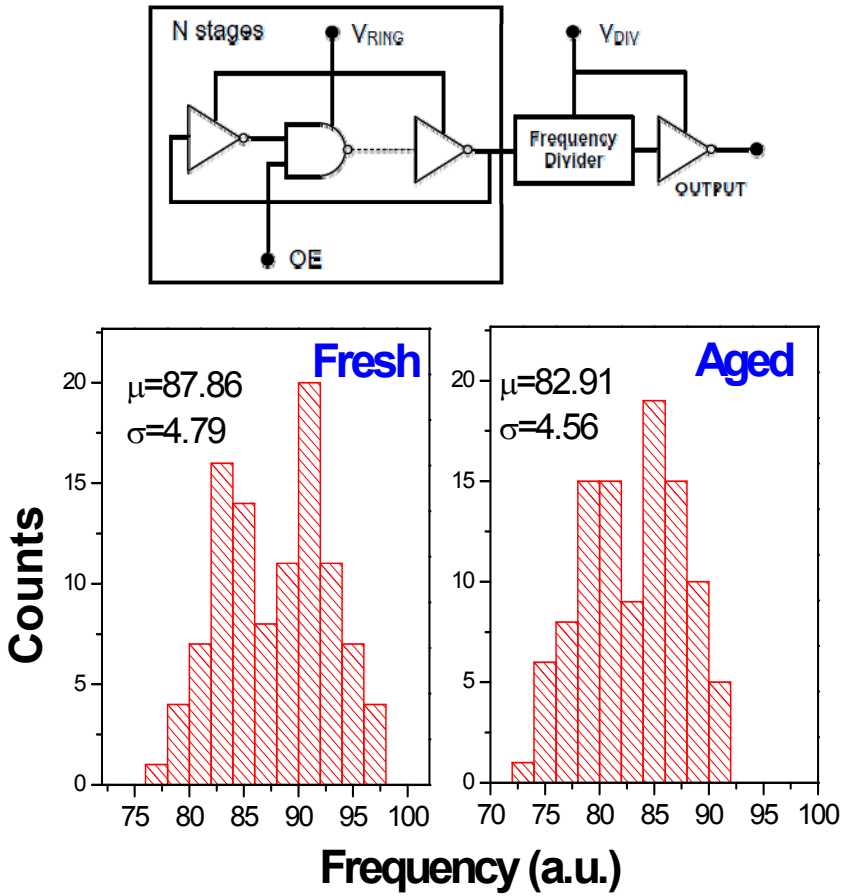
$$E_{ox} \propto V_{gs}/T_{ox}$$



- Aging is highly sensitive to T_{ox} variation
  - Such an exponential dependence helps extract T_{ox} from the aging rate
  - Again, aging effect is **negatively correlated** with T_{ox} variation
- Aging effect could be exploited to reduce process variations
  - But the required annealing time is too long

Statistics of RO Frequency

100 ROs at 65nm



$$f_{i\_0} \propto V_{dd} - V_{thi\_0}$$

$$\Delta f_i \propto -\Delta V_{thi}$$
$$\propto -\left(V_{dd} - V_{thi\_0}\right)$$

$$f_i = f_{i\_0} + \Delta f_i$$
$$\propto \left(1 - At^n\right) \cdot \left(V_{dd} - V_{thi\_0}\right)$$

- RO speed variability is mainly due to V_{th} variations

Aging of RO Mean and STD

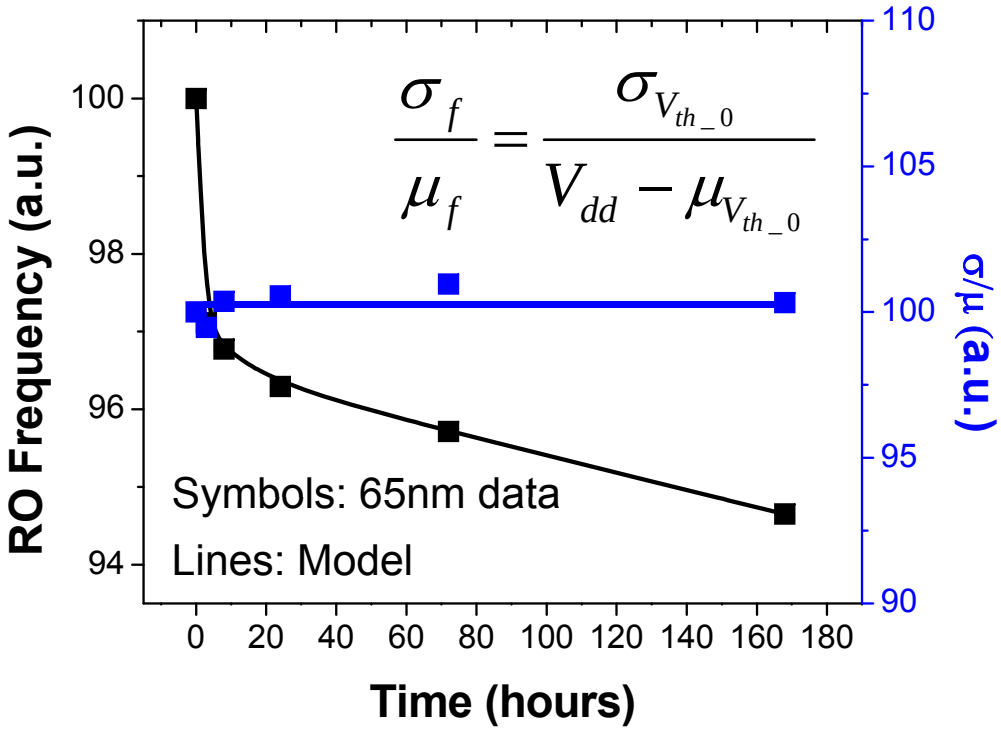
$$f_i = f_{i\_0} + \Delta f_i$$
$$\propto \left(1 - At^n\right) \cdot \left(V_{dd} - V_{thi\_0}\right)$$

Mean :

$$\mu_f \propto \left(1 - At^n\right) \cdot \left(V_{dd} - \mu_{V_{th\_0}}\right)$$

Standard Deviation :

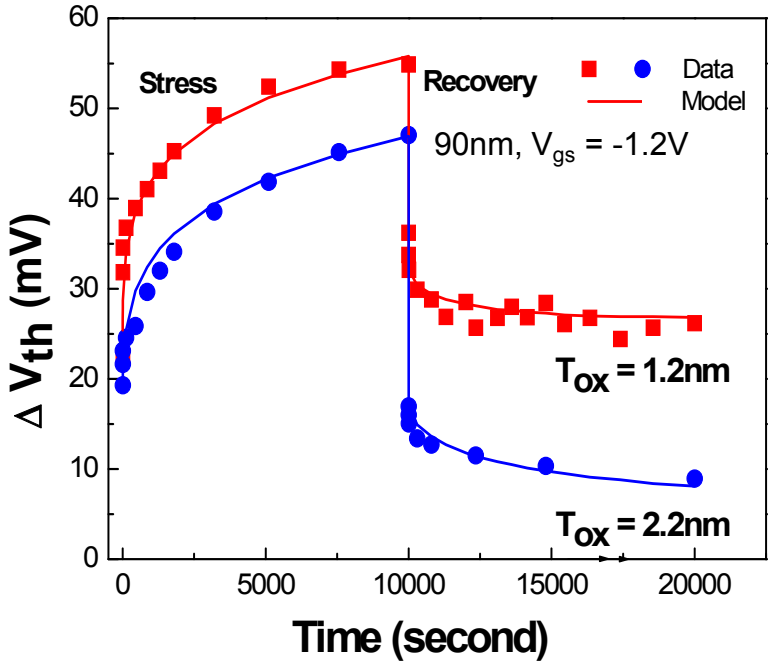
$$\sigma_f \propto \left(1 - At^n\right) \cdot \sigma_{V_{th\_0}}$$



- The mean shift follows the power law of time, while σ decreases with the stress time (at the same rate)
- **σ/μ stays the same** under the stress!

NBTI: Dynamic Effect

- A unique property of NBTI: recoverable when V_{gs}=0
- Consequently, the long-term degradation depends on duty cycle, i.e., the ratio of stress time in a clock cycle



Stress

$$\Delta V_{th} = \left[K_v \left(t - t_0\right)^{0.5} + \sqrt[2n]{\Delta V_{th0}}\right]^{2n}$$

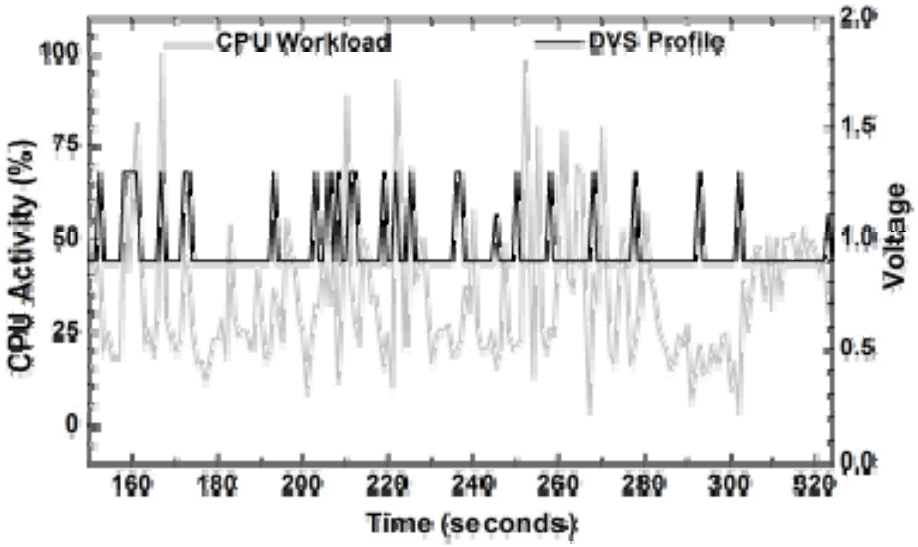
$$K_v \to Q_i \sqrt{\exp\left(-\frac{E_a}{kT}\right)}\left(\exp\left(\frac{E_{ox}}{E_0}\right)\right)^2$$

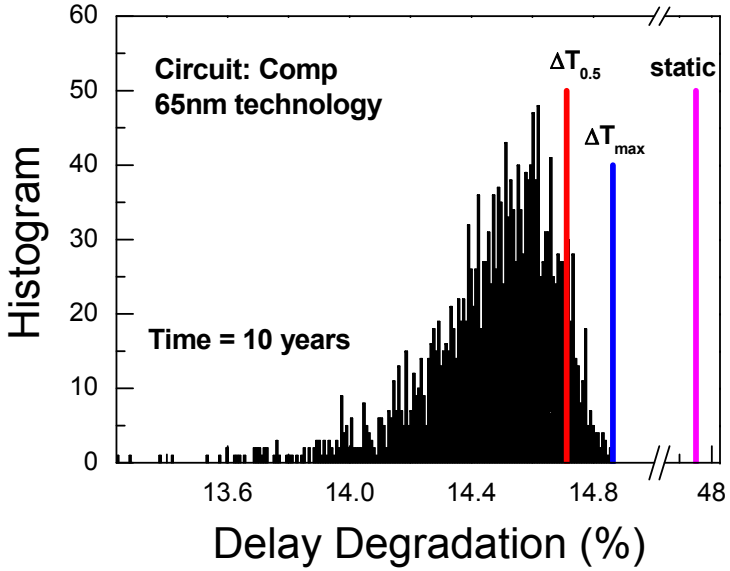
Recovery

$$\Delta V_{th} = \Delta V_{th0}\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 \cdot C \cdot \left(t - t_0\right)}}{2t_{ox} + \sqrt{C \cdot t}}\right)$$

Aging under Dynamic Operations

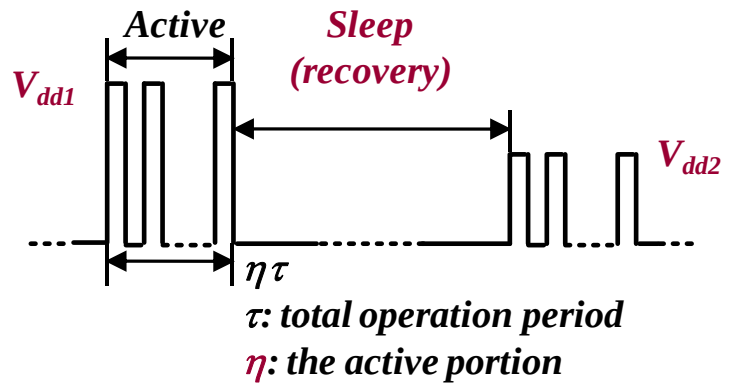
- Realistic circuit operations are statistical:
  - Multiple V_{dd}, such as dynamic voltage scaling (DVS)
  - Sleep mode (V_{dd} off): long recovery phase, no stress
  - Random duty cycle at each node



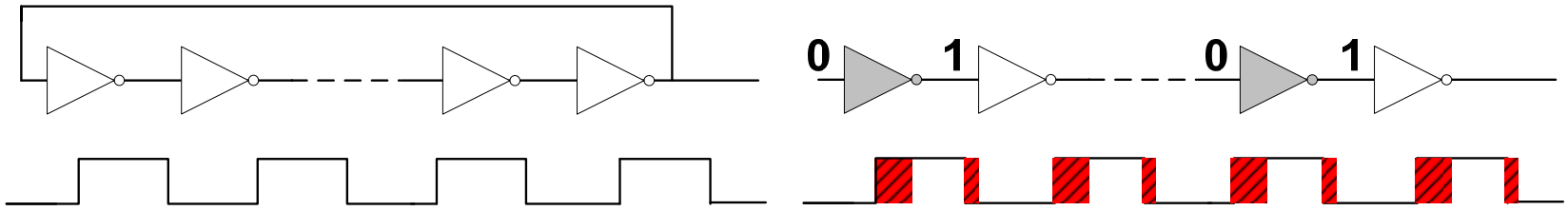


Gaps in Reliability Test

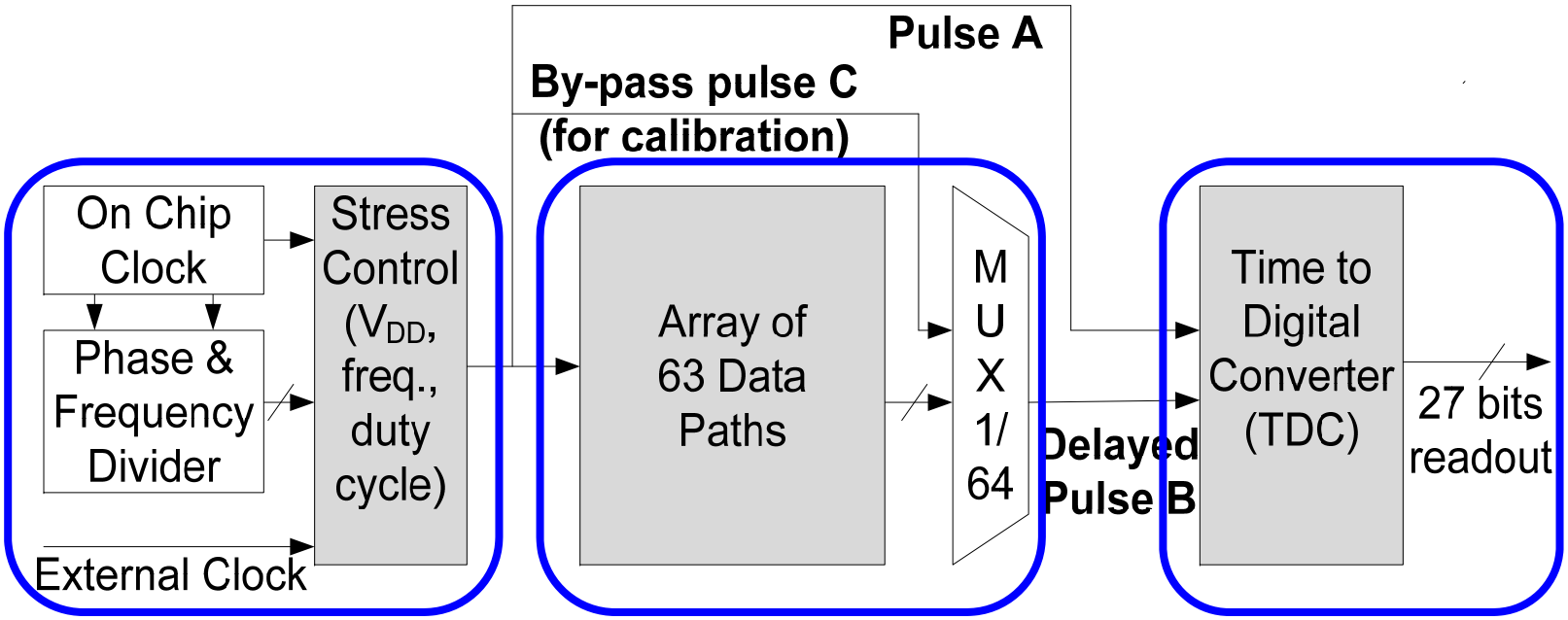
- Traditional RO based structure is incapable to capture:
  - Dynamic operation conditions: duty cycle (fixed at 50% in a RO), voltage, and their sequence



  - Sensitivity to the rising/falling edge; Such unsymmetrical stress is important for today's high performance synchronous design



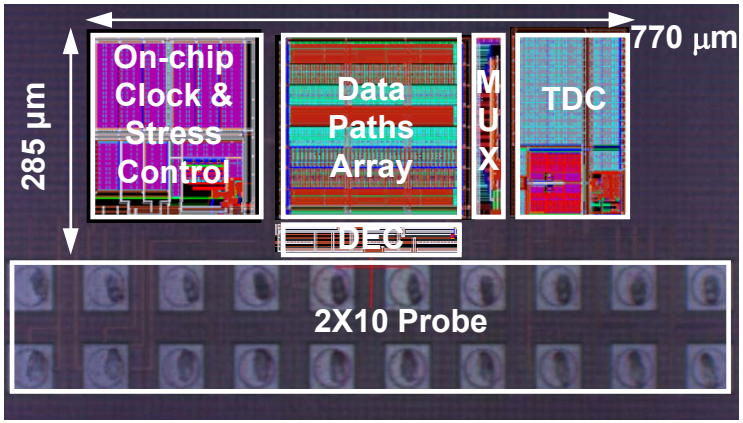
A Generic Test Platform



- On-chip clock and stress control:

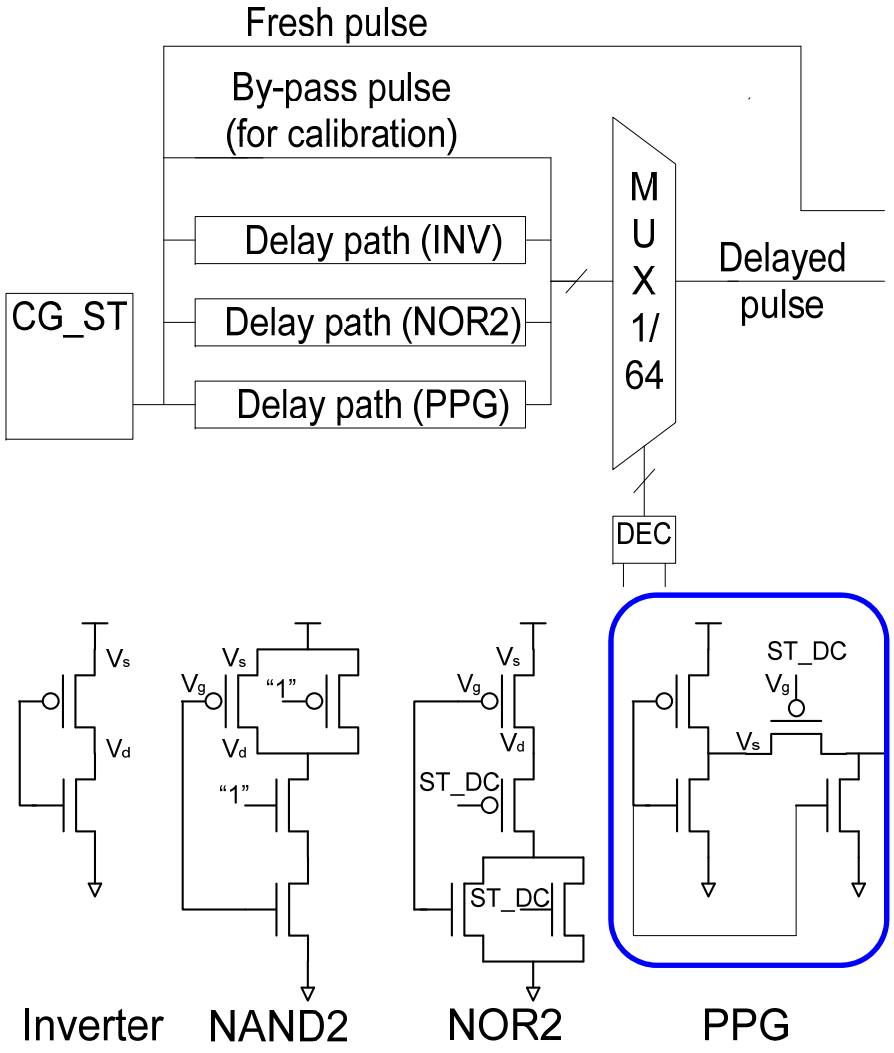
  10% to 90% duty cycle, 680MHz – 1.23 GHz, control of stress V_{DD} and temperature
- Test array: 63 types of data paths
- Time-to-digital converter (TDC):

  Detect delay shift, with 2ps resolution

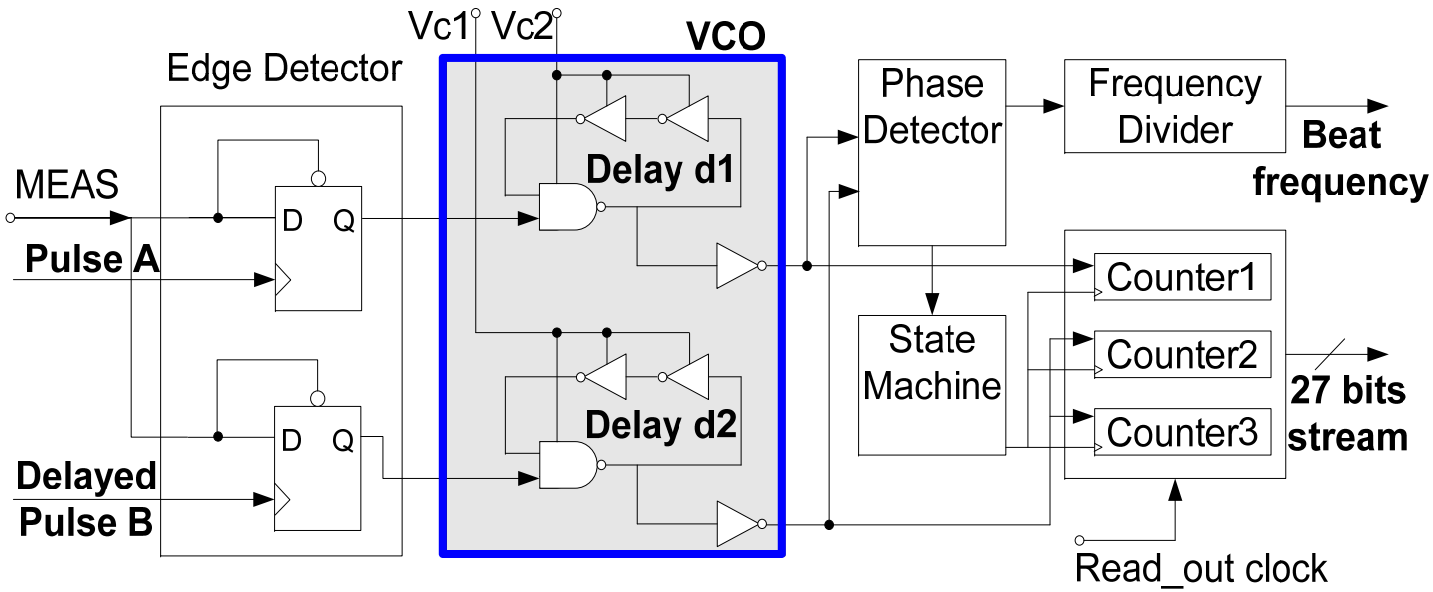


Data Path Array

- Atom level: Test array contains one bypass path for the calibration and 63 data paths
- Three 45nm device types
  - Core device
  - Analog friendly device
  - High-voltage device
- Four circuit structures representing different sensitivities to NBTI
- Fan-out = 1



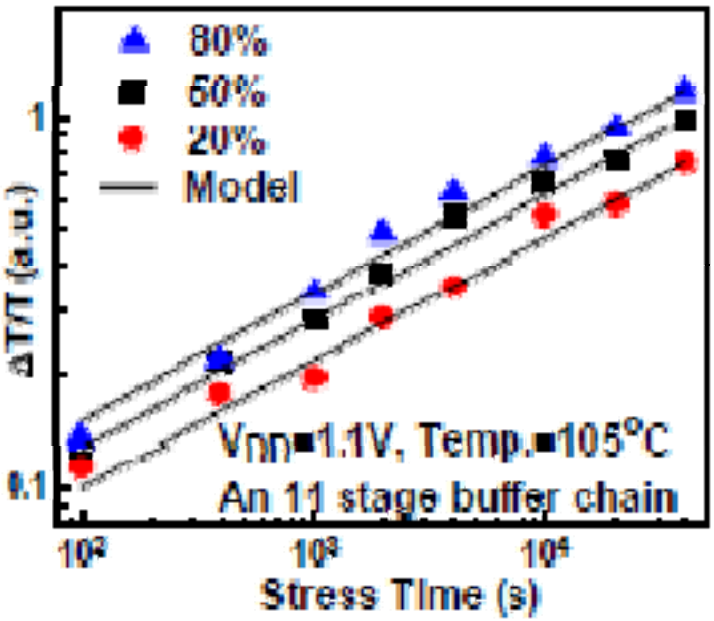
Cyclic TDC Design

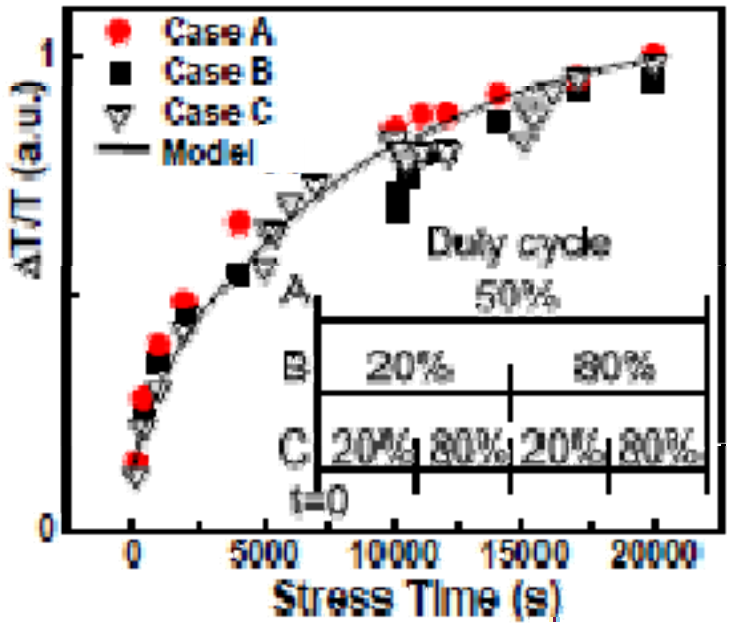


The Vernier ring structure

- A simple and small cyclic structure for easy integration
- Translates delay difference between two signals into digital output
- Oversampling to average random jitter in test circuits
  - 20 times to enhance the resolution to **2ps**, corresponding to **~0.5% delay shift**

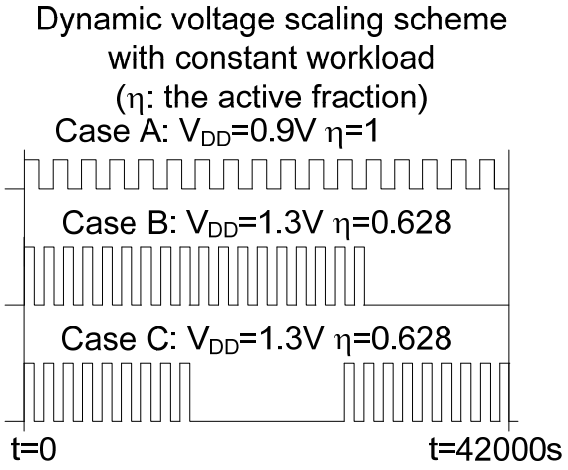
Duty Cycle Dependence



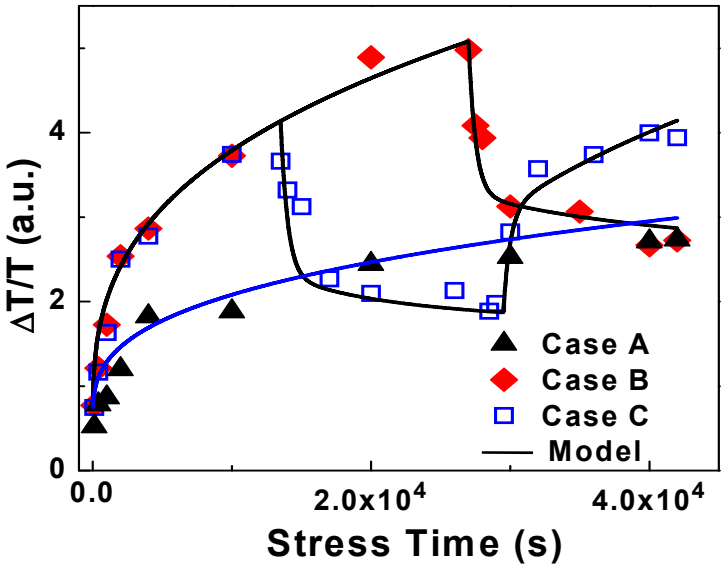


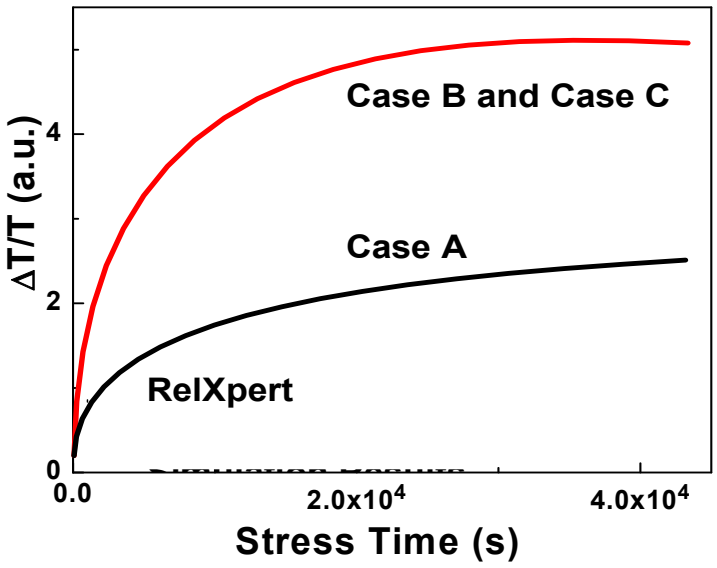
- Higher duty cycle leads to longer stress time and more degradation
- Under constant throughput, the degradation is relatively independent on dynamic sequence of duty cycle
  - Aging is approximately linear to duty cycle, between 10-90%

Dynamic Voltage Scaling



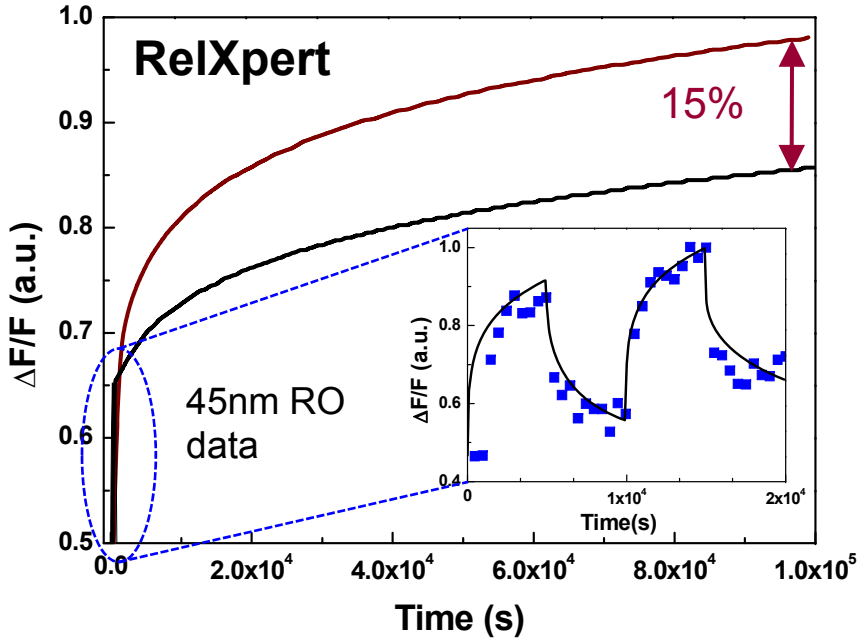
- Aging is highly sensitive to voltage, and its dynamic sequence
- Current reliability tools are only able to handle Case A (constant voltage and duty cycle)

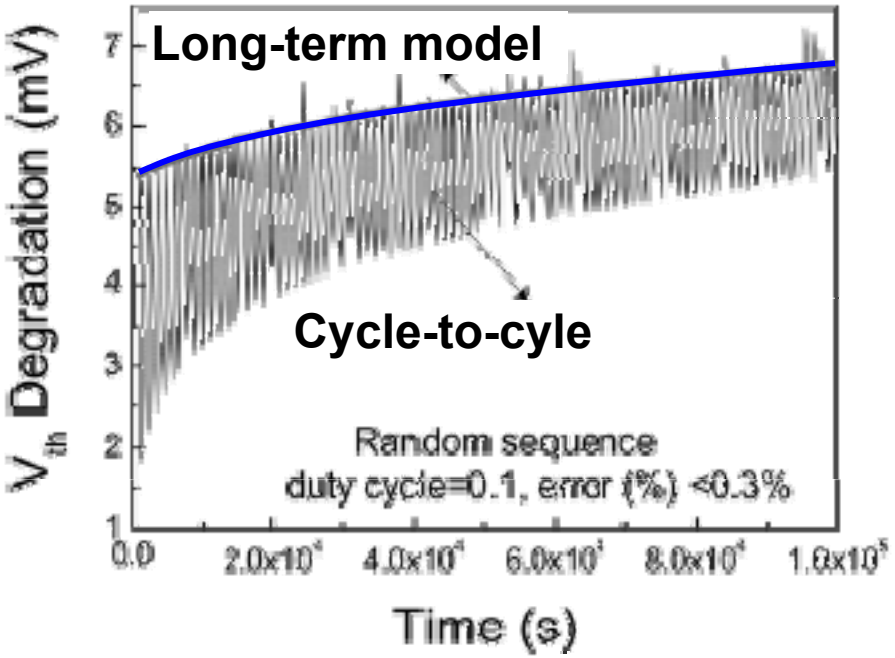




Dynamic Aging Model

- Cycle-to-cycle model: appropriate boundary conditions to connect different periods
- Long-term model: direct calculation assuming averaged design parameters

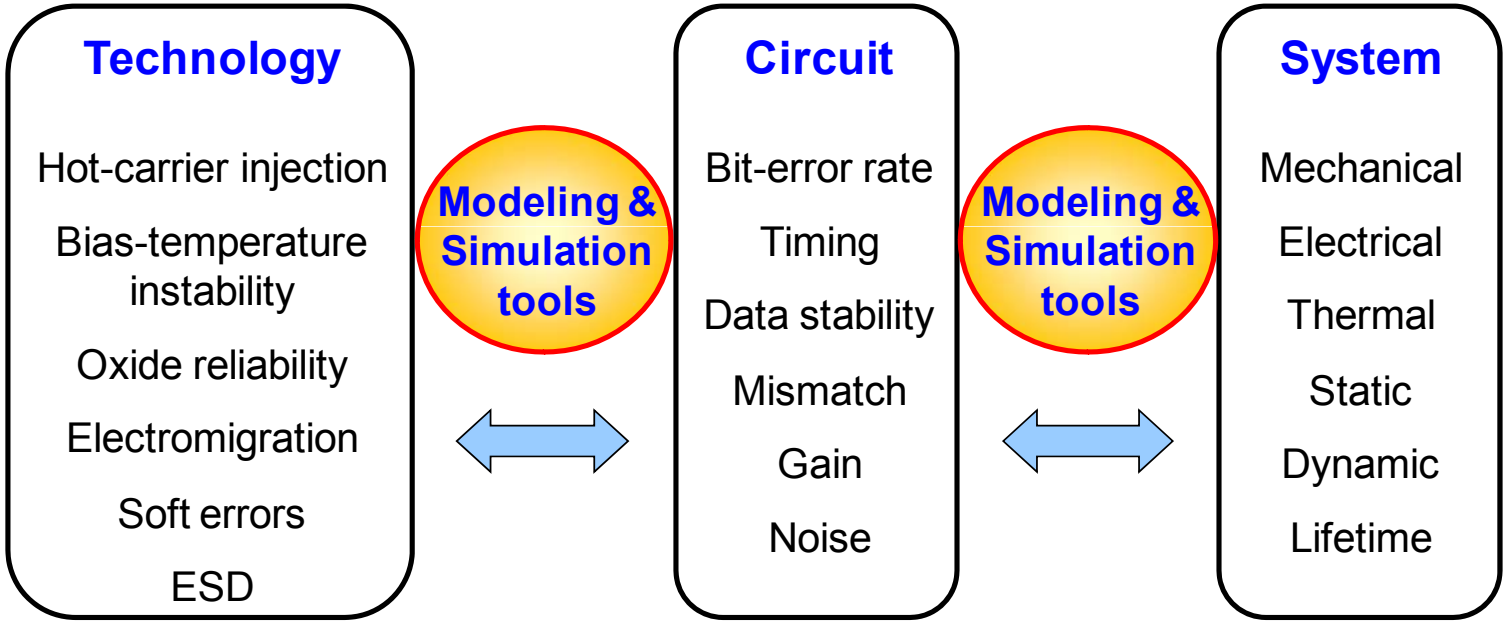




[R. Zhen, et al., CICC 2009]

Summary

- Atom level: modeling of the increased variability
- **Device level**: negative correlation with process variations
- **Circuit level**: a generic test platform for statistical circuit reliability in dynamic operations
- System level: hierarchical integration with VLSI design flow



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