Characterization and modelling of device variability in advanced CMOS technologies

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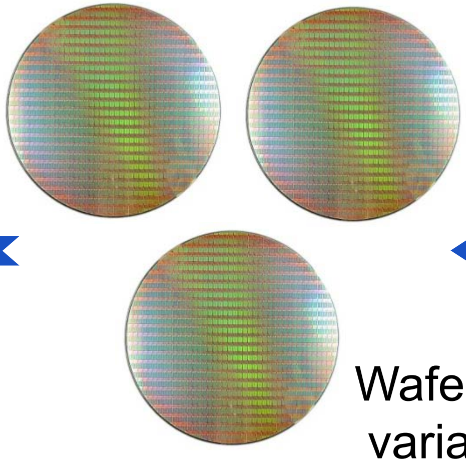
Outline

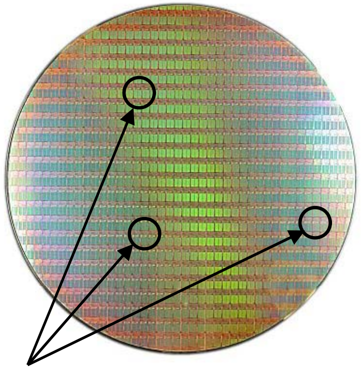
- ☐ **Introduction**
  - What is variability?, importance?
- ☐ **Experimental procedures**
  - Test structures, statistical treatment, measured quantities…
- ☐ **Variability sources and modelling aspects**
  - Channel and pocket issues
  - Polygate influence
- ☐ **Conclusions**
- ☐ **References**

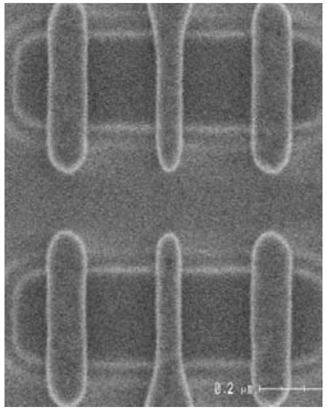
What is variability or mismatch?


Fab to fab variability


Lot to lot variability

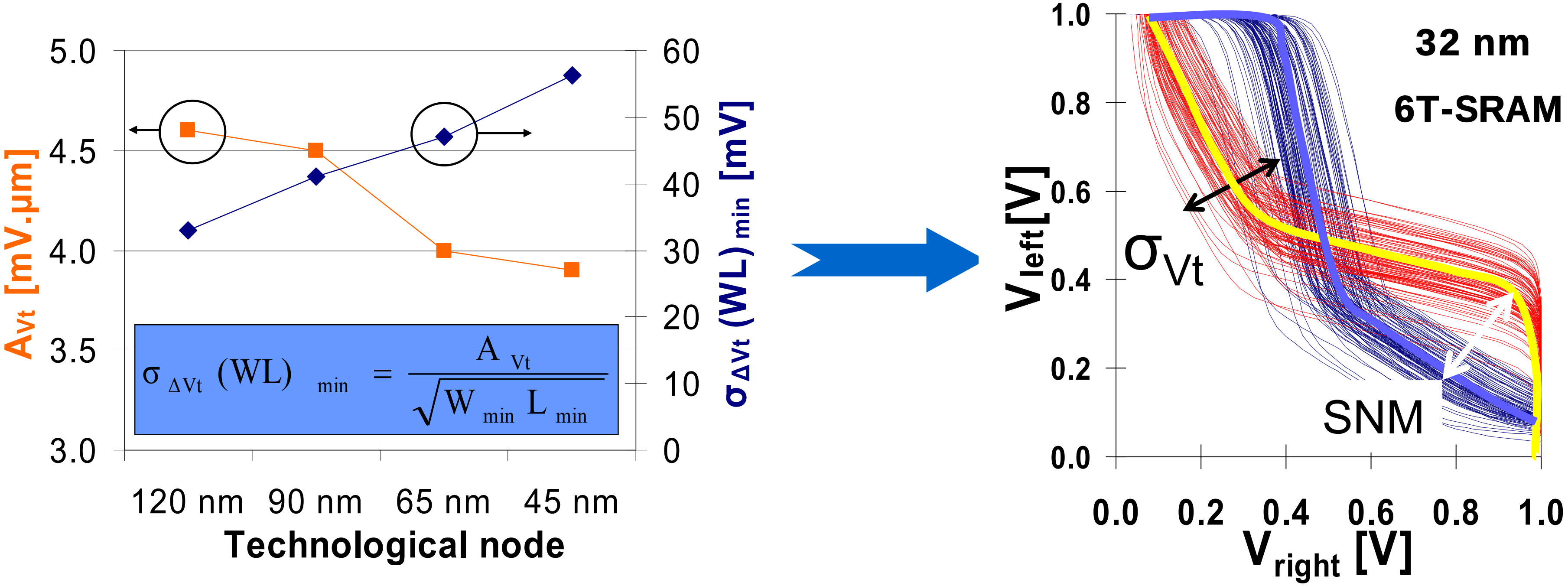

Wafer to wafer variability


Die to die variability



Local variability=
MOS to MOS variability

Importance of Variability



$$\sigma_{\Delta Vt}(WL)_{min} = \frac{A_{Vt}}{\sqrt{W_{min} L_{min}}}$$

- Mismatch critical for analog applications (mirror current, differential amplifier, DAC, ADC...)
- Variability now also affects digital and mixed applications

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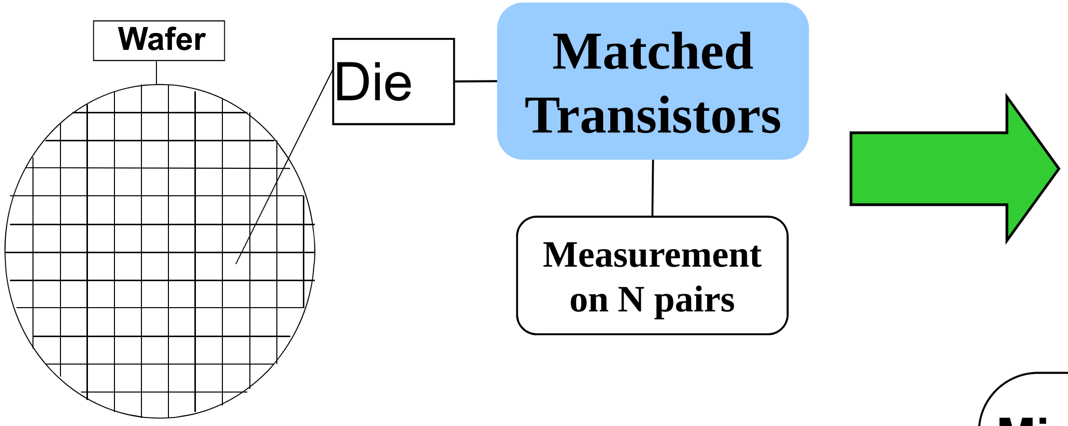
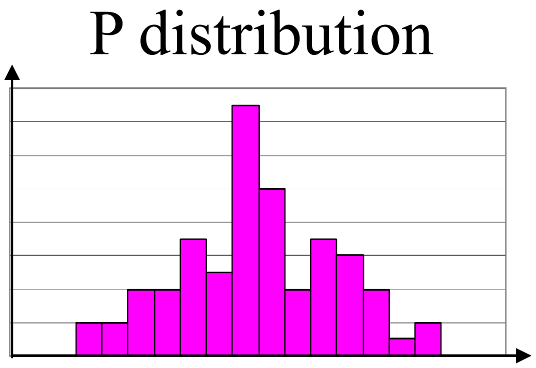
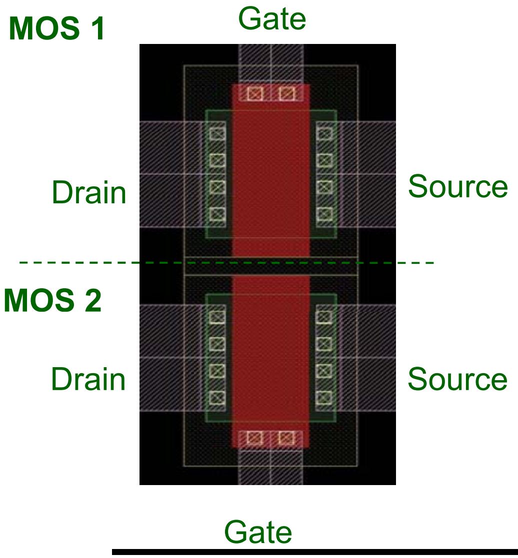
Experimental procedures

- **Matching measurement:**





- **Test Structure:**



Mismatch parameter:

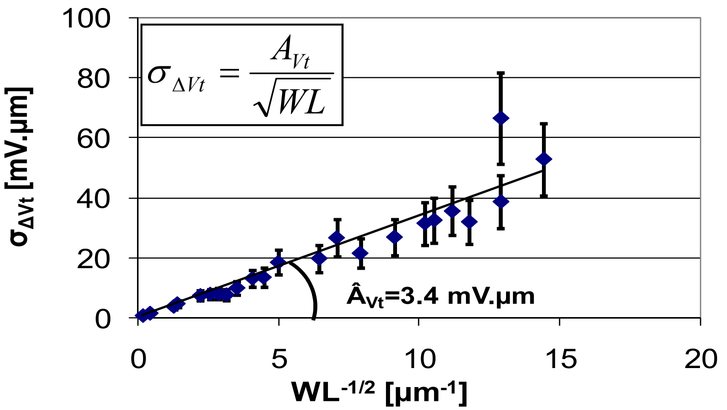
- mean$_P$: Systematic mismatch

☐ **σ$_P$: Stochastic mismatch (local process fluctuations)**

- Threshold voltage $\mathbf{V_T}$
- Gain factor β
- Drain current $\mathbf{I_D}$

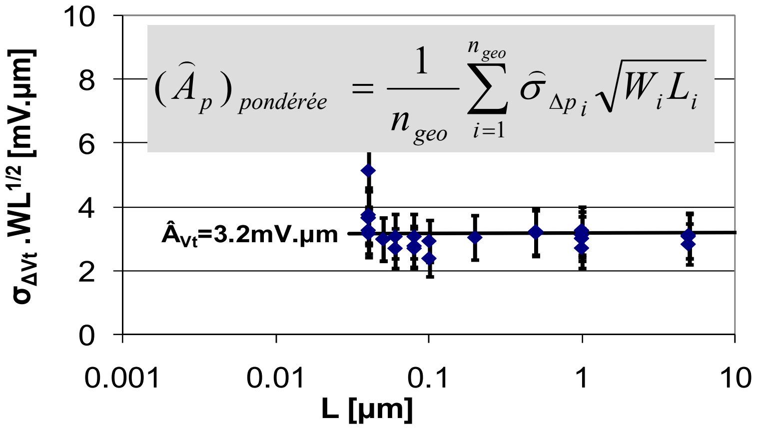
Mismatch parameter extraction

Standard …



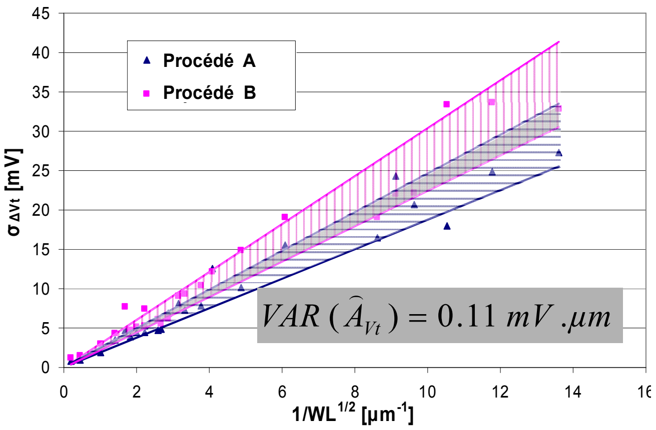
$$\sigma_{\Delta Vt} = \frac{A_{Vt}}{\sqrt{WL}}$$

Improved method …

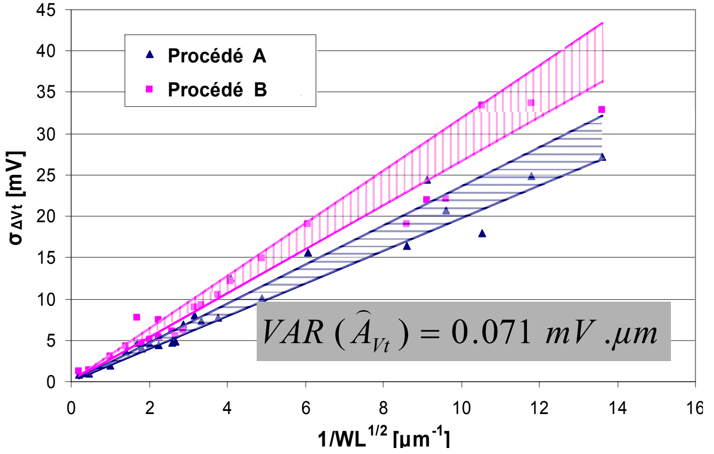


$$(\widehat{A}_p)_{pondérée} = \frac{1}{n_{geo}} \sum_{i=1}^{n_{geo}} \widehat{\sigma}_{\Delta p_i} \sqrt{W_i L_i}$$

=> Allows discrimination of process differences



$$VAR(\widehat{A}_{Vt}) = 0.11\ mV.\mu m$$



$$VAR(\widehat{A}_{Vt}) = 0.071\ mV.\mu m$$

[Cathignol *et al.*, ICMTS, 06]

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  - Channel and pocket contributions
  - Polygate influence
  - Variability sources diagnostic on C45 technology
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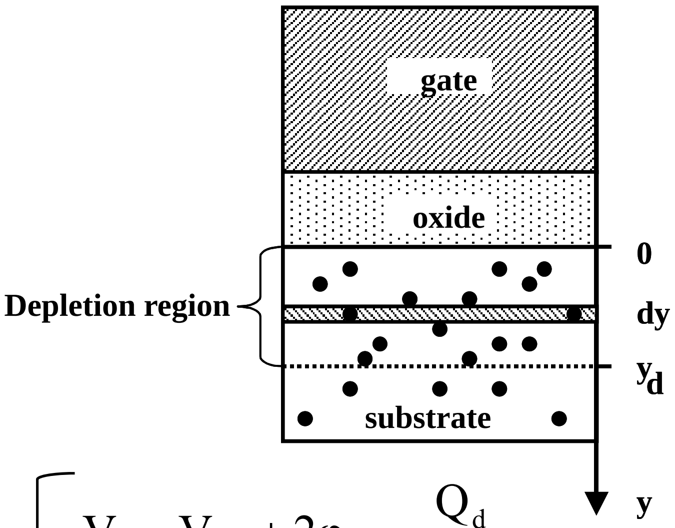
Channel contribution

Theory



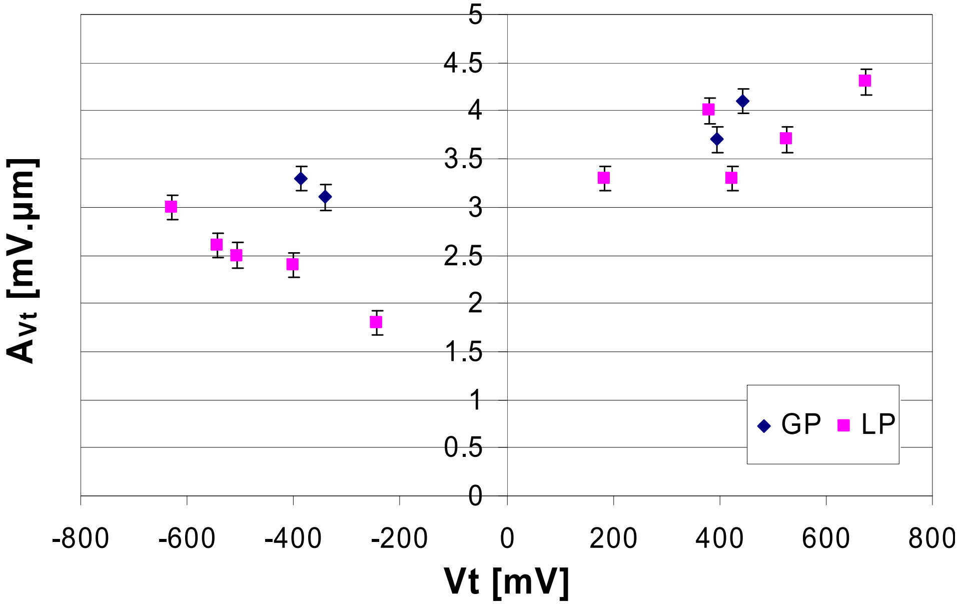
$$\left\{ \begin{array}{l} V_t = V_{FB} + 2\varphi_{Fp} - \dfrac{Q_d}{C_{ox}} \\ \sigma_{nc} = \sqrt{n_c} \end{array} \right.$$

[Mizuno *et al.*, TED, 89]

$$\Rightarrow \sigma_{Vt} = \frac{\left(2q^3 \cdot \varepsilon_{si} \cdot N_c \cdot \left(2\phi_{Fp} - V_b\right)\right)^{1/4}}{\sqrt{3}} \cdot \frac{T_{ox}}{\varepsilon_{ox}} \cdot \frac{1}{\sqrt{W \cdot L}}$$

$\sigma_{Vt} \approx t_{ox}.Nc^{\,0.4}$ [Roy, TED, 03]

Measurements



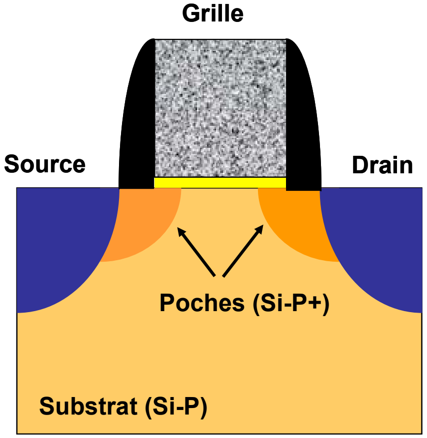
Strong correlation between Vt et A_{vt}
=> main contribution from channel dopants

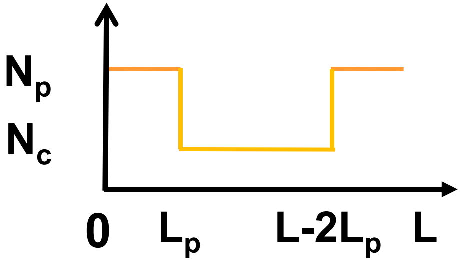
$$\sigma_{Vt} = B_{Vt} \sqrt{\frac{t_{ox}.(V_t + 0.1)}{W.L}}$$

[Takeuchi, 07]

Pockets contribution (1/3)

- ❑ **Existing models explain the usually observed fluctuations increase for shortest devices…**



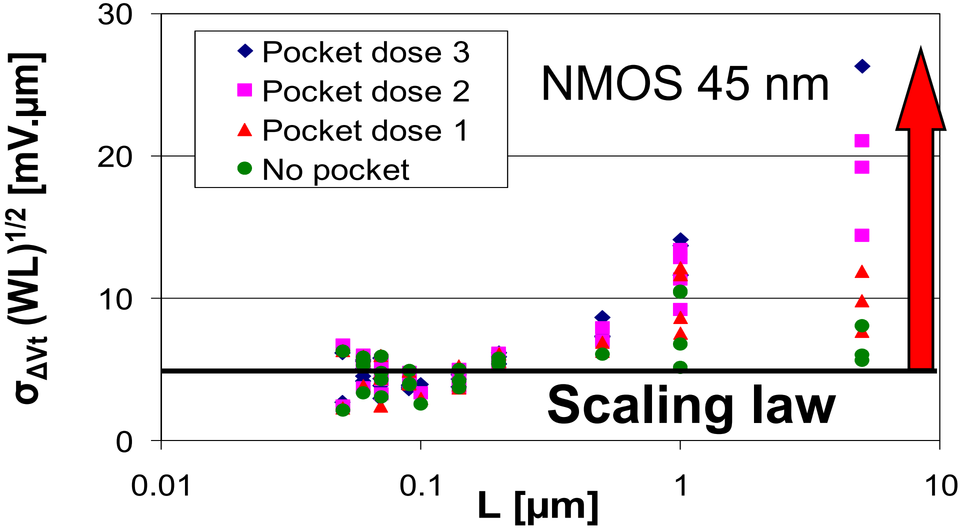


$$Vt = \int_0^L Vt(x)dx$$

$$\xcancel{\sigma_{Vt} = \frac{1}{\sqrt{W\cdot L}}\sqrt{\left(\frac{Q_d(N_p)}{\sqrt{3}\cdot C_{ox}}\right)^2\cdot\frac{2\cdot L_p}{L\cdot N_p\cdot y_d(N_p)} + \left(\frac{Q_d(N_c)}{\sqrt{3}\cdot C_{ox}}\right)^2\cdot\frac{L-2\cdot L_p}{L\cdot N_c\cdot y_d(N_c)}}}$$

[DiFrenza, 02]

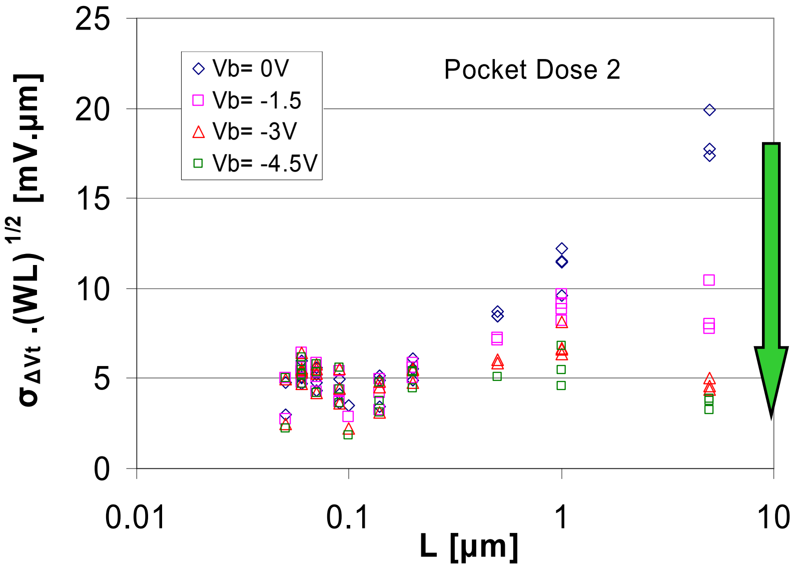
- ❑ **…but these models do not predict anomalous increase for long transistors…**



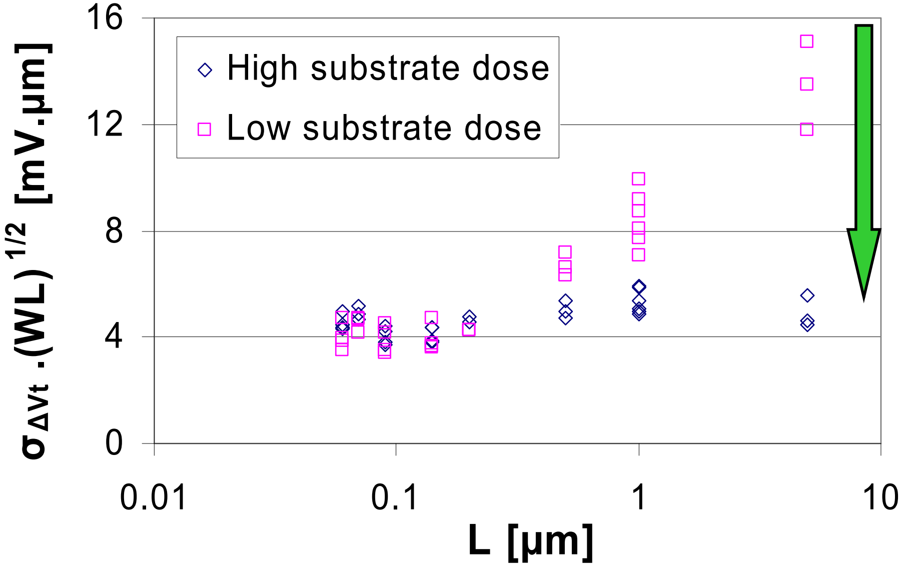
[Cathignol, SSE 09]

Pockets contribution (2/3)

Body bias influence…



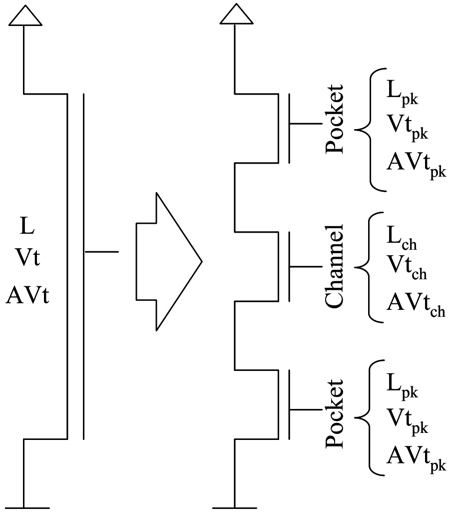
Channel dose influence…



[Cathignol, SSE 09]

Pockets contribution (3/3)

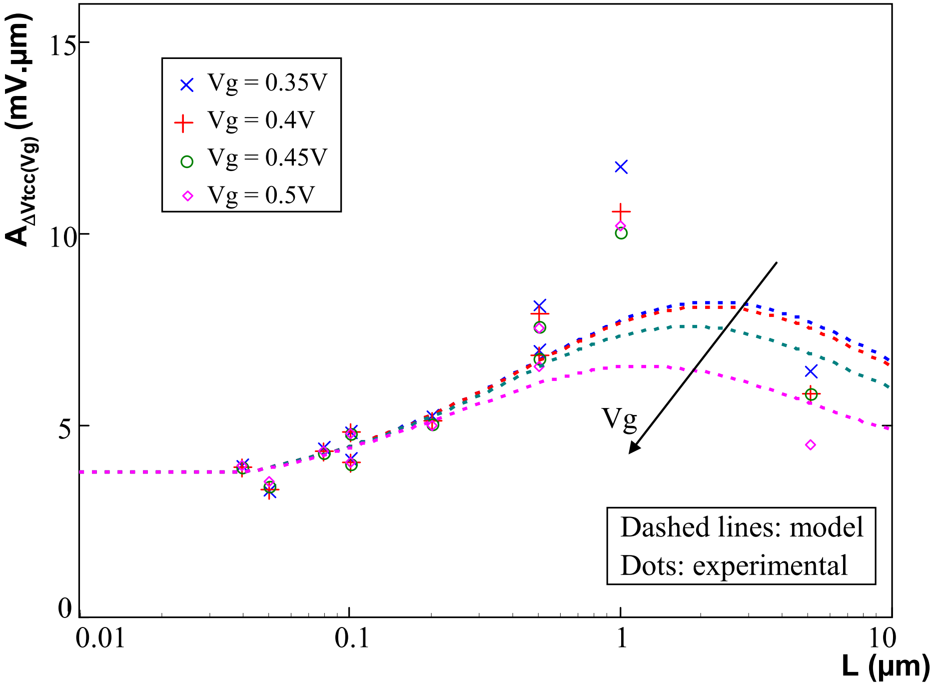
3-transistor model



$$\sigma_{R_{tot}}(Vg)=\sqrt{\left(\frac{\partial R_{ch}}{\partial Vg}\right)^2\frac{A_{ch}^2}{WL_{ch}}+2\left(\frac{\partial R_{pk}}{\partial Vg}\right)^2\frac{A_{pk}^2}{WL_{pk}}}$$

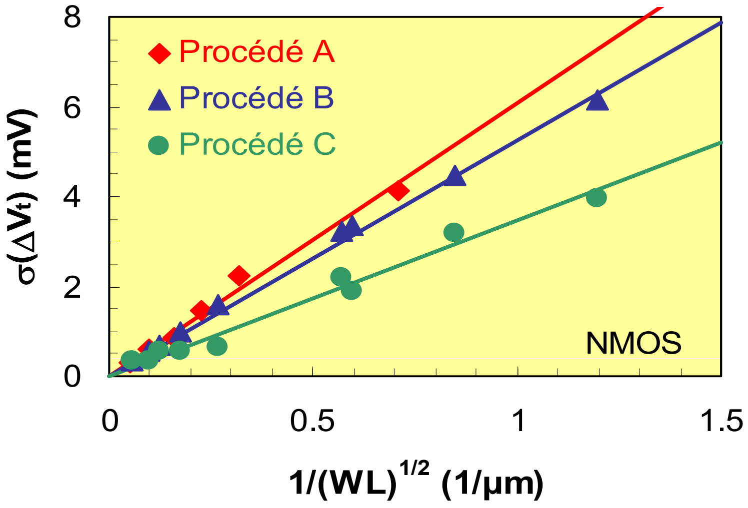
[Mezzomo, SSE 10]

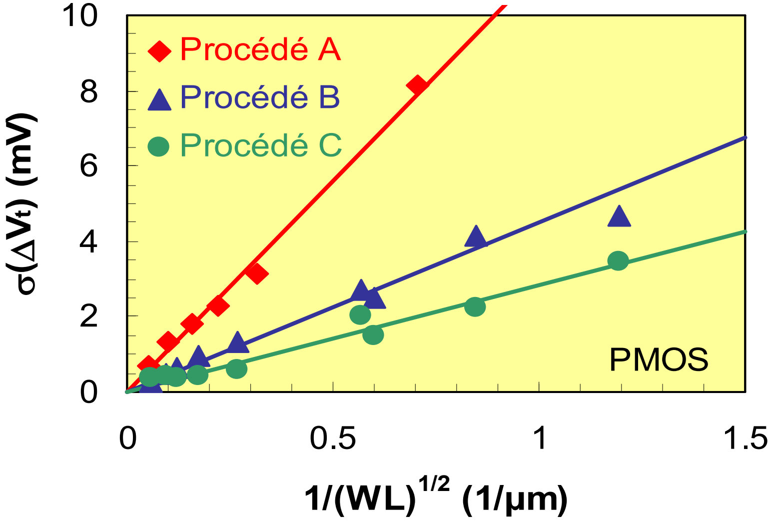
Bell-shaped behavior !



- ➢ Comprehensive modelling
- ➢ Can be extended to non-ohmic regime (see Mezzomo ESSDERC 2010)

Polygate influence: Impact of process (1/2)



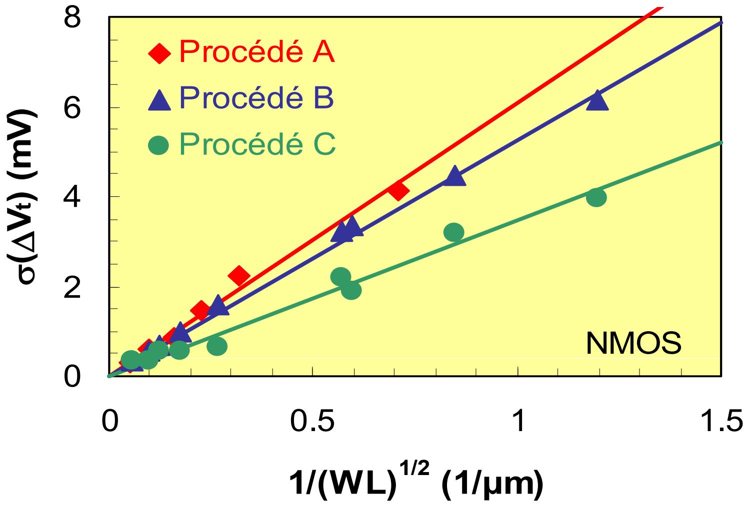


Process	A_{Vt} (mV.µm)	
	NMOS	PMOS
A	6.08	11.2
B	5.31	4.52
C	3.46	2.85

=> Significant matching improvement

[DiFrenza, 02]

Polygate influence: Impact of process (2/2)



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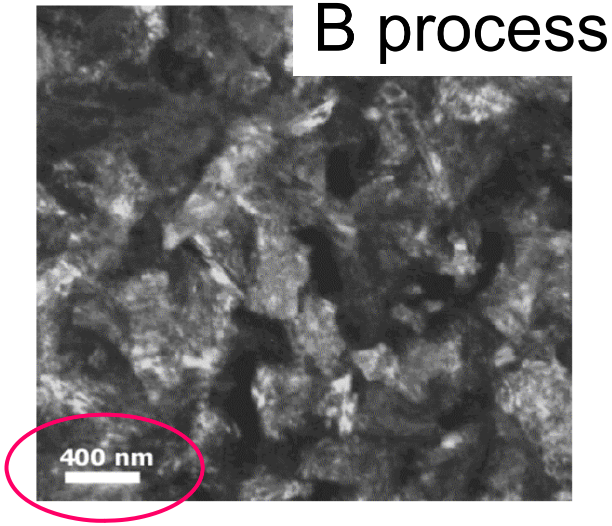
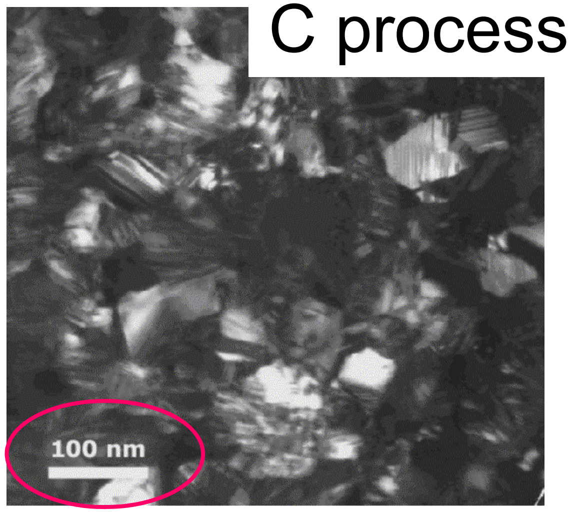


$L_{grain} \sim 0.1\mu m$



Photos MEB (Réf. E. Sondergard)

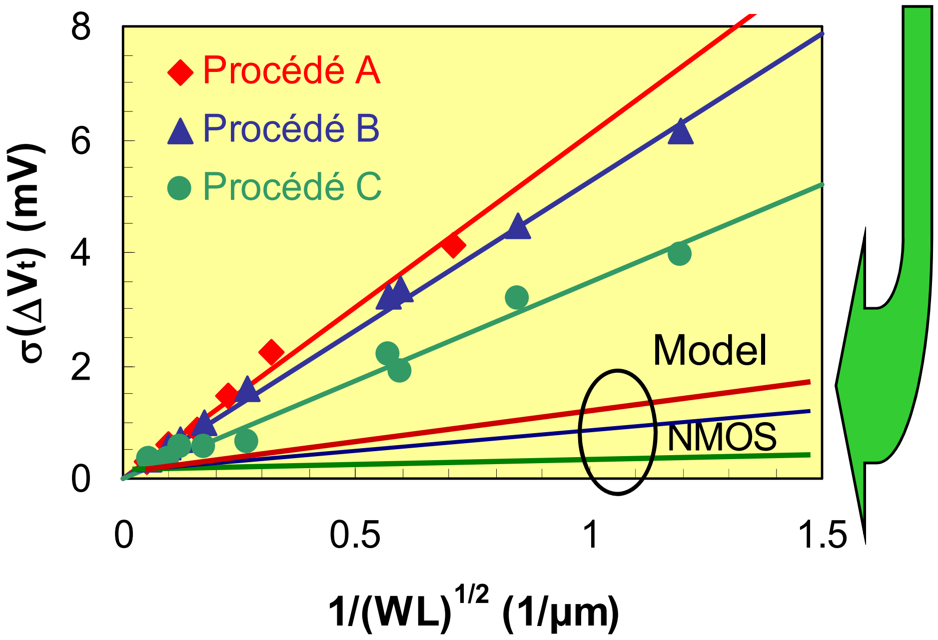
Grain size reduction from B to C!

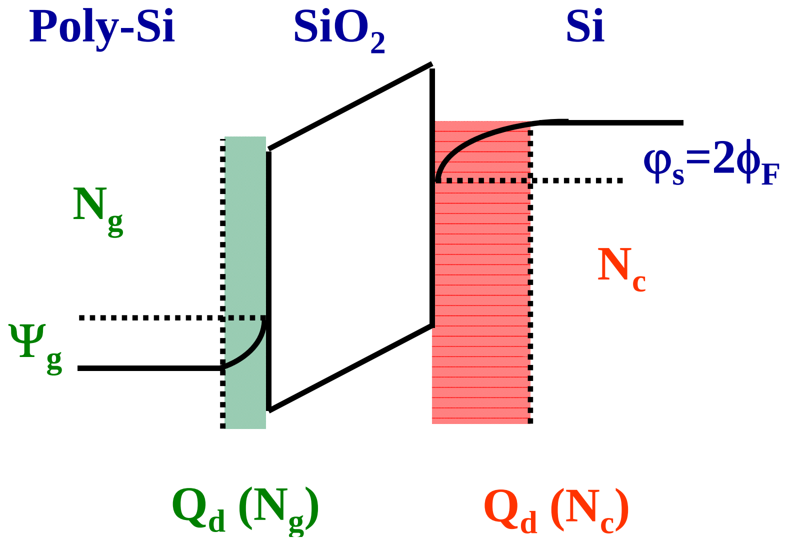
[DiFrenza, 02]

Polygate influence: doping approach (1/5)

$$V_t = V_{FB} + 2\phi_F - \frac{Q_d}{C_{ox}} + \psi_g$$ **with** $$\psi_g = (2\phi_F - V_b)\cdot\frac{Nc}{Ng}$$

Without clustering in poly $$\frac{\sigma(n)}{n} = \frac{1}{\sqrt{<n>}}$$





[DiFrenza, 02]

Polygate influence: doping approach (2/5)

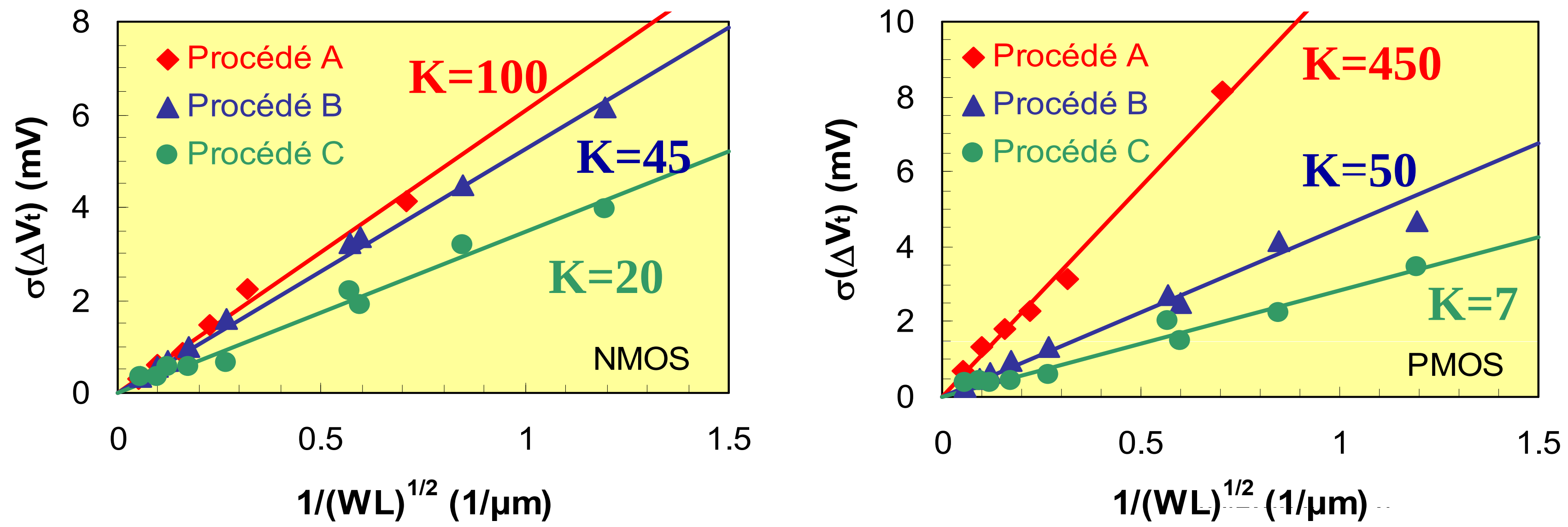
$$V_t = V_{FB} + 2\phi_F - \frac{Q_d}{C_{ox}} + \psi_g$$

with

$$\psi_g = \left(2\phi_F - V_b\right)\cdot\frac{Nc}{Ng}$$

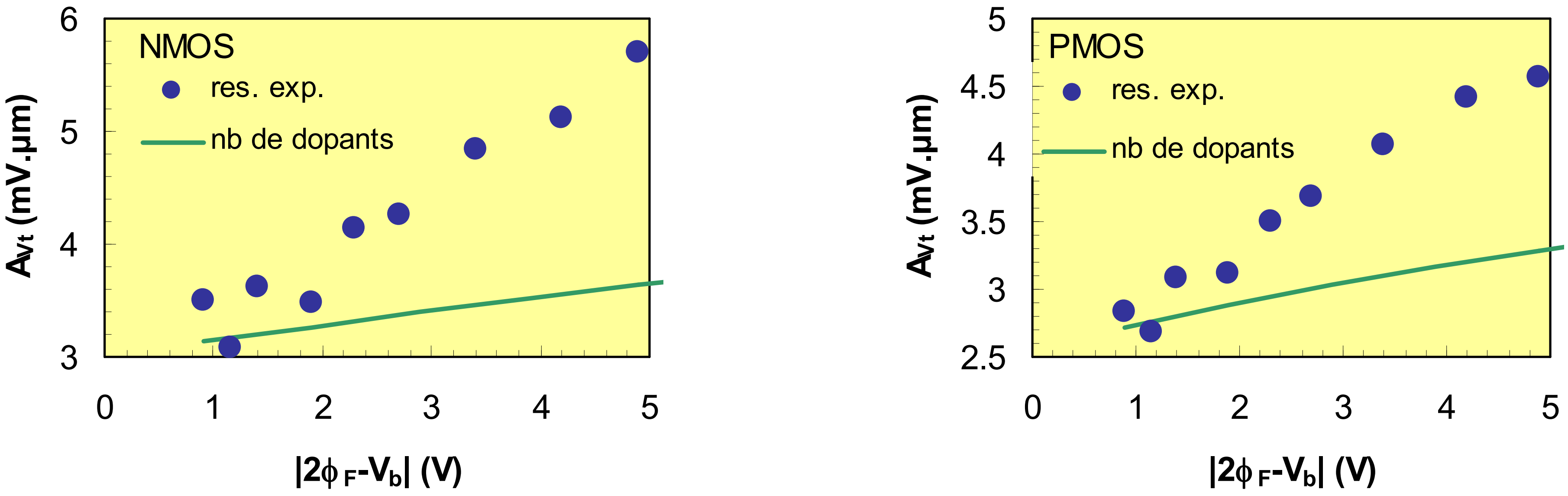
With clustering in poly

$$\frac{\sigma(n)}{n} = \frac{1}{\sqrt{\frac{<n>}{K}}}$$



Polygate influence: doping approach (3/5)

A_{Vt} as a function of V_b

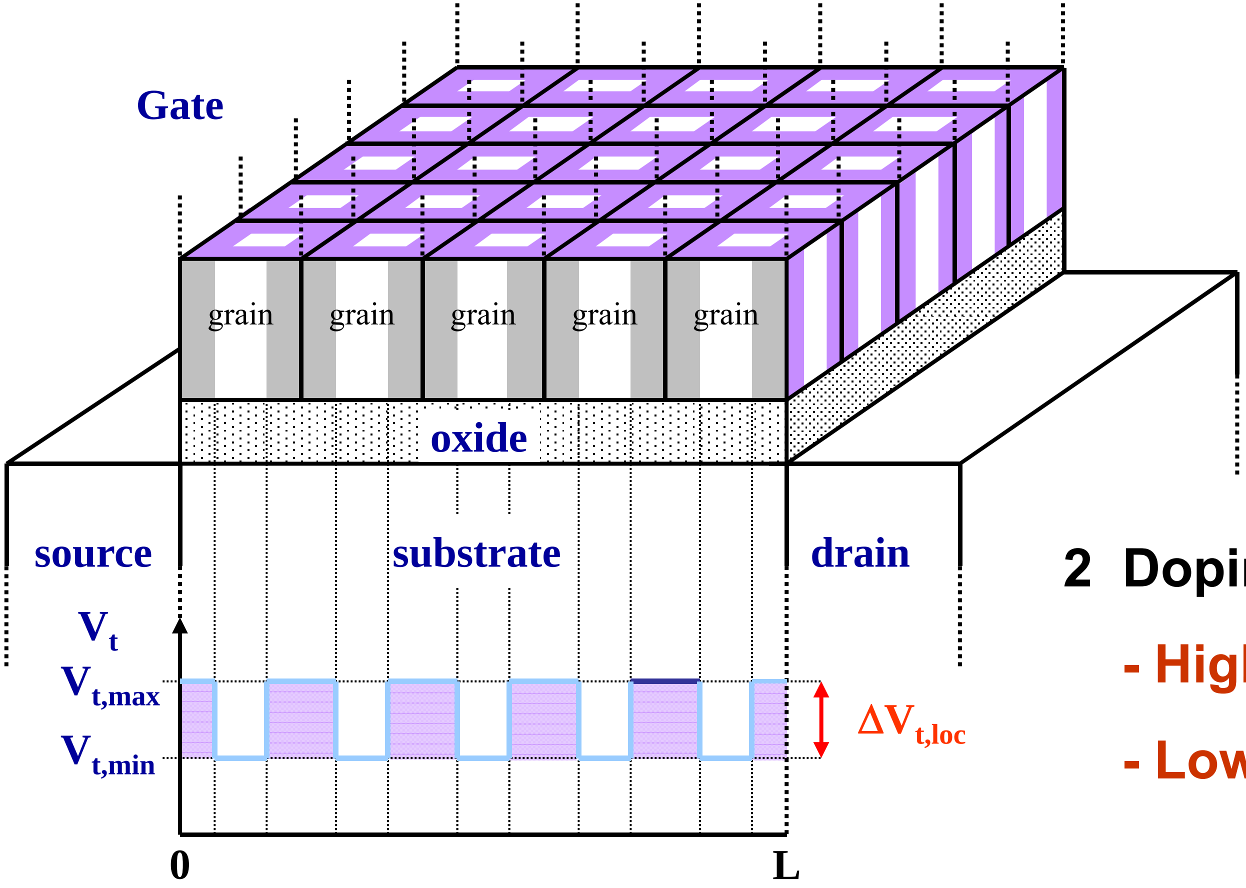


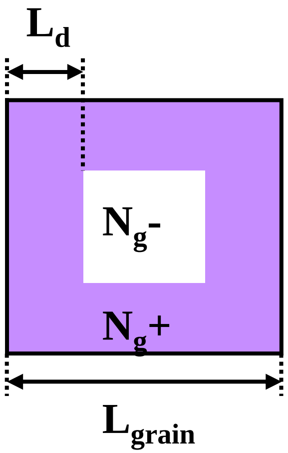
This model does not allow describing Avt variation as a function of bulk potential!

[DiFrenza, 02]

Polygate influence: doping approach (4/5)

Model with 2 Doping Levels in Grains





2 Doping levels :

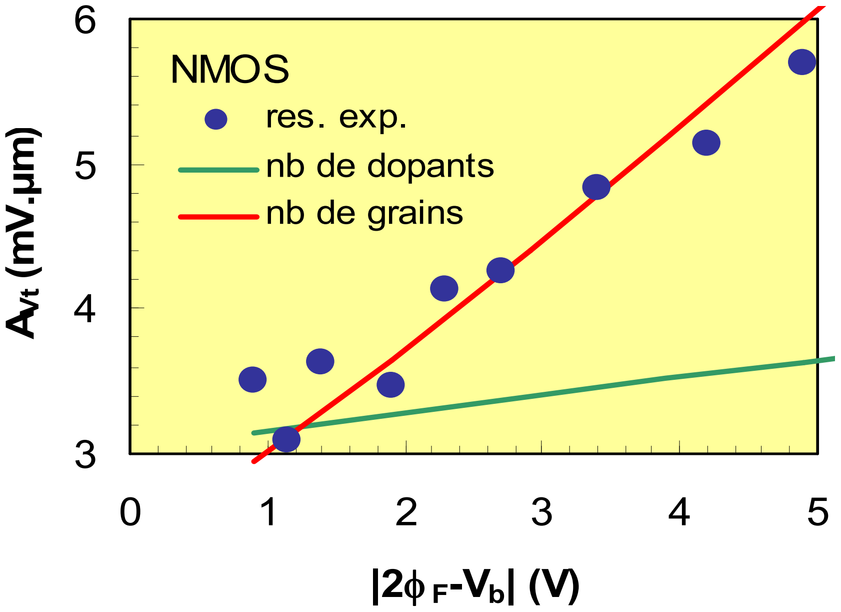
- High doping level: N_{g+}
- Low doping level: N_{g-}

[DiFrenza, 02]

Polygate influence: doping approach (5/5)

Model with 2 Doping Levels in Grains

$$V_t = V_{t,min} \cdot \frac{A_{N_{g-}}}{W \cdot L} + V_{t,max} \cdot \frac{A_{N_{g+}}}{W \cdot L} \Rightarrow \sigma_{Vt,Ngrain} = (2\phi_F - V_b) \cdot \frac{2L_d - 4L_d^2 \cdot \sqrt{N_{grain}}}{N_{g-} \cdot \sqrt{W \cdot L}}$$



Grains number fluctuation model leads to a good description of Bulk polarization impact on Avt

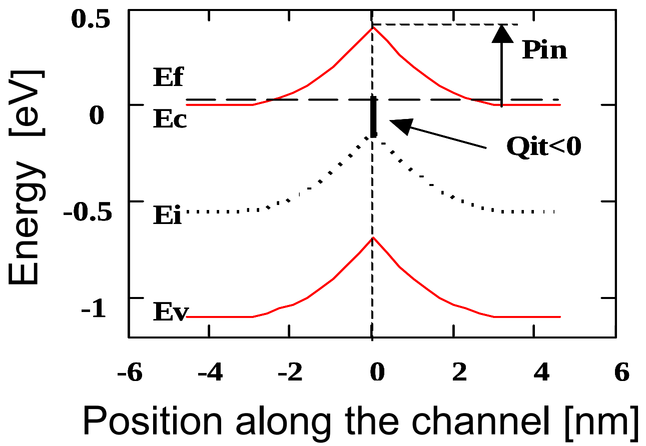
[DiFrenza, 02]

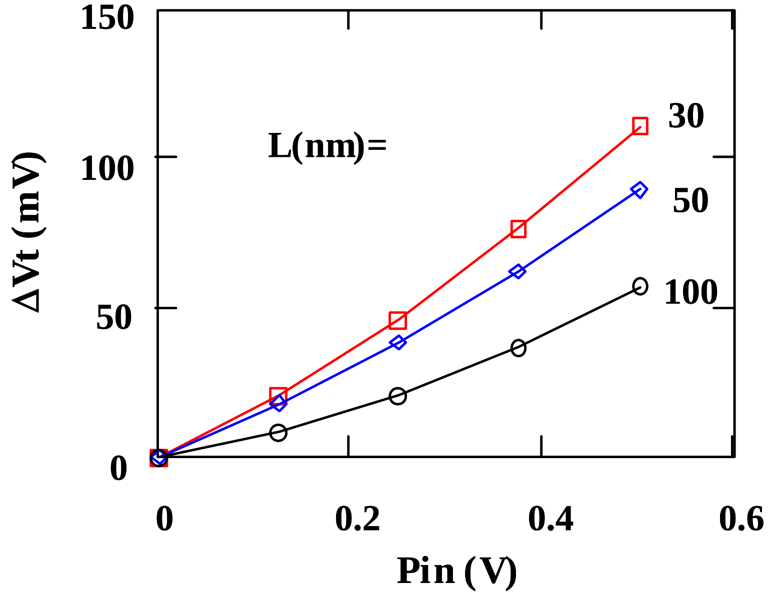
Polygate influence: GB approach (1/2)

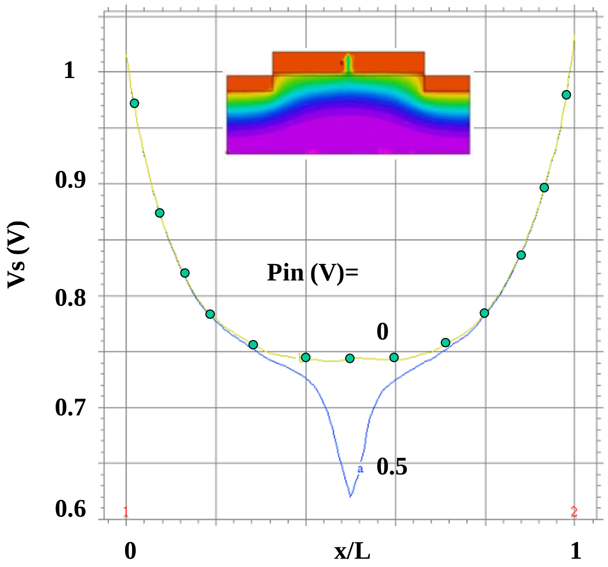
Model for a singe grain boundary

$$Qit(V) = q.Nit.(V - Vi)$$

$$2.Qd(V) + Qit(V) = 0$$







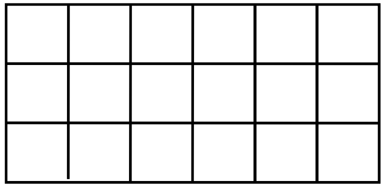
[Cathignol, ULIS 2006]

Polygate influence: GB approach (2/2)

Analytical expression of Vt shift induced by a single GB

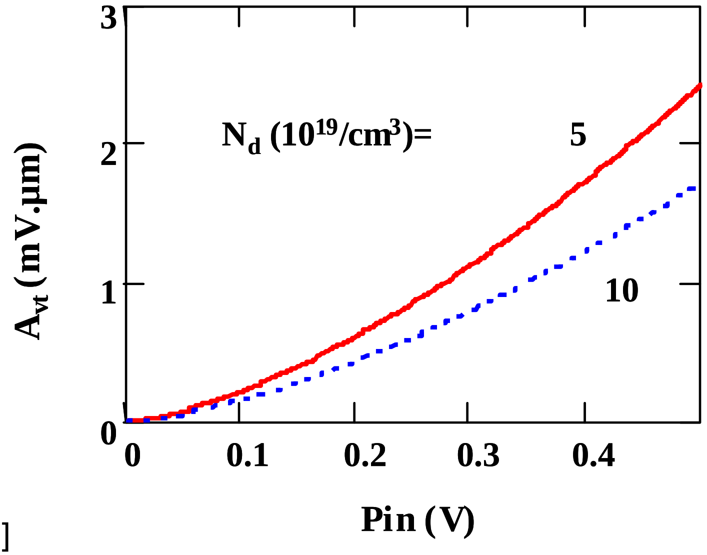
$$\Delta Vt_0 = \frac{1}{W\,L}.\int \delta\phi_{ms}(x,y)\,dxdy \Rightarrow \Delta Vt_0 = \frac{1}{WL}.\frac{4}{3}.\frac{\varepsilon_{si} Pin^{3/2}}{\sqrt{2\,q\,\varepsilon_{si} Nd}}$$

Analytical expression of the transistor Vt fluctuations induced by multiple GB



$$+ \quad \sigma_{ng} = \sqrt{ng}$$

$$\Rightarrow \sigma_{\Delta Vt} = \frac{1}{\sqrt{WL}}\frac{8}{3}\frac{\varepsilon_{si} Pin^{3/2}}{\sqrt{q\,\varepsilon_{si} Nd}} = \frac{Avt|_{gate}}{\sqrt{WL}}$$



[Cathignol, ULIS 2006]

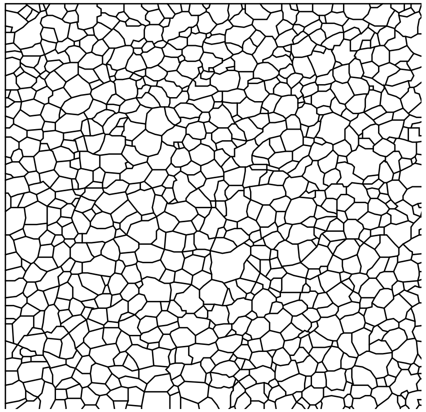
Polygate quantitative evaluation

Evaluation of the contribution thanks to atomistic simulation run on 200 generic NMOS transistors randomly generated

Fermi level pinning model at each grain boundary

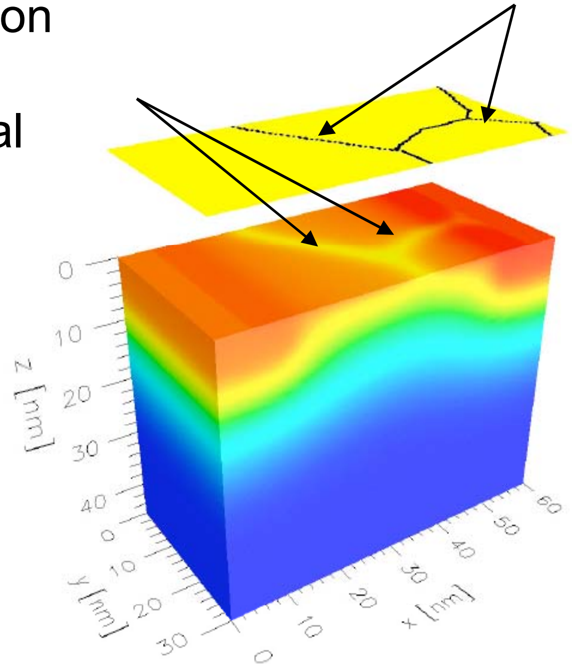
\+

Random position and size of grain through the gate according to a experimental top view of polysilicon



Impact on surface potential

Grain boundary

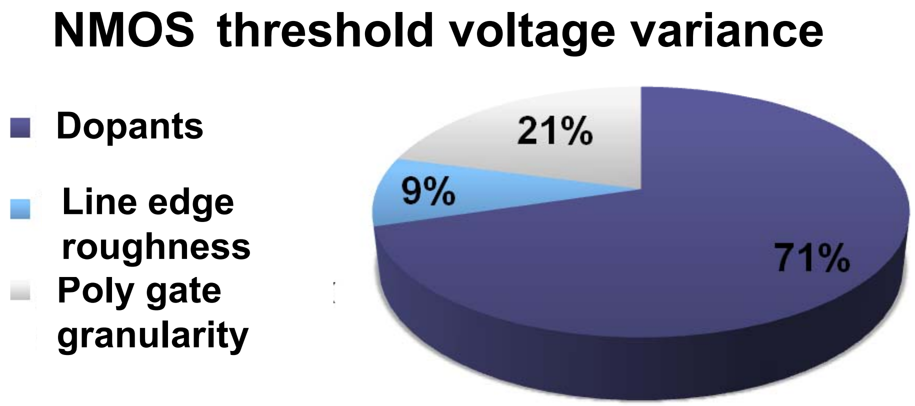


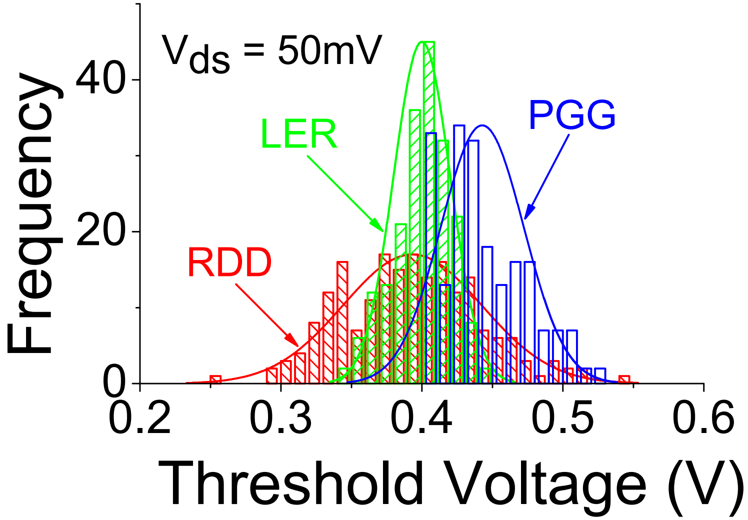
Brown *et al*., ESSDERC 06

=> The order of magnitude is 1 mV.µm

Diagnostic of variability sources on real C45 device: atomistic simulation

- ❑ Exact TCAD calibration done on silicon data
- ❑ Fluctuations sources not correlated
- ❑ Fermi level pinning evaluated at 200mV



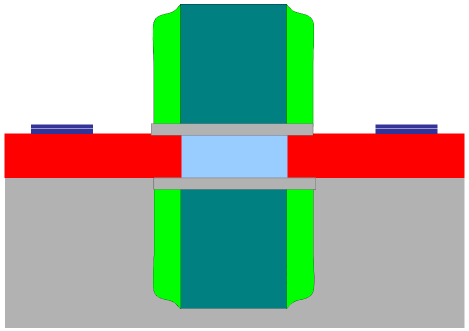


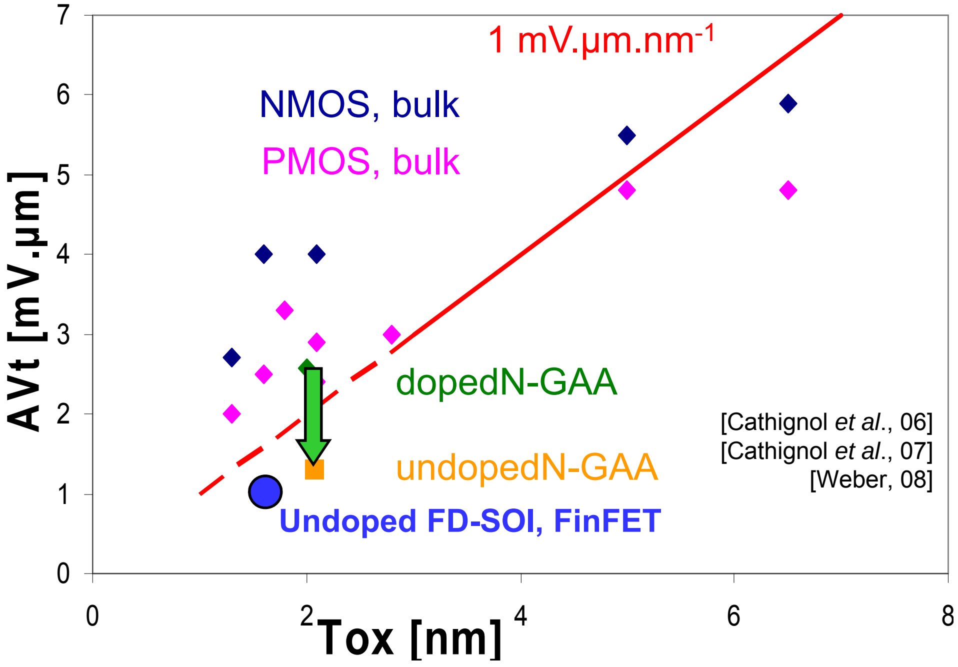
σVtexp=62 mV & σVtsim= 66mV

Cathignol *et al.*, EDL, 2008
Asenov, Cathignol *et al*. EDL, 2008

Conclusions (1/2)

- ❑ 70% of variability comes from channel & pocket dopant number fluctuations => undoped channels are required!
- ❑ Ultra thin film technologies are the best candidates
- ❑ Remaining variability sources: LER, Φ_{ms} fluctuations in GB of metal gate, stress, STI, S/D contact, …





Conclusions (2/2)

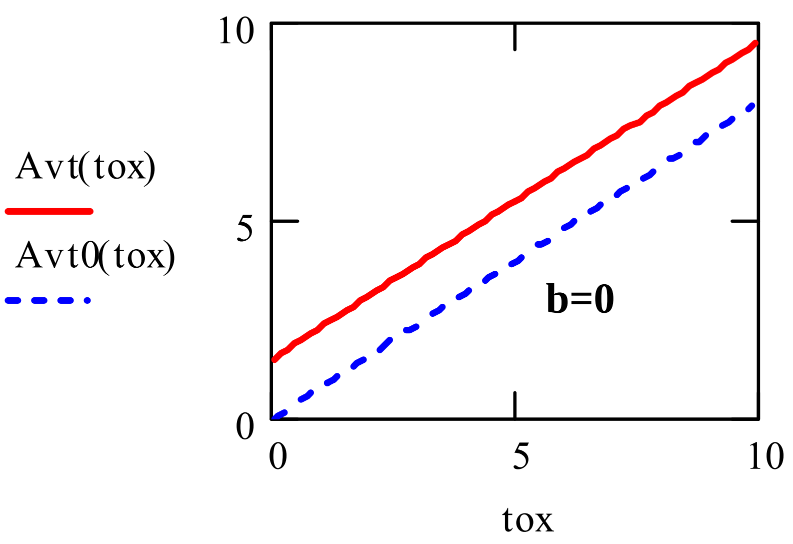
- **Scaling issues…**

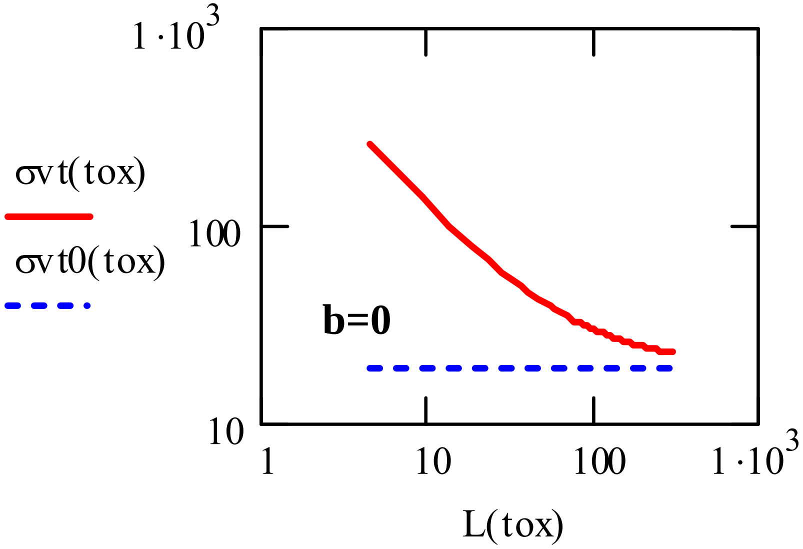
$$Avt(tox) := a \cdot tox + b$$

a=0.8 mV.µm/nm
b=1.5 mV.µm

$$\sigma vt(tox) := \frac{Avt(tox)}{\sqrt{WL(tox)}}$$

$$L(tox) := 30 \cdot tox$$





References

R. Difrenza, P. Llinares, G. Morin, E. Granger, G. Ghibaudo, A New Model for Threshold Voltage Mismatch Based on the Random Fluctuations of Dopant Number in the MOS Transistor Gate, ESSDERC 2001, Nuremberg, Germany (Sept. 2001)

R. Difrenza, P. Llinares, S. Taupin, R. Palla, G. Ghibaudo, Comparison Between Matching Parameters and Fluctuations at the Wafer Level, IEEE/ICMTS 2002, Cork, Ireland (March 2002)

R. DiFrenza, J.C. Vildeuil, P. Llinares, G. Ghibaudo, Impact of grain number fluctuations in the MOS transistor gate on matching performance, IEEE ICMTS 2003, Monterey, USA (March 2003)

R. Difrenza, P. Llinares, G. Ghibaudo, A New Model for the Current Factor Mismatch in the MOS Transistor, Solid State Electronics, 47, 1167 (2003).

R. Difrenza, P. Llinares, G. Ghibaudo, The impact of short channel and quantum effects on the MOS transistor mismatch, Solid State Electronics, 47, 1161 (2003).

A.Cathignol, K. Rochereau, S. Bordez, G. Ghibaudo, Improved methodology for the Characterization of Avt MOSFET matching parameter dispersion, IEEE ICMTS 2006, Austin, USA (March 2006)

A.Cathignol, K. Rochereau, G. Ghibaudo, Impact of a single grain boundary in the polycrystalline silicon gate on sub 100nm bulk MOSFET characteristics - Implication on matching properties, ULIS conference, Grenoble (April 2006)

A.Cathignol, A. Cros, S. Harrison, R. Cerrutti, P. Coronel, A. Pouydebasque, K. Rochereau, T. Skotnicki, G. Ghibaudo, High threshold voltage matching performance on gate-all-around MOSFET, Solid State Electronics, 51, 1450 (2007)

A.Cathignol, B. Cheng, D. Chanemougame,A. R. Brown, K. Rochereau, G. Ghibaudo, A. Asenov, Quantitative Evaluation of Statistical Variability Sources in a 45nm Technological Node LP N-MOSFET, IEEE Electron Device Letters, 29, 609 (2008).

A.Asenov, A. Cathignol, B. Cheng, K. P. McKenna, A. R. Brown, A. L. Shluger, G. Ghibaudo, Origin of the Asymmetry in the Statistical Variability of *n*- and *p*-channel Poly-Si Gate Bulk MOSFETs, IEEE Electron Device Letters, 29, 913 (2008).

A.Cathignol, S. Bordez, A. Cros, K. Rochereau, G. Ghibaudo, Abnormally high local electrical fluctuations in heavily pocket-implanted bulk long MOSFET, Solid State Electronics, 53, 127–133 (2009)

C.Mezzomo, M. Marin and G. Ghibaudo, MOSFET Mismatch Measure Improvement Using Kelvin Test Structures, IEEE ICMTS, Mandalay Beach Resort, Oxnard, CA, USA (april 2009)

C.Mezzomo, C. Leyris, E. Josse and G. Ghibaudo, Pockets Engineering Impact on Mismatch Performance on 45nm MOSFET technologies, IEEE ULIS Conference, Aachen, Germany (March 2009)

C.Mezzomo, A. Bajolet, A. Cathignol and G. Ghibaudo, Drain Current Variability in 45nm Heavily Pocket-implanted Bulk MOSFET: Characterization and Modeling, ESSDERC 2010, Sevilla, Spain (Sept 2010)

C.Mezzomo, A. Bajolet, A. Cathignol, E. Josse and G. Ghibaudo, Modeling Local Electrical Fluctuations in 45nm Heavily Pocket-implanted Bulk MOSFET, Solid State Electronics, in press (2010)