

Preliminary Technical Program

WEDNESDAY, SEPTEMBER 5

Plenary Session I (Invited Talks)

Chairpersons: N. Goldsman, *University of Maryland*
V. Axelrad, *Sequoia Design Systems*

- 08:30 **Welcome Presentation**
- 08:50 **The Story Beyond Primitive Compact Model -
I-1 A Super Compact Model for Advanced
Technology**
C.-K. Lin, C. Hsiao, K.-W. Su, M.-C. Jeng,
*Taiwan Semiconductor Manufacturing Company,
Hsin-Chu County, Taiwan*
- 09:30 **Strain Engineering in MOS and Tunnel FETs:
I-2 Models, Challenges and Opportunities**
D. Esseni,
DIEGM - University of Udine, Udine, Italy
- 10:10 Coffee Break

WEDNESDAY, SEPTEMBER 5

Session 1 – Transport: Monte Carlo and Boltzmann

Chairperson: S. Selberherr, *T.U. Vienna*

- 10:30 **Band Structure and Ballistic Electron
I-1 Transport Simulations in GeSn Alloys**
S. Gupta, B. Magyari-Köpe, Y. Nishi, K. C.
Saraswat,
Stanford University, Stanford, CA
- 10:50 **Monte Carlo Simulation of Program
I-2 Disturb in Contact-Less Virtual Ground
NOR Flash Memory**
Y. Isagi, Y. Yamauchi, Y. Kamakura*,
*Osaka University, Osaka, Japan, *Japan Science
and Technology Agency, CREST, Kawaguchi,
Japan*
- 11:10 **Impact of Single Trapped Charge in
I-3 Gate-All-Around Nanowire Channels
Studied by Ensemble Monte
Carlo/Molecular Dynamics Simulation**
T. Kamioka*, H. Imai*, T. Watanabe*, K.
Ohmori**, K. Shiraiishi**, M. Niwa**, K.
Yamada**, Y. Kamakura***,
*Japan Science and Technology Agency, CREST,
Kawaguchi, Japan, *Waseda University, Tokyo,
Japan, **University of Tsukuba, Ibaraki, Japan,
***Osaka University, Osaka, Japan*
- 11:30 **Methodology for Simulation of Electronic
I-4 Transport in Nanocrystal Solids**
H. Lepage, G. le Carval, A. Kaminski-Cachopo*,
*CEA, LETI, MINATEC Campus, France,
IMEP-LAHC, MINATEC Campus, France
- 11:50 **Bipolar Spherical Harmonics Expansions
I-5 of the Boltzmann Transport Equation**
K. Rupp, C. Jungemann*, M. Bina, A. Jungel,
T. Grasser,
*TU Wien, Wien, Austria, *RWTH Aachen,
Aachen, Germany*
- 12:10 Lunch on your own

WEDNESDAY, SEPTEMBER 5

Session 2 – Power Devices

Chairperson: Y. Kamakura, *Osaka University*

- 10:30
2-1 **Modeling and Simulations on Current Collapse in AlGaIn/GaN Power HEMTs**
H. Huang, Y. C. Liang, G. S. Samudra, Y. Li, Y.-C. Yeo,
National University of Singapore, Kent Ridge Crescent, Singapore
- 10:50
2-2 **Failure Analysis of Power MOSFETs based on Multi-finger Configuration under Unclamped Inductive Switching (UIS) Stress Condition**
K. Nidhi, N. Agarwal, S.-M. Yang, Purwadi, G. Sheu, J.-R. Tsai,
Asia University, Taichung, Taiwan
- 11:10
2-3 **Predictive TCAD Approach for the Analysis of Hot-Carrier-Stress Degradation in Integrated STI-based LDMOS Transistors**
S. Reggiani, G. Barone, S. Poli*, M.-Y. Chuang*, W. Tian*,
*University of Bologna, Bologna, Italy, *Texas Instruments Inc., Dallas, Texas*
- 11:30
2-4 **A Numerical a-posteriori - Method to Calculate Local Self-Heating in Power Devices After the Impact of a Cosmic Particle**
C. Weiß, G. Wachutka,
Munich University of Technology, Munich, Germany
- 11:50
2-5 **Correlation between Gate Charge and Gate Capacitances of Power MOSFETs and Extraction of Related BSIM3/4 Model Parameters**
W. Wu, U. Aghoram, H.-C. Wu, D. Basu, A. Sanford, S. Banerjee, K. Joardar,
Texas Instruments, Dallas, TX
- 12:10 Lunch on your own

WEDNESDAY, SEPTEMBER 5

Session 3 – Quantum Transport

Chairperson: I. Knezevic, *University of Wisconsin*

- 13:30
3-1 **Atomistic Quantum Transport Simulation of Topological Insulator Bi₂Se₃ Tunnel FETs**
J. Chang, L. F. Register, S. K. Banerjee,
The University of Texas at Austin, Austin, TX
- 13:50
3-2 **Multi-scale Simulation of Interfacial Roughness Effects in Silicon Nanowires**
B.-H. Kim, H.-E. Jung**, Y.-C. Chung*, M. Shin**, K.-R. Lee,
*Korea Institute of Science and Technology, Seoul, Republic of Korea, *Hanyang University, Seoul, Republic of Korea, **Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea*
- 14:10
3-3 **Time Dependent Quantum Transport in Graphene**
D. Reddy, P. Jadaun, A. Valsaraj, L. F. Register, S. K. Banerjee,
The University of Texas at Austin, Austin, TX
- 14:30
3-4 **Atomistic Simulation of Phonon-Assisted Tunneling in Bulk-like Esaki Diodes**
R. Rhyner, M. Luisier, A. Schenk,
Integrated Systems Laboratory, ETH Zurich, Zurich, Switzerland
- 14:50
3-5 **Molecular Dynamics Simulation of Heat Transport in Silicon Fin Structures**
T. Zushi, T. Watanabe*, K. Ohmori**, K. Yamada**,
*Waseda University, Tokyo, Japan, *Japan Science and Technology Agency, CREST, Saitama, Japan, **University of Tsukuba, Ibaraki, Japan*

WEDNESDAY, SEPTEMBER 5

Session 4 – Compact Modeling

Chairperson: S. Reggiani, *University of Bologna*

13:30 **CoolSPICE: SPICE for Extreme Temperature
4-1 Range Integrated Circuit Design and
Modeling**

A. Akturk, S. Potbhare, J. Booz, N. Goldsman, D. Gundlach*, R. Nandwana**, K. Mayaram**, *CoolCAD Electronics LLC, College Park, MD, *NIST, Gaithersburg, MD, **Oregon State University, Corvallis, OR*

13:50 **An Accurate Surface-Potential Based Large-
4-2 Signal Model for HEMTs**

J. Liu, Z. Yu, L. Sun, *Hangzhou Dianzi University, Hangzhou, China*

14:10 **Characterization of Time Dependent Carrier
4-3 Trapping in Poly-Crystalline TFTs and Its
Accurate Modeling for Circuit Simulation**

Y. Oodate, H. Tanoue, M. Miyake, A. Tanaka, Y. Shintaku, T. Nakahagi, A. Toda, T. Iizuka, H. Kikuchihara, H. J. Mattausch, M. Miura-Mattausch, *Hiroshima University, Hiroshima, Japan*

14:30 **A Compact Model for Graphene FETs for
4-4 Linear and Non-linear Circuits**

K. N. Parrish, M. E. Ramón, S. K. Banerjee, D. Akinwande, *The University of Texas at Austin, Austin, TX*

14:50 **Compact Model of Graphene Field Effect
4-5 Transistors and Its Application in Circuit
Simulation of RF Mixer Consisting of GFETs
and CMOS**

W. Zhu, C. Linghu, J. Zhang, L. Zhang, Z. Yu, *Tsinghua University, Beijing, China*

WEDNESDAY, SEPTEMBER 5

Plenary Session II (Invited Talks)

Chairpersons: N. Goldsman, *University of Maryland*
V. Axelrad, *Sequoia Design Systems*

15:20 **Modeling “Circuits” with Spins and Magnets
I-3**

S. Datta, *Purdue University, West Lafayette, IN*

Poster Session and Welcome Reception

16:00 – 18:00

Poster Listings: Pages X - XI of Program

THURSDAY, SEPTEMBER 6

Session 5 – Transport and Graphene

Chairperson: F. Register, *University of Texas, Austin*

- 08:30 **5-1 Thermal Transport in Suspended and Supported Graphene Nanostructures**
Z. Aksamija, I. Knezevic,
University of Wisconsin-Madison, Madison, WI
- 08:50 **5-2 Change of the Electronic Conductivity of CNTs and Graphene Sheets Caused by a Three-dimensional Strain Field**
M. Ohnishi, K. Suzuki, H. Miura,
Tohoku University, Sendai, Japan
- 09:10 **5-3 Plasma Instability and Non-linear Wave Propagation in Gate-controlled Semiconductor and Graphene Conduction Channels**
S. Rudin, G. Rupper,
U.S. Army Research Laboratory, Adelphi, MD
- 09:30 **5-4 Numerical Simulation of ac Transport in Graphene on a SiO₂ Substrate**
N. Sule, K. J. Willis, S. C. Hagness, I. Knezevic,
University of Wisconsin-Madison, Madison, WI
- 09:50 **5-5 THz-Frequency Conductivity in Monolayer and Bilayer Graphene**
W. Zhang, D. Woolard*,
North Carolina State University, Raleigh, NC,
**U. S. Army Research Office, RTP, NC*
- 10:10 Coffee Break

THURSDAY, SEPTEMBER 6

Session 6 – Devices: Reliability and Variability

Chairperson: P. Andrei, *Florida State University*

- 08:30 **6-1 A Unified Computational Scheme for 3D Statistical Simulation of Reliability Degradations of Nanoscale MOSFETs**
F. Adamu-Lema, S. Amoroso, S. Markov, L. Gerrer, A. Asenov*,
*University of Glasgow, Glasgow, United Kingdom, *Gold Standard Simulations, Ltd, Glasgow, United Kingdom*
- 08:50 **6-2 Comprehensive Study of Process-Induced Device Performance Variability and its Optimization for 14 nm Technology Node Bulk FinFETs**
R.-H. Baek, C. Y. Kang, A. Kumar, C.-W. Sohn*, T. Michalak**, C. Borst**, C. Hobbs, P. Kirsch, R. Jammy,
*SEMATECH, Albany, NY, *POSTECH, Pohang, South Korea, **University at Albany-SUNY, Albany, NY*
- 09:10 **6-3 Simulation of Reliability on Nanoscale Devices**
M. Bina, O. Triebel*, M. Karner*, B. Kaczer**, T. Grasser,
*TU Wien, Wien, Austria, *Global TCAD Solutions, Austria, **Imec, Belgium*
- 09:30 **6-4 Statistical TCAD Based PDK Development for a FinFET Technology at 14nm Technology Node**
B. Cheng, X. Wang, A. R. Brown*, C. Millar*, A. Asenov*, J. B. Kuang**, S. Nassif**,
*University of Glasgow, Glasgow, U.K., *Gold Standard Simulations Ltd, Glasgow, U.K., **Austin Research Laboratory, IBM Research Division, Austin, USA*
- 09:50 **6-5 Analytical Model for the Threshold Voltage Variability due to Random Dopant Fluctuations in Junctionless FETs**
A. Gnudi, S. Reggiani, E. Gnani, G. Baccarani,
University of Bologna, Bologna, Italy
- 10:10 Coffee Break

THURSDAY, SEPTEMBER 6

Session 7 – SiC and Molecular Level Modeling

Chairperson: A. Asenov, *University of Glasgow*

- 10:30 **Density Functional Theory Based**
7-1 **Investigation of Defects and Passivation of 4H-Silicon Carbide/SiO₂ Interfaces**
S. Salemi, N. Goldsman, A. Akturk, A. Lelis*,
University of Maryland, College Park, MD,
**U.S. Army Research Laboratory, Adelphi, MD*
- 10:50 **Influence of Bandgap Narrowing and Carrier**
7-2 **Lifetimes on the Forward Current-Voltage Characteristics of a 4H-SiC p-i-n Diode**
G. Donnarumma, V. Palankovski, S. Selberherr,
J. Wozny*, A. Kubiak*, L. Ruta*, Z. Lisik*,
*TU Wien, Wien, Austria, *TU Lodz, Lodz, Poland*
- 11:10 **Many-Level Trap-to-Band Transitions in**
7-3 **Chalcogenide Memories**
M. Rudan, F. Buscemi, G. Marcolini, F.
Giovanardi, A. Cappelli*, E. Piccinini, R.
Brunetti*,
University of Bologna, Bologna, Italy,
**University of Modena and Reggio Emilia, and*
CNR-Institute of NanoSciences, Modena, Italy
- 11:30 **Tight-Binding Molecular Dynamics Study of**
7-4 **Mechanical and Electronic Properties in Twisted Graphene Nanoribbons**
S. Souma, S. Kaino, M. Ogawa,
Kobe University, Kobe, Japan
- 11:50 **Empirical Pseudopotential Calculations of**
7-5 **Two-dimensional Electronic States in 4H-SiC Inversion Layers**
R. Watanabe, Y. Kamakura*,
*Osaka University, Osaka, Japan, *Japan Science*
and Technology Agency, CREST, Kawaguchi,
Japan
- 12:10 Lunch on your own

THURSDAY, SEPTEMBER 6

Session 8 – Devices, Transport and Variability

Chairperson: C.-K. Lin, *TSMC*

- 10:30 **Numerical Study of Variability of**
8-1 **Technological Parameters on Remote Coulomb Scattering in Nanowire MOSFETs**
J. Dura, F. Triozon, D. Munteanu*, S. Barraud,
S. Martinie, J.L. Autran*,
CEA-LETI MINATEC, Grenoble, France,
**IM2NP-CNRS, Marseille, France*
- 10:50 **A Physical Model to Predict Grain Boundary**
8-2 **Induced V_{th} Variation in Poly-Si TFTs**
C.-H. Ho, G. D. Panagopoulos, C. Lu, K. Roy,
Purdue University, West Lafayette, IN
- 11:10 **3D Simulation Study of Work-Function**
8-3 **Variability in a 25 nm Metal-Gate FinFET with Curved Geometry using Voronoi Grains**
G. Indalecio, A.J. Garcia-Loureiro, M.
Aldegunde*, K. Kalna*,
University of Santiago de Compostela, Santiago
*de Compostela, Spain, *Swansea University,*
Swansea, United Kingdom
- 11:30 **Electric Field and Strain Effects on Surface**
8-4 **Roughness Induced Spin Relaxation in Silicon Field-Effect Transistors**
D. Osintsev, O. Baumgartner, Z. Stanojevic, V.
Sverdlov, S. Selberherr,
TU Wien, Wien, Austria
- 11:50 **Time Domain Simulation of Statistical**
8-5 **Variability and Oxide Degradation Including Trapping/detrapping Dynamics**
S. Markov, L. Gerrer, F. Adamu-Lema, S.
Amoroso, A. Asenov*,
*University of Glasgow, Glasgow, UK, *Gold*
Standard Simulations, Glasgow, UK
- 12:10 Lunch on your own

THURSDAY, SEPTEMBER 6

Session 9 – Sensors

Chairperson: D. Vasileska, *Arizona State University*

13:30 **Modeling of Biomimetic Flow Sensor based on
9-1 Artificial Hair Cell using CFD and FEM
Approach**
M. Norzaidi Mat Nawi, A. Abd Manaf, M. Rizal
Arshad, O. Sidek,
*Universiti Sains Malaysia, Pulau Pinang,
Malaysia*

13:50 **Detection Limit of ultra-scaled Nanowire
9-2 Biosensors**
A. Afzalain, N. Couniot, D. Flandre,
*Université catholique de Louvain (UCL),
Louvain-la-Neuve, Belgium*

14:10 **A Simulation Study of the Effect of Platinum
9-3 Contact on CNT Based Gas Sensors Using
Self-Consistent Field with NEGF Method**
A. Basak, S. K. Manhas, G. Kapil, S. Dasgupta,
N. Jain*,
*Indian Institute of technology Roorkee
Roorkee, India, *Defence Research and
Development Organization, Delhi, India*

14:30 **Quantum Mechanical TCAD Study of
9-4 Epitaxial SiGe Thermistor Layers**
B. G. Malm, M. Kolahdouz, F. Forsberg*, F.
Niklaus*,
*KTH Royal Institute of Technology, Kista,
Sweden, *KTH Royal Institute of Technology,
Stockholm, Sweden*

14:50 **Transient State in the Affinity-Based
9-5 Biosensor: A Simulation and Experimental
Study**
J.-M. Woo, S. H. Kim, Y. J. Park,
*Seoul National University, Seoul, Republic of
Korea*

15:10 Coffee Break

THURSDAY, SEPTEMBER 6

Session 10 – Process and Device Effects

Chairperson: A. Burenkov, *Fraunhofer IISB*

13:30 **Resist Diffusion Model for Fast and Accurate
10-1 sub-20nm Lithography Simulation**
V. Axelrad, K. Tsujita*, K. Mikami*, R.
Nakayama*,
*Sequoia Design Systems Inc., CA,
Canon Inc., Japan

13:50 **An Improved 3D Monte Carlo Simulation of
10-2 Reaction Diffusion Model for Accurate
Prediction of the NBTI Stress/Relaxation**
S. Choi, Y. J. Park, C.-K. Baek*, S. Park*,
*Seoul National University, Seoul, Korea,
POSTECH, Pohang, Korea

14:10 **Simulations of Local Oxidation
10-3 Nanolithography by AFM Based on the
Generated Electric Field**
L. Filipovic, S. Selberherr,
TU Wien, Wien, Austria

14:30 **Accurate Simulation of Doping-Dependent
10-4 Silicide Contact Resistance Using Nano-
contact Test Structure for 22nm-node and
Beyond**
S.-D. Kim, E. Alptekin, S. Jain, H. Shang,
A. Scholze*, S. Furkay*, D.-I. Lee, C. Lavoie**,
P. Solomon**, M. Raymond***,
*IBM SRDC, Hopewell Junction, NY, * Essex
Junction, VT, **IBM Research Division,
Yorktown Heights, NY, ***Globalfoundries Inc.,
Albany, NY*

14:50 **A Comprehensive Solution for Process
10-5 Variation Characterization and Modeling**
C.-K. Lin, C. Hsiao, HC Tseng, M.-C. Jeng,
*Taiwan Semiconductor Manufacturing Company,
Hsin-Chu County, Taiwan*

15:10 Coffee Break

THURSDAY, SEPTEMBER 6

Session 11 – New Developments in Modeling

Chairperson: P. Oldiges, *IBM Corporation*

- 15:30 **New Developments in a Finite-Volume
11-1 Electro-Thermal Solver Coupled with the
Level Set Method to Study Crystallization
Mechanisms in PCM Devices**
O. Cueto, G. Navarro, V. Sousa, L. Perniola, A.
Glière,
*CEA, LETI, MINATEC Campus, Grenoble,
France*
- 15:50 **Modeling Statistical Variability with the
11-2 Impedance Field Method**
K. El Sayed, E. Lyumkis, A. Wettstein*,
*Synopsys Inc., Mountain View, CA, *Synopsys
Switzerland LLC, Zurich, Switzerland*
- 16:10 **Simulating the Random Dopant Effect: A New
11-3 Three-Dimensional Monte Carlo Approach**
K. Wei, X. Liu, G. Du, E. James*,
*Peking University, Beijing, China,
Global Foundries, Milpitas, USA
- 16:30 **Development of Predictive Model and Circuit
11-4 Simulation Methodology for Negative Bias
Temperature Instability Effects**
C. Ma, H. J. Mattausch, M. Miyake, M. Miura-
Mattausch, T. Iizuka*, K. Matsuzawa*, S.
Yamaguchi*, T. Hoshida*, A. Kinoshita*, T.
Arakawa*, J. He**,
*Hiroshima University, Hiroshima, Japan,
*Semiconductor Technology Academic
Research Center, Yokohama-shi, Japan,
**PKU-HKUST Shenzhen-Hong Kong
Institution, Shenzhen, China*
- 16:50 **A Self-Consistent Electro-Thermo-
11-5 Mechanical Device Simulator based on the
Finite-Element Method**
E. Patrick, D. Horton, M. Griglione, M. E. Law,
University of Florida, Gainesville, FL
- 18:30 Conference Dinner

THURSDAY, SEPTEMBER 6

Session 12 – Devices: GaN and Magnetic

Chairperson: A. Akturk, *University of Maryland*

- 15:30 **Modeling InGaN Disk-in-Wire LEDs:
12-1 Interplay of Quantum Atomicity and
Structural Fields**
K. Yalavarthi, V. Chimalgi, S. Sundaresan,
S. Ahmed,
*Southern Illinois University at Carbondale,
Carbondale, IL*
- 15:50 **A Robust and Efficient MTJ-based Spintronic
12-2 IMP Gate for New Logic Circuits and Large-
Scale Integration**
H. Mahmoudi, V. Sverdlov, S. Selberherr,
TU Wien, Wien, Austria
- 16:10 **Study of Self-Accelerating Switching in MTJs
12-3 with Composite Free Layer by Micromagnetic
Simulations**
A. Makarov, V. Sverdlov, S. Selberherr,
TU Wien, Wien, Austria
- 16:30 **Carrier Dynamics Study of Lateral Scaling
12-4 and the Limiting High-Frequency
Performance of GaN-HEMTs**
R. Soligo, D. Guerra, D. K. Ferry, S. M.
Goodnick, M. Saraniti,
Arizona State University, Tempe, AZ
- 16:50 **Influence of Shielding on the Thermal
12-5 Characteristics of GaN HEMTs**
B. Padmanabhan, D. Vasileska, S. M. Goodnick,
Arizona State University, Tempe, AZ
- 18:30 Conference Dinner

FRIDAY, SEPTEMBER 7

Session 13 – Energy Related Devices
and Novel Structures

Chairperson: G. Wachutka, *Munich University of
Technology*

- 08:30 **Limitations and Potential Li-Air Batteries:**
13-1 A Simulation Prediction
M. Mehta, V. V. Bevara, P. Andrei, J. Zheng,
*Florida A&M University and Florida State
University, Tallahassee, FL*
- 08:50 **Optics and Device Simulation of Surface**
**13-2 Plasmonic Enhancement of Organic Solar Cell
Performance using Silver Nano-Prisms**
W. Jiang, D. S. Ginger, M. Salvador, S. T.
Dunham,
University of Washington, Seattle, WA
- 09:10 **Simulation Study of Rectifying Antenna**
**13-3 Structure for Infrared Wave Energy
Harvesting Applications**
X. Shao, N. Goldsman*, N. Dhar**, F. Yesilkoy,
A. Akturk*, S. Potbhare*, M. Peckerar,
University of Maryland, College Park, MD,
**CoolCAD Electronics LLC, College Park, MD,*
***Defense Advanced Research Projects Agency,
Microsystems Technology Office, Arlington, VA*
- 09:30 **Toward 44% Switching Energy Reduction for**
13-4 FinFETs with Vacuum Gate Spacer
K. Wu*, A. Sachid**, F.-L. Yang, C. Hu**,
*National Nano Device Laboratories, Hsinchu,
Taiwan, *National Center for High-Performance
Computing, Hsinchu, Taiwan, **University of
California, Berkeley, CA*
- 09:50 **Non-Hysteretic Negative Capacitance FET**
**13-5 with Sub-30mV/dec Swing over 10⁶X Current
Range and I_{ON} of 0.3mA/μm without Strain
Enhancement at 0.3V V_{DD}**
C.W. Yeung, A. I. Khan, J.-Y. Cheng*, S.
Salahuddin, C. Hu,
University of California, Berkeley, CA,
**National Taiwan University, Taipei, Taiwan*
- 10:10 Coffee Break

FRIDAY, SEPTEMBER 7

Session 14 – Physical Level Circuit Simulation

Chairperson: T. Kurusu, *Toshiba Corporation*

- 08:30 **Correlation-Aware Analysis of the Impact of**
14-1 Process Variations on Circuit Behavior
A. Burenkov, E. Baer, J. K. Lorenz, C. Kampen*,
*Fraunhofer Institute for Integrated Systems and
Device Technology IISB, Erlangen, Germany,*
**Fraunhofer Institute for Integrated Systems and
Device Technology IISB, now with Infineon
Technologies, Munich, Germany*
- 08:50 **TCAD Study of Electromigration Failure**
14-2 Modes in Sn-Based Solder Bumps
H. Ceric, R. L. de Orio, S. Selberherr,
TU Wien, Wien, Austria
- 09:10 **Modeling of Electromigration Induced**
**14-3 Resistance Change in Three-Dimensional
Interconnects with Through Silicon Vias**
R. L. de Orio, H. Ceric, S. Selberherr,
TU Wien, Wien, Austria
- 09:30 **Full-TCAD Device Simulation of CMOS**
14-4 Circuits with a Novel Half-Implicit Solver
D. Gong, C. Shen,
Cogenda Pte Ltd, Singapore
- 09:50 **Investigation of the Impact of Random Dopant**
**14-5 Fluctuation on Static Noise Margin of 22nm
SRAM**
S. Q. Xu, K. Xiu*, P. Oldiges*,
Cornell University, Ithaca, NY,
**IBM Corporation, Hopewell Junction, NY*

10:10 Coffee Break

FRIDAY, SEPTEMBER 7

Session 15 – Devices: FinFETs

Chairperson: C. Weber, *Intel Corporation*

- 10:30 **Atomistic Analysis of Electrical Performance of Highly Scaled Si_{1-x}Ge_x p-FinFETs**
15-1 B. Behin-Aein, A. Paul, S. Mehrotra, B. Sahu*, K. Akarvardar*, A. Jacob*, Z. Krivokapic, G. Klimeck**,
*Global Foundries, Sunnyvale, CA, *Albany, NY, **Purdue University, W. Lafayette, IN*
- 10:50 **On the Nonlocal Modeling of Tunnel-FETs - Device and Compact Models**
15-2 K. Fukuda, T. Mori, W. Mizubayashi, Y. Morita, A. Tanabe, M. Masahara, T. Yasuda, S. Migita, H. Ota,
National Institute of Advanced Industrial Science and Technology, Ibaraki, Japan
- 11:10 **Modeling and Analysis of the Parasitic Series Resistance in Raised Source/Drain FinFETs with Polygonal Shaped Epitaxy**
15-3 C.-W. Sohn, C. Y. Kang, R.-H. Baek, P. Kirsh, R. Jammy, M.-D Ko*, D.-Y. Choi*, H. C. Sagong*, E.-Y. Jeong*, C.-K. Baek*, J.-S. Lee*, Y.-H. Jeong*, J. C. Lee**,
*SEMATECH, Albany, NY, *Pohang University of Science and Technology, Pohang, South Korea, **University of Texas at Austin, Austin, TX*
- 11:30 **Compact Models for Real Device Effects in FinFETs**
15-4 S. Venugopalan, M. A. Karim, A. M. Niknejad, C. Hu, D. D. Lu*,
*University of California, Berkeley, CA, *IBM T.J. Watson Research Center, Yorktown Heights, NY*
- 11:50 **RTS Amplitude Distribution in 20nm SOI FinFETs Subject to Statistical Variability**
15-5 X. Wang, A. R. Brown*, B. Cheng, A. Asenov*,
*University of Glasgow, Glasgow, UK, *Gold Standard Simulations Ltd., Glasgow, UK*
- 12:10 Lunch on your own

FRIDAY, SEPTEMBER 7

Session 16 – Devices and Transport Effects

Chairperson: D. Esseni, *University of Udine*

- 10:30 **A Simple, Unified 3D Stress Model for Device Design in Stress-Enhanced Mobility Technologies**
16-1 A. Kumar, K. Xiu, W. Haensch, R. Robison*, M. Bajaj**, J.B. Johnson*, S. Furkay*, R.Q. Williams*,
*IBM T. J. Watson Research Center, Yorktown Heights, NY, *IBM Semiconductor Research and Development Center, Essex Junction, VT, **Bangalore, India*
- 10:50 **Impact of Line-Edge Roughness on Electrical Resistivity in Decananoscale Copper Wires: A Monte Carlo Study**
16-2 T. Kurusu, H. Tanimoto, M. Wada, A. Isobayashi, A. Kajita, N. Aoki, Y. Toyoshima,
Toshiba Corporation, Isogo, Yokohama, Japan
- 11:10 **Multi-Via Electromigration Lifetime Model**
16-3 D. Li, Z. Guan, M. Marek-Sadowska, S. R. Nassif*,
*University of California, Santa Barbara, CA, *IBM Research-Austin IBM, Austin, USA*
- 11:30 **Stochastic Simulation of Forming, SET and RESET Process for Transition Metal Oxide-based Resistive Switching Memory**
16-4 P. Huang, B. Gao, B. Chen, F. Zhang, L. Liu, G. Du, J. Kang, X. Liu,
Peking University, Beijing, China
- 11:50 **On the Design of 2-port SRAM Memory Cells Using PNP Diodes for VLSI Application**
16-5 X. Tong, H.Wu, Q. Liang, H. Zhong, H. Zhu, D. Chen, T. Ye,
Institute of Microelectronics of Chinese Academy of Sciences, Beijing, PR China
- 12:10 Lunch on your own
- Tutorials and Demonstration**
- 13:30 **nanoHUB.org: Open Access Device and Process Simulation and Much More**
Jean Michel D. Sellier*, Lynn K. Zentner, and Gerhard Klimeck, *Purdue University West Lafayette, IN*
- 14:30 **CoolSPICE: A Circuit Simulation Tool for Specialized Applications** CoolCAD Electronics LLC
Akin Akturk, *CoolCAD Electronics LLC, College Park, MD*

WEDNESDAY, SEPTEMBER 5

POSTER SESSIONS

Chairpersons: V. Axelrad, *Sequoia Design Systems*
N. Goldsman, *University of Maryland*

- P-1 Modeling the Distributed Physical Effects in the Intrinsic Base of SiGe HBTs Using Transmission Line Concepts**
G. Alvarez-Botero, R. Torres-Torres, R. Murphy-Arteaga, *National Institute for Astrophysics, Optics and Electronics, Tonantzintla, Puebla, Mexico*
- P-2 Design and Simulation of a Pressure Sensor Based on Optical Waveguides for Applications in Hydraulic Fracturing**
R. Ambrosio, G. Lara, A. Jimenez, J. Mireles, J. Ibarra, A. Heredia*,
*Universidad Autónoma de Ciudad Juárez, Ciudad Juárez, Mexico, *Universidad UPAEP, Puebla, Mexico*
- P-3 Quantum Drift Diffusion and Quantum Energy Simulation of Nanowire Transistors**
O. Badami, N.Kumar, D. Saha, S. Ganguly,
Indian Institute of Technology Bombay, Mumbai, India
- P-4 GaN MOSFET: Projections for High Power High Frequency Applications**
K. Bothe, P. von Hauff, D. Barlage, A. Afshar, A. Foroughi-Abari, K. Cadien,
University of Alberta, Edmonton, Canada
- P-5 Analysis of the Frequency Dependent Gate Capacitance in CNTFETs**
M. Claus, S. Blawid*, P. Sakalas, M. Schroter**,
*Technische Universität Dresden, Germany, *Universidade de Brasília, Brazil, **University of California, San Diego, CA*
- P-6 Physics of Optimized High Current ESD Performance of Drain Extended NMOS (De-NMOS)**
A. Chatterjee, C. Duvvury*, F. Brewer,
*University of California, Santa Barbara, CA, *Texas Instruments Inc., Dallas, TX*
- P-7 Modeling Source/Drain Contact Resistance in Nanoscale MOSFETs**
E. Chen, A. C-C Wang, H.S. Chen, W.H. Hsieh, T-H Yu, T.M. Shen, J. Wu, C.H. Diaz,
Taiwan Semiconductor Manufacturing Company, Hsinchu County, Taiwan
- P-8 Process Window Definition for Power MOSFET by Transient Avalanche Device Simulation**
J. Chen, T. Henson,
International Rectifier, El Segundo, CA
- P-9 Comparison for Various Kinds of Hamiltonian in Graphene Nanoribbon Quantum Transport Calculation**
J. Ding, Q. Shao, J. Zhang, Z. Yu,
Tsinghua University, Beijing, China
- P-10 Comparison of Noise Predictions by Commercial TCAD Device Simulator to Results from a Spherical Harmonics Expansion Solver**
T. V. Dinh, D.B.M. Klaassen**, T. Vanhoucke, E. Gridelet, H. Mertens, R. van Dalen*, P.H.C. Magnee*, M. Ramonas***, C. Jungemann***,
*NXP Semiconductors Research, Leuven, Belgium, *NXP Semiconductors Nijmegen, Nijmegen, The Netherlands, **NXP Semiconductors Research, Eindhoven, The Netherlands, *** RWTH Aachen University, Aachen, Germany*
- P-11 Mobility Calculation for Nanoscale Multi-Gate FETs with Arbitrary Two-Dimensional Cross Section with a Homogeneous Channel Including Strain Effects**
S.-M. Hong, W. Choi, W. Lee*, Y. T. Kim*, U. Kwon*, K.-H. Lee*, Y. Park*,
*Samsung Semiconductor Inc., San Jose, CA, *Samsung Electronics, Hwasung-si, Gyeonggi-do, Korea*
- P-12 Nickel Silicide Growth Model: Coupling of Diffusion with Level Set Methods**
A. Kumar, M. Law,
University of Florida, Gainesville, FL
- P-13 Analysis of Tunneling Characteristics Through Hetero Interface of InAs/Si Nanowire Tunneling Field Effect Transistors**
Y. Miyoshi, M. Ogawa, S. Souma, H. Nakamura*,
*Kobe University, Nada, Kobe, Japan, * Tokyo Research Lab, IBM-Japan, Yamato, Kanagawa, Japan*

- P-14 Interplay between the Electrical and Thermal Transport of Silicon Nanoscale MOSFETs**
M. Mohamed, Z. Aksamija, W. Vitale, F. Hassan, U. Ravaioli, *University of Illinois at Urbana-Champaign, Urbana, IL*
- P-15 A 3D Simulation of the Lateral Charge Spreading Effect in Charge Trapping NAND Flash Memory**
S. Park, S. Choi, K.S. Jeon, H.J. Kim, S. M. Rhee, I. Yoon, Y.J. Park, *Seoul National University, Seoul, Korea*
- P-16 TCAD Electrical Parameters Extraction on Through Silicon Via (TSV) Structures in a 0.35 μ m Analog Mixed-Signal CMOS**
F. Roger, J. Kraft, K. Molnar, R. Minixhofer, *ams AG, Premstaetten, Austria*
- P-17 Fast Perturbative Treatment for Efficient Nano-Scale Device Simulation Based on Bridge-Function Pseudo-Spectral Method**
Y. Saito, H. Fujikawa, S. Souma, M. Ogawa, *Kobe University, Nada, Kobe, JAPAN*
- P-18 NEMO5, a Parallel, Multiscale, Multiphysics Nanoelectronics Modeling Tool**
J.M.D. Sellier, J.E. Fonseca, T. Kubis, M. Povolotskyi, Y.W. He, H. Ilatikhameh, Z. Jiang, S.G. Kim, D.F. Mejia, P. Sengupta, Y. P. Tan, G. Klimeck, *Purdue University West Lafayette, IN*
- P-19 3D Simulations of Random Dopant Induced Threshold Voltage Variability in Inversion-Mode In_{0.53}Ga_{0.47}As GAA MOSFETs**
N. Seoane, A. Garcia-Loureiro, E. Comesana, R. Valin, G. Indalecio, M. Aldegunde*, K. Kalna*, *University of Santiago de Compostela, Santiago de Compostela, Spain, * Swansea University, Swansea, United Kingdom*
- P-20 Stress-induced Migration of Electroplated Copper Thin Film Interconnections Depending on Thermal History**
K. Suzuki, H. Miura, O. Asai, N. Saito, N. Murata, *Tohoku University, Sendai, Japan*
- P-21 A Flexible Execution Framework for High-Performance TCAD Applications**
J. Weinbub, K. Rupp, S. Selberherr, *TU Wien, Wien, Austria*
- P-22 A TCAD Study of Substrate Dopant for Extremely Thin SOI MOSFETs with Ultra-Thin Buried Oxide**
H. Wu, X. Tong, M. Xu, W. Xiao, B. Wu, H. Zhu, Q. Liang, L. Zhao, H. Zhong, Z. Luo, H. Yin, Q. Xu, C. Zhao, D. Cheng, T. Ye, H. Yu*, *Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China, *Nanyang Technological University, Singapore*
- P-23 Simulation of Phonon-Induced Mobility under Arbitrary Stress, Wafer and Channel Orientations and its Application to FinFET Technology**
K. Xiu, P. Oldiges, *IBM Semiconductor Research and Development Center, Hopewell Junction, NY*
- P-24 Correction of the RTN Model considering 3D Effect of Single Trapped Charge**
I. Yoon, S. Choi, S. Rhee, H. Kim, S. Park, Y. J. Park, *Seoul National University, Seoul, Rep. of Korea*
- P-25 Improvement of Drive Current Prediction in FinFET Using Full 3D Process/Stress/Device Simulations**
T-H Yu, J-H Ho, C-W Liu, C-C Wang, W-Y Chen, H-S Chen, K-H Wu, K-C Tu, W-H Hsieh, C-F Huang, T-M Shen, Y-M Sheu, J. Wu, C.H. Diaz, *Taiwan Semiconductor Manufacturing Company, Taiwan*