SISPAD 2010

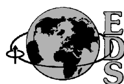
15th International Conference on Simulation of Semiconductor Processes and Devices

September 6-8, 2010
Bologna, Italy

ARCES Research Center
University of Bologna

Technically Co-Sponsored by

IEEE



SISPAD 2010 TIMETABLE

Monday, September 6, 2010

Time	Room A	Room B
09.00	Conference Opening Room A	
09.20	Session 01-A Plenary Room A	
10.00	Session 02-A Room A Graphene	Session 02-B Room B Process: Metallization & Interconnects
10.40	Coffee break	
11.20	Session 03-A Room A Nanoelectronics and Interfaces	Session 03-B Room B Process: Deposition & Etching
12.40	Lunch	
14.00	Session 04-A Plenary presentation Room A	
14.40	Session 05-A Room A Nanowires: Transport Models I	Session 05-B Room B TCAD: Applications I
15.20	Coffee break	
15.40	Session 06-A Room A Nanowires: Transport Models II	Session 06-B Room B TCAD: Applications II
19.00	Welcome party	

Tuesday, September 7, 2010

Time	Room A	Room B
09.00	Presentation of the 2011 Edition Room A	
09.20	Session 07-A Plenary presentation Room A	
10.00	Session 08-A Room A Variability: Simulation Approaches	Session 08-B Room B TCAD: Simulation Approaches I
10.40	Coffee break	
11.20	Session 09-A Room A Variability: CMOS & Memories	Session 09-B Room B TCAD: Simulation Approaches II
12.40	Lunch	
14.00	Session 10-A Plenary presentation Room A	
14.40	Session 11-A Room A Variability: SOI & Nanowires	Session 11-B Room B Process: Ion Implantation
15.20	Coffee break	
15.40	Session 12-A Room A Nanowires: RF & Strain	Session 12-B Room B Process: Interfaces & Electromigration
19.50	Gala dinner	

Wednesday, September 8, 2010

Time	Room A	Room B
09.00	Session 13-A Plenary presentation Room A	
09.40	Session 14-A Room A Memories I	Session 14-B Room B Compact Modeling
10.40	Coffee break	
11.20	Session 15-A Room A Memories II	Session 15-B Room B TCAD: Transport Models
12.40	Lunch	
14.00	Session 16-A Plenary presentation Room A	
14.40	Session 17-A Room A Numerics for Device Simulation	Session 17-B Room B Sensors and MEMS

Tuesday, September 9, 2010

Time		
08.30	Workshop I	Workshop II

WELCOME

On behalf of the Organizing Committee, we would like to welcome you to the 2010 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2010) held in Bologna, Italy, on September 6-8, 2010.
SISPAD provides an international forum for presentation of the leading-edge research and development results in the area of process and device simulation. SISPAD is held annually, with the location of the conference circulating among Asia, Europe, and U.S.A., and is one of the longest running conferences devoted to technology computer-aided design (TCAD). This year, the 15th SISPAD has been organized by the ARCES Research Center of the University of Bologna, Italy, with the technical co-sponsorship of the IEEE Electron Devices Society (EDS).
The main themes of interest for SISPAD 2010 are: i) Electronic transport in semiconductor materials and devices, ii) Device modeling and simulation, iii) Sensors, biosensors, and (bio)-electromechanical systems simulation, iv) Process and equipment modeling and simulation, v) Compact models, vi) Physical-level circuit simulation, vii) New algorithms for process and device modeling.
This year, the conference program features 6 invited papers and 62 oral presentations which were carefully selected out of a total of 116 abstracts submitted from all over the world. These papers disclose new and interesting concepts for the simulation and understanding of processes and devices. Also, two workshops are being organized on Thursday, September 9, 2010 on the simulation and characterization of statistical CMOS variability and reliability, and on steep slope switches.
We would like to thank the Technical Program Committee for their efforts in reading, evaluating and selecting the accepted papers. We wish to express our sincere appreciation to all of the members of the Organizing Committee for planning and organizing every single detail of this conference. We are very grateful to all invited speakers and authors for contributing to the success of the conference. A special thank is due to Profs. A. Asenov and A. Ionescu for setting up the program of the satellite workshops. It is with great pleasure that we extend a warm welcome to everyone attending SISPAD 2010.

Giorgio Baccarani
Massimo Rudan

Conference Chairs

About Bologna

Located in Italy's scenic Emilia-Romagna area, Bologna is known as a city of culture, with large public squares, offering a close-up look and many impressive buildings and landmarks. Highlights in Bologna include many historic buildings with magnificent medieval architecture and endless red tiled roofs. Bologna is also home to the oldest University in the whole of Europe.

Places to visit in Bologna

- Piazza Maggiore, a large public square in the heart of the oldest part of Bologna, surrounded by Renaissance-style architecture and offering a mixture of street entertainment, coffee shops and bars.
- Basilica di S. Petronio, a late Italian Gothic style with its unfinished façade, whose construction started in 1390. It was the site of numerous historic events, the most important of which is the coronation of Charles V as the emperor of the Holy Roman Empire in 1530.
- Fontana del Nettuno, Bologna's spectacular 16th-century Fountain of Neptune, which connects the Piazza Maggiore with the neighboring Piazza del Nettuno.
- University Quarter, located in the center of Bologna and overflowing with bars, cafés and restaurants, home to Europe's most historic university, dating back to more than 900 years.
- Torre degli Asinelli and Torre Garisenda, two iconic leaning towers which have become symbols of Bologna, standing in Piazza di Porta Ravegnana.
- Palazzo Comunale, Bologna's historic town hall located in Piazza Maggiore, housing a large and important collection of paintings, many of which were painted by well-known artists.
- Tombe dei Glossatori, graves of Bolognese jurists located in Piazza San Domenico and Piazza Malpighi, locally referred to as the Glossatori Tombs as they used to add glosses within the lines of law textbooks.
- Archaeological Museum, known locally in Bologna as the Museo Civico Archeologico and home to many important local treasures.
- Basilica di Santo Stefano, featuring a complex of connecting chapels and courtyards.

Climate

September is usually a sunny month with an average temperature of 15-25° C. Since rain showers are possible, light clothing and a raincoat are recommended.

Time Zone

Central European Summer time (GMT+2).

Electricity

Electricity is supplied at 220 Volts, 50 cycles AC. Only round-pin plugs can be used in Italian sockets. Please use an adapter plug and a voltage converter if you are using 110/120 volt appliances.

Banks

Typical opening hours: Monday: 8:00-13:30 and 14:00-16:30; Tuesday: 8:00-16:30; Wednesday: 8:00-13:30 and 14:00-16:30; Thursday: 8:00-14:30; Friday: 8:00-13:30.

Post Office

Opening hours: 8:30 to 13:30 from Mondays to Saturdays.

Shopping

Shops generally open from Monday through Saturday at 9:00 - 13:00. and 15:30 - 19:30. On Monday morning, Thursday afternoon and Sunday most shops are closed.

Emergency in Italy

In case of emergency dial 118 for ambulance and 113 for police.

Conference Site

The SISPAD 2010 Conference will be held at

Royal Hotel Carlton
Via Montebello, 8
40121 Bologna, Italy
Tel. +39 051 249 361
Fax +39 051 249 724

CONFERENCE REGISTRATION

Conference Registration

The Conference registration covers admission to all technical sessions during the Congress, conference material (Program, abstract book, congress bag, USB pen with the accepted papers and certificate of attendance), welcome cocktail on Monday 6th afternoon, coffee breaks, lunches, gala dinner.

Registration Fees

Conference Registration Fees

	Before July 4	After July 4
Full	€ 600	€ 650
IEEE Member	€ 550	€ 600
Student	€ 550	€ 600

Workshop Registration Fees

Workshop 1: "Simulation and Characterization of Statistical CMOS Variability and Reliability" Organizers: A. Asenov, S. Nassif, G. Baccarani Duration: Full day	€ 100
Workshop 2: "Simulation and Characterization of Steep-Slope Switches (SSS)" Organizers: A. Ionescu, G. Baccarani Duration: Full day	€ 100

Accompanying Persons

Registration Fee (including Welcome Party and Gala Dinner)	€ 130
Tour to Ravenna	€ 45
Downtown Bologna	€ 15

Registration Desk

Reception and on-site registration will be open on Sunday September 5, 2010 at the Royal Hotel Carlton in Bologna at 17:00 and during the next three conference days from 8:30 in the morning.

Workshop Registration

The on-site registration will be open starting from Sept. 8 at 17:00.

SOCIAL PROGRAM

Monday, September 6

Welcome party at the Royal Hotel Carlton garden beginning from 19:00.

Tuesday, September 7

Gala dinner at Palazzo De' Rossi, Sasso Marconi. Buses leaving at 19:50 from Royal Hotel Carlton.

Wednesday, September 8

Cocktail for workshop participants at 18:00 in the Conference foyer.

Excursions

Monday, September 6

Tour to Ravenna: bus leaving at 13:00 from the Royal Hotel Carlton. Guided visit to Basilica di S. Vitale, Mausoleo di Galla Placidia, Battistero Neoniano, Basilica di S. Apollinare Nuovo, Mausoleo di Teodorico.

Tuesday, September 7

Sightseeing in Bologna: meeting place at 9:30 in Piazza Maggiore, next to the Neptune fountain. Guided visit to Basilica di S. Petronio, Archiginnasio, Medieval Market, Mercanzia Palace and Santo Stefano.

Conference Language

The working language for the conference will be English and English will be used for all presentations and printed material.

Lecture Presentation Information

The duration of a presentation slot is 20 minutes. Speakers are advised to keep their own presentation within 17 minutes, in order to leave 3 minutes for questions from the audience.
An LCD projector & computer (Windows Vista, MS Powerpoint & Adobe Acrobat Reader) will be available in every session room for regular and invited presentations. Neither overhead projector, 35mm slides projector nor VHS videotape player will be available.

Preparation of Visuals

Please note that speakers using computer projection must bring a memory stick containing their presentation.
Files can be uploaded to the local PCs in the lecture rooms during the breaks between the sessions. To avoid software compatibility problems (MS Powerpoint), speakers are advised to save their Powerpoint presentation AND bring a backup PDF version of their presentation.
Speakers should arrive in their session room 15 minutes BEFORE the start of their session to report to the chair person. A proctor will also be available in case you need technical assistance.
Speakers are strongly encouraged to review their presentation in advance to avoid any last minute problems. Some PCs will be available from Sunday through Thursday.

Internet Service

Lecture halls and the foyer are served by a Wi-Fi network. Access cards can be purchased at the Hotel reception desk at the cost of € 10,00 for one hour and € 22,00 for 24 hours.

Satellite Workshops

The Conference is followed by two workshops scheduled on Thursday, September 9. Workshop no. 1 is entitled: **“Simulation and Characterization of Statistical CMOS variability and Reliability”** and is organized by Prof. A. Asenov**.** Workshop no. 2 is entitled: **“Simulation and Characterization of Steep-Slope Switches”** and is organized by Prof. A Ionescu.

ORGANIZING COMMITTEE

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Giorgio Baccarani	University of Bologna
Massimo Rudan	University of Bologna

Technical Program Chair

Massimo Rudan	University of Bologna

Past Chairs

K. Mayaram	Oregon State University
V. Axelrad	Sequoia Design Systems

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Rita Mambelli
ARCES - University of Bologna
Via Toffano 2/2
40125 Bologna, Italy
Phone +39 051 209 5400
Fax +39 051 209 5410
email: sispad2010@arces.unibo.it

COMMITTEES

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S. Yamakawa	Sony	Japan

Transport and Noise Properties of Graphene-Based Transistors Revealed Through Atomistic Modeling

G. Iannaccone, A. Betti, G. Fiori
University of Pisa, Italy

In this talk we will discuss an intriguing set of transport and noise properties of graphene-based transistors that can be investigated in a direct way with atomistic modeling - Non-Equilibrium Green's Functions with a Tight-Binding Hamiltonian - and are not directly accessible with models based on a higher level of physical abstraction. As far as noise is concerned, we will show the impact of electron-electron interaction and of interband transitions in enhancing the channel noise of FETs based on small-gap nanoribbons or nanotubes. Then, we shall discuss the achievable electron mobility in channels based on graphene nanoribbons with realistic imperfections. Finally, we will discuss how the small gap and small density of states of bilayer graphene can be used to design tunnel FETs with extremely steep subthreshold slope.

Giuseppe Iannaccone received the M.S. and Ph.D. degrees in Electrical Engineering in 1992 and 1996, respectively, from the University of Pisa, Pisa, Italy. Since 2001 he is an Associate Professor of Electronics at the Department of Information Engineering of the same University. He has coordinated a few European and national projects involving multiple partners and acted as principal investigator in several research projects funded by public agencies and by private organizations. He has authored and coauthored more than 120 papers published in peer-reviewed journals and more than 80 papers in conference proceedings. His interests include transport and noise in nanoelectronic and mesoscopic devices, development of TCAD tools and design of extremely low-power circuits and systems for RFID and ambient-intelligent applications.

Si Nanowire Device and its Modeling

H. Iwai[1], K. Natori[1], K. Kakushima[1], P. Ahmet[1], K. Shiraishi[2], J. Iwata[2], A. Oshiyama[3], K. Yamada[4], K. Ohmori[4]
[1]Tokyo Institute of Technology, Japan; [2]Tsukuba University, Japan; [3]University of Tokyo, Japan; [4]Waseda University, Japan

Si nanowire FET could be regarded as the ultimate structure of transistors for use for future CMOS integrated circuits because of good control of the off-leakage current with high conduction current at on-stage. It is also a big advantage that the current Si integrated circuit technology can be used almost as it is for the fabrication of the nanowire FETs. However, it is still in a research level and there are many

many unknown things because of its complicated conduction mechanism based on the band structure strongly dependent of the diameter, shape, or crystal orientation of the nanowire, and its immature technology. In this talk, current status of Si nanowire FET research is explained.

Hiroshi Iwai received the B.E. and Ph.D. degrees in electrical engineering from the University of Tokyo and worked in the research and development of integrated circuit technology for 26 years in Toshiba and 11 years in Tokyo Institute of Technology. He is now a professor of Frontier Research Center and Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology. Since joining Toshiba, he has developed several generations of high density static RAM's, dynamic RAM's and logic LSI's including CMOS, bipolar, and Bi-CMOS devices. He has authored and coauthored more than 850 journal and conference papers. His current research interest is future mainstream CMOS technologies, such as high-k with below 0.5nm EOT, and Si nanowire FETs. He served as the president of IEEE Electron Devices Society. He is currently the director of IEEE Division I. He is a recipient of IEEE Paul Rappaport Award and IEEE J. J. Ebers Award.

Cost-Effective Variability Reduction Approaches to Enable Future Technology Nodes

A. Strojwas
Carnegie Mellon University, United States

This paper will describe a comprehensive study of the primary sources of variability and their effects on active devices, interconnect and ultimately product performance and yield. We will first provide an overview of process variability sources and the resulting random and systematic variability down to 28nm. Next we will present the evolution of yield loss mechanisms and characterization methods for assessing process-design interactions with a focus on layout printability for 28nm and below. To overcome the impact of such a high level of variability on product performance, circuit designers should adopt advanced statistical process characterization, performance verification and optimization techniques. We will describe robust design methodology requirements based on statistical optimization approaches with realistic process/device characterization for logic, memory and analog circuits. We will then present an extremely regular layout methodology for 28nm and below. The key to the practical implementation of this methodology is the creation of a design fabric with a limited number of printability friendly patterns that enable the co-optimization of circuit, process and design.

Andrzej J. Strojwas is Joseph F. and Nancy Keithley Professor of Electrical and Computer Engineering at Carnegie Mellon University. Since 1997 he has served as Chief Technologist at PDF Solutions, Inc. He has held positions at Harris Semiconductor Co., AT&T Bell Laboratories, Texas Instruments, NEC, HITACHI, SEMATECH, KLA-Tencor and PDF Solutions, Inc. He received multiple awards for the best papers published in the IEEE *Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *IEEE Transactions on Semiconductor Manufacturing* and IEEE-ACM Design Automation Conference. He is also a recipient of the SRC Inventor Recognition Award. He was the Editor of the IEEE *Transactions on CAD of ICAS* from 1987 to 1989. He served as Technical Program Chairman of the 1988 ICCAD and Conference Chairman of the 1989 ICCAD. In 1990 he was elected IEEE Fellow.

Quasi-Ballistic Transport in Nano-Scale Devices: Boundary Layer, Potential Fluctuation, and Coulomb Interaction

N. Sano
University of Tsukuba, Japan

We briefly review the singular nature of the Boltzmann transport equation leading to the boundary layers around the virtual source and provide its physical interpretation that clarifies the physical mechanism of quasi-ballistic transport in nanoscale devices. Theoretical prediction is then confirmed by the Monte Carlo simulations under double-gate MOSFETs including the full Coulomb interaction. It is explicitly demonstrated that the long-range part of the Coulomb interaction becomes of greater importance in nanoscale channels in determining the device performance by showing the degradation of transconductance by the dynamical Coulomb interaction of the channel electrons with plasmon in the source or drain.

Nobuyuki Sano received the Ph.D. degree in physics from Auburn University, Auburn, U.S.A., in 1988. From 1988 to 1995, he was a Research Scientist with NTT LSI Laboratories, Japan and since 1995 he is with the Institute of Applied Physics, the University of Tsukuba, Japan, where he is a Professor. He has been working on the theory and simulations of electron transport under nanoscale semi-conductor structures by employing the Drift-Diffusion and Monte Carlo simulations. He is also interested in the theory of quantum transport in nanoscale devices from the viewpoint of many-body effects.

Future High Density Memories for Computing Applications: Device Behavior and Modeling Challenges

G. Spadini, I. Karpov, D. Kencke
Intel Corporation, United States

Computer memory architecture is becoming more complicated due to the increased performance of processors and the limitation in cost / power / speed offered by existing I/O subsystems and their respective memory devices. Hard drives provide cheap storage with high latency and DRAM provides expensive and power hungry storage at low latency. A significant research effort is underway to find technologies that provide low latency data storage at high density with low cost and low power consumption. A brief review of the field is presented and the challenges of some of the most promising technologies are reviewed with the aim to highlight gaps in our knowledge of device behavior and in modeling.

Gianpaolo Spadini received the Dr degree in Electronic Engineering from the University of Bologna in 1973. He started his career at the CNR-LAMEL laboratory in Italy, then was engaged in device and process technology development in the Agrate site of SGS (now ST). In 1980 he moved to the technology development group of the recently founded VLSI Technology corporation in Santa Clara, CA. He was later responsible for the technology development activities of Microchip Technology and Zilog. Since 2005 he is the Director, Novel NVM Technologies at Intel, Santa Clara, CA responsible for the development of phase change memory technologies.

Solving Boltzmann Transport Equation Without Monte-Carlo Algorithms - New Methods for Industrial TCAD Applications

B. Meinerzhagen[1], A. Pham[1], S. Hong[2], C. Jungemann[2]
[1]*TU Braunschweig, Germany;* [2]*Bundeswehr University, Germany*

The Drift-Diffusion Model is still by far the most frequently used numerical device model in industry today. One important reason for this success is the robust numerical implementation of this model providing CPU efficient DC, AC, transient and noise simulations with high accuracy and high convergence reliability. On the other hand many of todays design applications vary strain, crystal and channel orientation, material composition and the carrier confinement. Such applications certainly require the solution of the Boltzmann Transport Equation in order to be predictive. It will be demonstrated in this talk that with new alternative discretization

and solution methods avoiding the Monte-Carlo Algorithm many of the favorable numerical properties of the traditional Drift Diffusion Model can be transferred to numerical device models that include the solution of the Boltzmann Transport Equation.

Bernd Meinerzhagen is Full Professor and Head of the Institute for Electron Devices and Circuits at the Technical University Braunschweig, Braunschweig, Germany. He received the Dipl. Ing. degree in electrical engineering, the Dipl. Math. degree in mathematics, the Dr.Ing. degree in electrical engineering, and the “venia legendi,” all from the RWTH Aachen (Aachen University of Technology), Aachen, Germany, in 1977, 1981, 1985, and 1995, respectively. From 1978 to 1986, he worked mainly on the development of numerical device modeling codes as a Research and Teaching Assistant at the RWTH Aachen. In 1986, he joint AT&T Bell Laboratories, Allentown, PA, as a Member of Technical Staff, where he developed advanced numerical models for MOS substrate and gate currents. From 1988 to 1995 he was the Head of the Research and Development Group for Silicon technology modeling and simulation (TCAD) at the RWTH Aachen and he continued this research as Professor at the University of Bremen, Bremen, Germany between 1995 and 2003. Currently his most prominent research topic is the advanced modeling of transport and noise in nanoscale Si/SiGe devices. Several key contributions in this field have been made by him and his group in the last decade. Prof. Meinerzhagen has coauthored two books and more than 200 papers published in international journals and conference proceedings and has been a Technical Program Committee member of IEDM, ESSDERC, SISPAD, IWCE and other conferences.

NOTES

Conference Opening

Monday, September 6, 2010, 09:00-09:20
9:00 Room A

Session 01-A: Invited

Monday, September 6, 2010, 09:20-10:00
Room A
Chair: Giorgio Baccarani

9:20
01-A.1 Transport and Noise Properties of Graphene-Based Transistors Revealed Through Atomistic Modeling
G. Iannaccone, A. Betti, G. Fiori
University of Pisa, Italy

Session 02-A: Graphene

Monday, September 6, 2010, 10:00-10:40
Room A
Chair: Giorgio Baccarani

10:00
02-A.1 Quantum Transport of Dirac Fermions in Graphene Field Effect Transistors
V. Nguyen, A. Bournel, C. Chassat, P. Dollfus
Université Paris Sud, France

10:20
02-A.2 Improving Channel Mobility in Graphene-FETs by Minimizing Surface Phonon Scattering – A Simulation Study
X. Yu, J. Kang, J. Zhang, L. Tian, Z. Yu
Tsinghua University, China

Session 02-B: Process: Metallizations & Interconnects

Monday, September 6, 2010, 10:00-10:40
Room B
Chair: Herve Jaouen

10:00
02-B.1 A Kinetic Monte Carlo Study on the Dynamic Switching Properties of Electrochemical Metallization RRAMs During the Set Process
F. Pan, V. Subramanian
University of California Berkeley, United States

10:20
02-B.2 Simulation of Three Dimensional Grain Growth for Cu-Interconnects
X. Cheng, Y. Wang
Tsinghua University, China

Session 03-A: Nanoelectronics and Interfaces

Monday, September 6, 2010, 11:20-12:40
Room A
Chair: Wim Magnus

11:20
03-A.1 Fabry-Perot Oscillations in the Thermopower of Ballistic Graphene Ribbons
G. Kliros[1], P. Divari[2]
[1]Hellenic Air-Force Academy, Greece; [2]Hellenic Army Academy, Greece

11:40
03-A.2 Modeling of Thin-Film Cu(In,Ga)Se_2 Solar Cells
F. Troni, F. Dodi, G. Sozzi, R. Menozzi
Università di Parma, Italy

12:00
03-A.3 Spin-Transfer Torques: Self-Consistent Solution of the Spin-Diffusion Equation and the Landau-Lifshitz Equation
S. Possanner, N. Ben Abdallah
Paul Sabatier University, France

12:20
03-A.4 First-Principle Calculation for Luminescent-Effects of Si and Zn Impurities in GaN
X. Ji, M. Gao, Y. Wang
Tsinghua University, China

Session 03-B: Process: Deposition & Etching

Monday, September 6, 2010, 11:20-12:40
Room B
Chair: Kenichiro Sonoda

11:20
03-B.1 Topography Simulation of BiCS Memory Hole Etching Modeled by Elementary Experiments of SiO_2 and Si Etching
T. Ichikawa, D. Ichinose, K. Kawabata, N. Tamaoki
Toshiba Corporation, Japan

11:40
03-B.2 Three-Dimensional Simulation of Focused Ion Beam Processing Using the Level Set Method
O. Ertl, L. Filipović, S. Selberherr
TU Wien, Austria

12:00
03-B.3 Coupling of Monte Carlo Sputter Simulation and Feature-Scale Profile Simulation and Application to the Simulation of Back Etching of an Intermetal Dielectric
E. Baer[1],D. Kunder[1],J. Lorenz[1],M. Sekowski[2],U. Paschen[3]
[1]Fraunhofer IISB, Germany; [2]University of Erlangen-Nuernberg, Germany; [3]Fraunhofer IMS, Germany

12:20
03-B.4 Coupling of Equipment Simulation and Feature-Scale Profile Simulation for Dry-Etching of Polysilicon Gate Lines
E. Baer, D. Kunder, P. Evanschitzky, J. Lorenz
Fraunhofer IISB, Germany

Session 04-A: Invited

Monday, September 6, 2010, 14:00-14:40
Room A
Chair: Nobuyuki Sano

14:00
04-A.1 Si Nanowire Device and its Modeling
H. Iwai[1], K. Natori[1], K. Kakushima[1], P. Ahmet[1], K. Shiraishi[2], J. Iwata[2], A. Oshiyama[3], K. Yamada[4], K. Ohmori[4]
[1]Tokyo Institute of Technology, Japan; [2]Tsukuba University, Japan; [3]University of Tokyo, Japan; [4]Waseda University, Japan

Session 05-A: Nanowires: Transport Models I

Monday, September 6, 2010, 14:40-15:20
Room A
Chair: Nobuyuki Sano

14:40
05-A.1 Steep-Slope Nanowire Field-Effect Transistor (SS-NWFET)
E. Gnani, A. Gnudi, S. Reggiani, G. Baccarani
ARCES-University of Bologna, Italy

15:00
05-A.2 Molecular Dynamics Simulation on LO Phonon Mode Decay in Si Nano-Structure Covered with Oxide Films
T. Zushi[1], Y. Kamakura[2], K. Taniguchi[2], I. Ohdomari[1], T. Watanabe[1]
[1]Waseda University, Japan; [2]Osaka University, Japan

Session 05-B: TCAD: Applications I

Monday, September 6, 2010, 14:40-15:20
Room B
Chair: Wladek Grabinski

14:40
05-B.1 Modeling Gate-Pitch Scaling Impact on Stress-Induced Mobility and External Resistance for 20nm-Node MOSFETs
S. Kim[1], S. Jain[1], H. Rhee[2], A. Scholze[1], M. Yu[1], S. Lee[2], S. Furkay[1], M. Zorzi[3], F. Bufler[3], A. Erlebach[3]
[1]IBM, United States; [2]Samsung Electronics, United States; [3]Synopsys, Switzerland

15:00
05-B.2 **Schrödinger-Poisson and Monte Carlo Analysis of III-V MOSFETs for High Frequency and Low Consumption Applications**
M. Shi, J. Saint-Martin, A. Bournel, P. Dollfus
CNRS, Université Paris Sud, France

Session 06-A: Nanowires: Transport Models II

Monday, September 6, 2010, 15:40-16:40
Room A
Chair: Philippe Dolfus

15:40
06-A.1 **Coupled Monte Carlo Simulation of Transient Electron-Phonon Transport in Nanoscale Devices**
Y. Kamakura[1], N. Mori[1], K. Taniguchi[1], T. Zushi[2], T. Watanabe[2]
[1]Osaka University, Japan; [2]Waseda University, Japan

16:00
06-A.2 **A Theoretical Study of Effect of Gate Voltage on Electron-Modulated-Acoustic-Phonon Interactions in Silicon Nanowire MOSFETs**
J. Hattori[1], S. Uno[1], N. Mori[2], K. Nakazato[1]
[1]Nagoya University, Japan; [2]Osaka University, Japan

16:20
06-A.3 **Dissipative Transport in Multigate Silicon Nanowire Transistors**
N. Dehdashti, A. Kranti, I. Ferain, C. Lee, R. Yan, P. Razavi, R. Yu, J. Colinge
Tyndall National Institute, Cork, Ireland

Session 06-B: TCAD: Applications II

Monday, September 6, 2010, 15:40-16:40
Room B
Chair: Anco Heringa

15:40
06-B.1 **Optimal Design of III-V Heterostuctures MOSFETs**
A. Nainani, Z. Yuan, T. Krishnamohan, K. Saraswat
Stanford University, United States

16:00
06-B.2 **Microscopic Simulation of Electron Transport and Self-Heating Effects in InAs Nanowire MISFETs**
T. Sadi[1], J. Thobel[2], F. Dessenne[2]
[1]Technische Universitat Ilmenau, Germany;
[2]Université Lille 1, France

16:20

06-B.3 Numerical Investigation of the Total SOA of Trench Field-Plate LDMOS Devices

S. Poli[1], S. Reggiani[1], G. Baccarani[1], E. Gnani[1], A. Gnudi[1], M. Denison[2], S. Pendharkar[2], R. Wise[2]
[1]University of Bologna, Italy; [2]Texas Instruments, United States

19:00 Welcome party

Presentation of 2011 Edition

Tuesday, September 7, 2010, 09:00-09:20
9:00 Room A

Session 07-A: Invited

Tuesday, September 7, 2010, 09:20-10:00
Room A
Chair: Tibor Grasser

9:20
07-A.1 Cost-Effective Variability Reduction Approaches to Enable Future Technology Nodes
A. Strojwas
Carnegie Mellon University, United States

Session 08-A: Variability: Simulation Approaches

Tuesday, September 7, 2010, 10:00-10:40
Room A
Chair: Tibor Grasser

10:00
08-A.1 A Comparative 3D Simulation Approach with Extensive Experimental Vt/Avt Data and Analysis of LER/RDF/Reliability of CMOS SRAMs at 40-nm Node and Beyond
T. Okada, M. Sengoku, H. Aikawa, O. Fujii, H. Yoshimura, H. Oyamatsu
Toshiba Corporation, Japan

10:20
08-A.2 A Novel Approach to the Statistical Generation of Non-Normal Distributed PSP Compact Model Parameters Using a Nonlinear Power Method
U. Kovac, D. Dideban, B. Cheng, N. Moezi, G. Roy, A. Asenov
University of Glasgow, United Kingdom

Session 08-B: TCAD: Simulation Approaches I

Tuesday, September 7, 2010, 10:00-10:40
Room B
Chair: Phil Oldiges

10:00
08-B.1 A Simple and Efficient Method for the Calculation of Carrier-Carrier Scattering in Monte-Carlo Simulations
W. Lee, U. Ravaioli
University of Illinois at Urbana-Champaign, United States

10:20
08-B.2 Inclusion of the Pauli Principle in a Deterministic Boltzmann Equation Solver for Semiconductor Devices
S. Hong, C. Jungemann
Bundeswehr University, Germany

Session 09-A: Variability: CMOS & Memories

Tuesday, September 7, 2010, 11:20-12:40
Room A
Chair: Asen Asenov

11:20
09-A.1 **Compact Process and Layout Aware Model for Variability Optimization of Circuit in Nanoscale CMOS**
Y. Kim, J. Jeon, Y. Jang, Y. Park, G. Yang, Y. Park, M. Yoo, C. Chung
Samsung Electronics, Korea, South

11:40
09-A.2 **Halo Profile Engineering to Reduce Vt Fluctuation in High-K/Metal-Gate nMOSFETs**
W. Chen[1], T. Yu[1], T. Ohtou[1], Y. Sheu[1], J. Wu[1], C. Liu[2]
[1]TSMC, Taiwan; [2]National Taiwan University, Taiwan

12:00
09-A.3 **Lithography Induced Layout Variations in 6-T SRAM Cells**
C. Kampen, P. Evanschitzky, A. Burenkov, J. Lorenz
Fraunhofer IISB, Germany

12:20
09-A.4 **Statistical Simulation of Metal-Gate Work-Function Fluctuation in High-K/Metal-Gate CMOS Devices**
C. Yu, M. Han, H. Cheng, Z. Su, Y. Li, H. Watanabe
National Chiao Tung University, Taiwan

Session 09-B: TCAD: Simulation Approaches II

Tuesday, September 7, 2010, 11:20-12:40
Room B
Chair: Shinichi Takagi

11:20
09-B.1 **System Matrix Compression for Spherical Harmonics Expansions of the Boltzmann Transport Equation**
K. Rupp, T. Grasser, A. Jüngel
TU Wien, Austria

11:40
09-B.2 **Study of the Wigner Function Boundary Conditions at Different Barrier Heights**
A. Savio, A. Poncet
Lyon Institute of Nanotechnologies, France

12:00
09-B.3 **Spherical Harmonics Expansion of the Conduction Band for Deterministic Simulation of SiGe HBTs with Full Band Effects**
G. Matz, S. Hong, C. Jungemann
Bundeswehr University, Germany

12:20
09-B.4 **A Non-Linear Variational Principle for the Self-Consistent Solution of Poisson's Equation and a Transport Equation in the Local Density Approximation**
H. Carrillo Nuñez[1], W. Magnus[2], F. Peeters[1]
[1]University of Antwerp, Belgium; [2]University of Antwerp/imec-Leuven, Belgium

Session 10-A: Invited

Tuesday, September 7, 2010, 14:00-14:40
Room A
Chair: Massimo Fischetti

14:00
10-A.1 **Quasi-Ballistic Transport in Nano-Scale Devices: Boundary Layer, Potential Fluctuation, and Coulomb Interaction**
N. Sano
University of Tsukuba, Japan

Session 11-A: Variability: SOI & Nanowires

Tuesday, September 7, 2010, 14:40-15:20
Room A
Chair: Massimo Fischetti

14:40
11-A.1 **Variability in Nano-Scale Intrinsic Silicon-on-Thin-Box MOSFETs (SOTB MOSFETs)**
Y. Yang, G. Du, R. Han, X. Liu
Peking University, China

15:00
11-A.2 **Simulation of Line-Edge Roughness Effects in Silicon Nanowire MOSFETs**
T. Yu, R. Wang, R. Huang
Peking University, China

Session 11-B: Process: Ion Implantation

Tuesday, September 7, 2010, 14:40-15:20
Room B
Chair: Juergen Lorenz

14:40
11-B.1 **Proposal of a Point-Source Model for Highly-Accurate Analytical 3D Calculation of Ion Implanted Dopant Profiles**
K. Nishi[1], M. Mochizuki[2], H. Hayashi[2], K. Fukuda[2], I. Kurachi[2]
[1]Kinki Univ Tech College, Japan; [2]Oki semiconductor, Japan

15:00
11-B.2 **Compact Process Model of Temperature Dependent Amorphization Induced by Ion Implantation**
A. Schmidt, I. Jang, T. Kim, K. Lee, Y. Park, M. Yoo, C. Chung
Samsung Electronics, Korea, South

Session 12-A: Nanowires: RF & Strain

Tuesday, September 7, 2010, 15:40-16:20
Room A
Chair: Massimo Rudan

15:40
12-A.1 **Modeling of NQS Effects in Carbon Nanotube Transistors**
M. Claus, S. Mothes, M. Schröter
Technische Universität Dresden, Germany

16:00
12-A.2 **Strain Effects on Hole Current in Silicon Nanowire FETs**
H. Minari[1], T. Kitayama[2], M. Yamamoto[2], N. Mori[1]
[1]CREST, Japan; [2]Osaka University, Japan

Session 12-B: Process: Interfaces & Electromigration

Tuesday, September 7, 2010, 15:40-16:20
Room B
Chair: Valery Axelrad

15:40
12-B.1 **Improvement of the Interface Integrity Between a High-K Dielectric Film and a Metal Gate Electrode by Controlling Point Defects and Residual Stress**
K. Suzuki, T. Inoue, H. Miura
Tohoku University, Japan

16:00
12-B.2 **Impact of Parameter Variability on Electromigration Lifetime Distribution**
H. Ceric, R. Lacerda de Orio, S. Selberherr
TU Wien, Austria

19:50 **Gala dinner**

Session 13-A: Invited

Wednesday, September 8, 2010, 09:00-09:40
Room A
Chair: Bernd Meinerzhagen

9:00
13-A.1 Future High Density Memories for Computing Applications: Device Behavior and Modeling Challenges
G. Spadini, I. Karpov, D. Kencke
Intel Corporation, United States

Session 14-A: Memories I

Wednesday, September 8, 2010, 09:40-10:40
Room A
Chair: Bernd Meinerzhagen

09:40
14-A.1 A Novel Algorithm for the Solution of Charge Transport Equations in MANOS Devices Including Charge Trapping in Alumina and Temperature Effects
A. Padovani, L. Larcher
Università di Modena e Reggio Emilia, Italy

10:00
14-A.2 Investigation of Charge Loss Mechanisms in Planar and Raised STI Charge Trapping Flash Memories
Z. Xia, D. Kim, J. Lee, K. Lee, Y. Park, M. Yoo, C. Chung
Samsung Electronics, Korea, South

10:20
14-A.3 Stochastic Modeling Hysteresis and Resistive Switching in Bipolar Oxide-Based Memory
A. Makarov, V. Sverdlov, S. Selberherr
TU Wien, Austria

Session 14-B: Compact Modeling

Wednesday, September 8, 2010, 09:40-10:40
Room B
Chair: Susanna Reggiani

09:40
14-B.1 Modeling of 2D Bias Control in Overlap Region of High-Voltage MOSFETs for Accurate Device/Circuit Performance Prediction
A. Tanaka[1], Y. Oritsuki[1], H. Kikuchihara[1], M. Miyake[1], H. Mattausch[1], M. Miura-Mattausch[1], Y. Liu[2], K. Green[2]
[1]Hiroshima University, Japan; [2]TI, United States

10:00
14-B.2 **Compact Modeling of Fe-FET and Implications on Variation-Insensitive Design**
C. Wang, Y. Ye, Y. Cao
Arizona State University, United States

10:20
14-B.3 **Proposal of a Fitting Accuracy Metric Suitable for Compact Model Qualification in All MOSFET Operation Regions**
H. Sakamoto, T. Iizuka
Renesas Electronics, Japan

Session 15-A: Memories II

Wednesday, September 8, 2010, 11:20-12:40
Room A
Chair: Kaustav Banerjee

11:20
15-A.1 **Modeling of the Voltage Snap-Back in Amorphous-GST Memory Devices**
M. Rudan[1], F. Giovanardi[1], T. Tsafack[1], F. Xiong[2], E. Piccinini[1], F. Buscemi[1], A. Liao[2], E. Pop[2], R. Brunetti[3], C. Jacoboni[3]
[1]University of Bologna, Italy; [2]University of Illinois at Urbana-Champaign, United States; [3]University of Modena and Reggio Emilia, Italy

11:40
15-A.2 **Detailed Physical Simulation of Program Disturb Mechanisms in Sub-50 nm NAND Flash Memory Strings**
C. Nguyen[1], A. Kuligk[1], M. Vexler[1], M. Klawitter[1], V. Beyer[2], T. Melde[3], M. Czernohorsky[2], B. Meinerzhagen[1]
[1]TU Braunschweig, Germany; [2]CNT, Germany; [3]NaMLab gGmbH, Germany

12:00
15-A.3 **Multiphysics Modeling of PCM Devices for Scaling Investigation**
G. Ferrari[1], A. Ghetti[2], D. Ielmini[1], A. Redaelli[2], A. Pirovano[2]
[1]Politecnico di Milano, Italy; [2]Numonyx, Italy

12:20
15-A.4 **FinFET SRAM Cell Optimization Considering Temporal Variability Due to NBTI/PBTI and Surface Orientation**
V. Hu, M. Fan, C. Hsieh, P. Su, C. Chuang
National Chiao Tung University, Taiwan

Session 15-B: TCAD: Transport Models

Wednesday, September 8, 2010, 11:20-12:40
Room B
Chair: Axel Erlebach

11:20
15-B.1 **Symmetry Reduction by Surface Scattering and Mobility Model for Stressed <100>/(001) MOSFETs**
F. Bufler, A. Erlebach, M. Oulmane
Synopsys Schweiz GmbH, Switzerland

11:40
15-B.2 **Analytical Models of Effective DOS, Saturation Velocity and High-Field Mobility for SiGe HBTs Numerical Simulation**
G. Sasso[1], G. Matz[2], C. Jungemann[2], N. Rinaldi[1]
[1]University of Naples - Federico II, Italy; [2]Bundeswehr University, Germany

12:00
15-B.3 **TCAD Simulation Vs. Experimental Results in FDSOI Technology: from Advanced Mobility Modeling to 6T-SRAM Cell Characteristics Prediction**
M. Jaud[1], P. Scheiblin[1], S. Martinie[2], M. Cassé[1], O. Rozeau[1], J. Dura[1], J. Mazurier[1], A. Toffoli[1], O. Thomas[1], F. Andrieu[1], O. Weber[1]
[1]CEA-LETI, MINATEC, France; [2]IM2NP-CNRS, France

12:20
15-B.4 **Improved Impact-Ionization Modelling and Validation with pn-Junction Diodes**
Z. Pan[1], S. Holland[1], D. Schroeder[2], W. Krautschneider[2]
[1]NXP Semiconductors, Germany; [2]Hamburg University of Technology, Germany

Session 16-A: Invited

Wednesday, September 8, 2010, 14:00-14:40
Room A
Chair: Andreas Schenk

14:00
16-A.1 **Solving Boltzmann Transport Equation Without Monte-Carlo Algorithms - New Methods for Industrial TCAD Applications**
B. Meinerzhagen[1], A. Pham[1], S. Hong[2], C. Jungemann[2]
[1]TU Braunschweig, Germany; [2]Bundeswehr University, Germany

Session 17-A: Numerics for Device Simulation

Wednesday, September 8, 2010, 14:40-15:40
Room A
Chair: Andreas Schenk

14:40
17-A.1 **Pseudo-Spectral Method for the Modelling of Quantization Effects in Nanoscale MOS Transistors**
A. Paussa, F. Conzatti, D. Breda, R. Vermiglio, D. Esseni
Università degli studi di Udine, Italy

15:00
17-A.2 **Stable Implementation of a Deterministic Multi-Subband Boltzmann Solver for Silicon Double-Gate nMOSFETs**
K. Zhao[1], S. Hong[2], C. Jungemann[2], R. Han[1]
[1]Peking University, China; [2]Bundeswehr University, Germany

15:20
17-A.3 **Improving the Accuracy of the Schroedinger-Poisson Solution in CNWs and CNTs**
M. Rudan, A. Gnudi, E. Gnani, S. Reggiani, G. Baccarani
University of Bologna, Italy

Session 17-B: Sensors and MEMS

Wednesday, September 8, 2010, 14:40-15:40
Room B
Chair: Mitiko Miura-Mattausch

14:40
17-B.1 **Fast DNA Sequencing via Transverse Differential Conductance**
Y. He[1], R. Scheicher[2], A. Grigoriev[2], R. Ahuja[2], S. Long[1], Z. Ji[1], Z. Yu[1], M. Liu[1]
[1]Chinese Academy of Sciences, China; [2]Uppsala University, Sweden

15:00
17-B.2 **Modeling and Fast Simulation of RF-MEMS Switches Within Standard IC Design Frameworks**
M. Niessner[1], G. Schrag[1], J. Iannacci[2], G. Wachutka[1]
[1]Munich University of Technology, Germany; [2]Fondazione Bruno Kessler, Italy

15:20
17-B.3 **Giant Piezoresistance Effect in P-Type Silicon**
T. Nghiêm, V. Aubry-Fortuna, C. Chassat, A. Bossebeuf, P. Dollfus
Université Paris Sud, France

WORKSHOP 1

Simulation and Characterization of Statistical CMOS Variability and Reliability

Organized by: A. Asenov (Glasgow University), S. Nassif (IBM), and G. Baccarani (University of Bologna).

08.30 Introduction: Impact of statistical variability and reliability on circuit design
S. Nassif (IBM)

09.00 TCAD simulation of statistical variability
09:00 A. Brown (Glasgow University, UK)
09:25 V. Moroz (Synopsys, USA)
09:50 S. Toriyama (Toshiba, Japan)

10.15 Coffee break

10.45 Measurements and characterization of statistical variability
10:45 C. Spanos (University of California at Berkeley, USA)
11:10 G. Ghibaudo (IMEP/MINATEC, France)
11:35 T. Hiramoto (Tokyo University, Japan)

12.00 Buffet lunch and interactive presentations from TCAD vendors.

13.30 Reliability impact and scaling trends.
13:30 K. Cao (Arizona State University, USA)
13:55 K. Takeuchi (Renesas Electronics, Japan)
14:20 T. Grasser (TU Vienna)

14.45 Coffee break

15.00 Statistical compact model strategies and statistical circuit simulation.
15:00 M. Miura-Mattausch (Hiroshima University, Japan)
15:25 J. Victory (Sentinel, USA)
15:50 A. Juge (ST Microelectronics, France)

16.15 Closing address
Interaction between TCAD, compact models and circuit simulation to support statistical and robust design. A. Asenov, (University of Glasgow, UK)

16.45 Close

WORKSHOP 2

Simulation and Characterization of Steep-Slope Switches (SSS)

Organized by: A. M. Ionescu (Ecole Polytechnique Fédérale de Lausanne) and G. Baccarani (University of Bologna).

08.30 Introduction: Welcome and general information on FP7 STEEPER initiative in Europe
Adrian M. Ionescu (EPFL)

08.50 Tunnel FETs: Fabrication and Characterization
Tejas Krishnamohan (Intel Corp & Stanford Univ.)

09:30 Tunnel FETs: impact of the fabrication process on the electrical performances
Cyrille Le Royer (CEA LETI – MINATEC)

09:50 Planar and Nanowire Si-TFETs
Qing-Tai Zhao, Siegfried Mantl (Institute of Bio- and Nanosystems, Forschungszentrum – Juelich)

10.15 Coffee break

10.40 Novel concepts for steep slope switches
Sayeef Salahuddin (Univ. of California at Berkeley)

11:20 Sub-60mv/decade switching in junction-less transistors
Nima Dehdashti Akhavan, Jean-Pierre Colinge (Tyndall National Institute)

11:40 Steep-slope nanowire FETs: from concept to design
Elena Gnani, Giorgio Baccarani (Univ. of Bologna)

12.00 Buffet Lunch

13.30 Atomistic Simulations of TFETs: from Coherent to Phonon-Assisted Tunneling
Mathieu Luisier (Purdue University)

14:10 Simulation challenges in tunnel FETs
Luca Selmi (University of Udine)

14.30 Modeling negative capacitance field effect transistor
David Jiménez (Universitat Autònoma de Barcelona, Spain)

14.50 Coffee break

15.10 Nanowire tunnel FETs in silicon and III-V systems
H. Riel (IBM Research GmbH, Zurich Research Laboratory)

15:50 III-V heterojunction tunnel FETs
Joachim Knoch (TU Dortmund).

16:10 Abrupt hybrid switches using internally combined band-to-band and barrier tunneling mechanisms
Livio Lattanzio (EPFL).

16:30 Role of the transport in the channel for I_{ON} optimization in Tunnel FETs
David Esseni (Univ. Udine)

16.50 Close