Statistical Compact Model Strategies, and Statistical Circuit Simulation

SISPAD Variability Workshop on "*Simulation and Characterization of Statistical CMOS Variability and Reliability*"

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Presenter: André Juge

Acknowledgments

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- *Modern project team*: A.Asenov and University of Glasgow Device modeling group, G.Ghibaudo (IMEP), Jan van Gerwen (NXP)

- *Reality project team*: M.Miranda (IMEC)

- *European Union*: support through REALITY FP7-2008-IST-1-216537 and ENIAC Modern projects

Outline

- <u>Variations and Impact</u>

- Statistical Compact Models

- Statistical Circuit Simulation

- European project: Modern

- Conclusion

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Variability components at circuit scale

		Process	Environment	Temporal
Global		$<L_g>$ and $<W>$ <layer thicknesses> $<R>$'s <doping> $<V_{body}>$	T environment range V_{dd} range	$<NBTI>$ Hot electron shifts
Local	**Systematic**	OPC Phase shift Layout mediated strain Well proximity	Self-heating IR drops	Distribution of NBTI Voltage noise SOI V_{body} history Oxide breakdown history
	Statistical	**Random dopants Line Edge Roughness Poly Si granularity Interface roughness High-k morphology**		
Across-chip		Line width due to pattern density effects	Thermal hot spots due to non-uniform power dissipation	Computational load dependent hot spots

Classification from University of Glasgow (2009)

❑ SPICE models are built to reflect impact of Process, Voltage, Temperature variations and Temporal shift of individual components during circuit operation
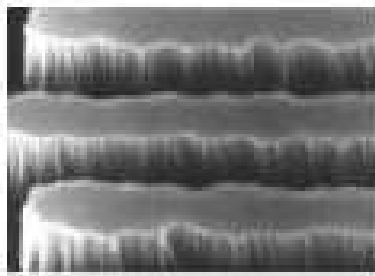
❑ Chip level methodologies need to be developped concurently (beyond transistor level SPICE models) to allow manufacturing of high yield and reliable products
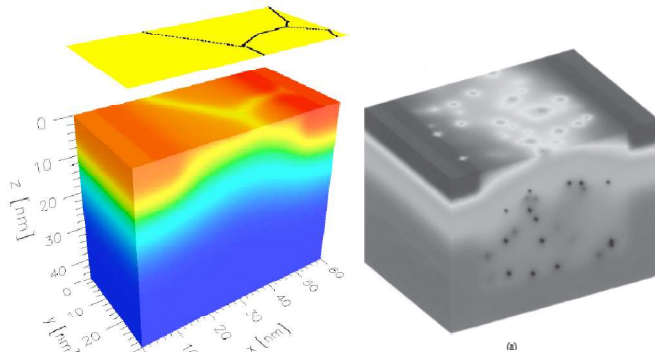
Variations in statistical models: examples of sources

Local Statistical
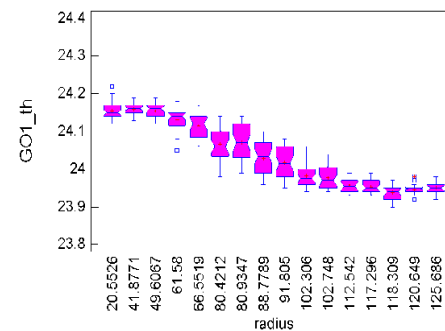
Line edge roughness
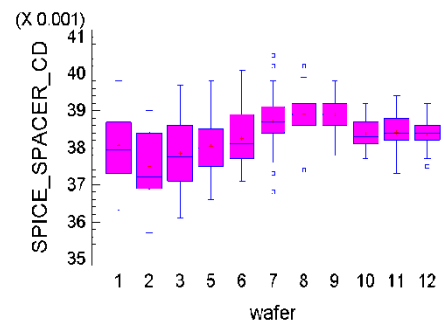

Poly Si granularity

Channel dopants

Source: A.Asenov
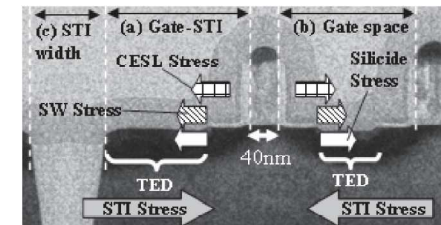
Global Process

Die to die

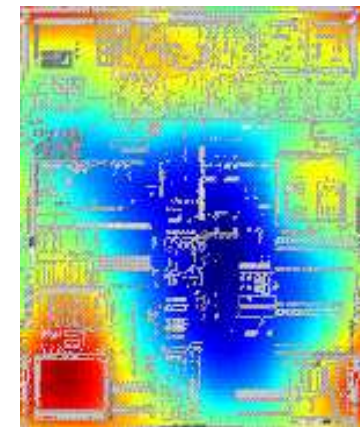**Wafer to wafer**

Local Systematic
(Layout dependent)

H.Tsuno, Sony, VLSI 2007

Across chip

Variations impact: transistor

W ref transistor
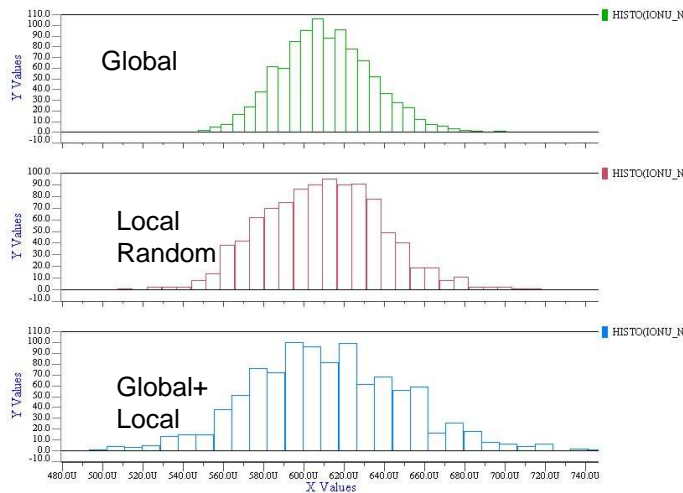
σ	Idsat Wref	Idsat Wmin
Global	1	1.1
Local	1	2
All	1.4	2.2

W min transistor
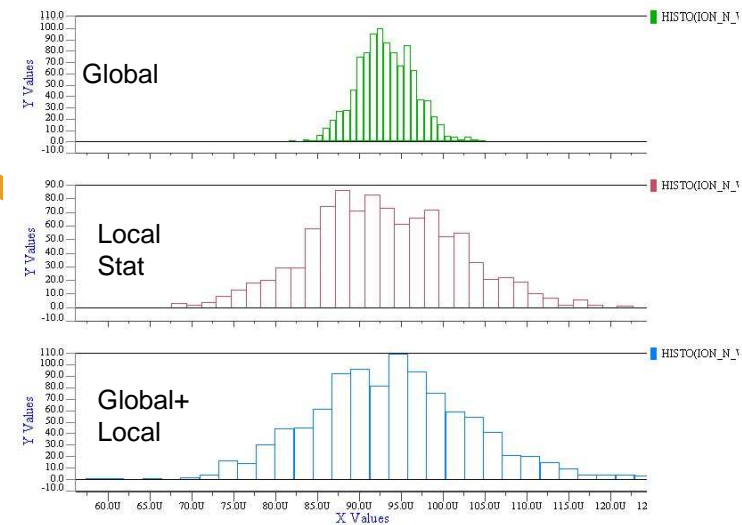
❑Impact:
- ➢ Wref Local ~ Global
- ➢ Wmin: Local random ~ 2 x Global
- ➢ Local vs Global strongly geometry dependent

❑Characterization challenge:
- ➢Design of sensitive Test structures
- ➢De-embedding Local/Global Systematic/Random variations

Variations impact: RO example
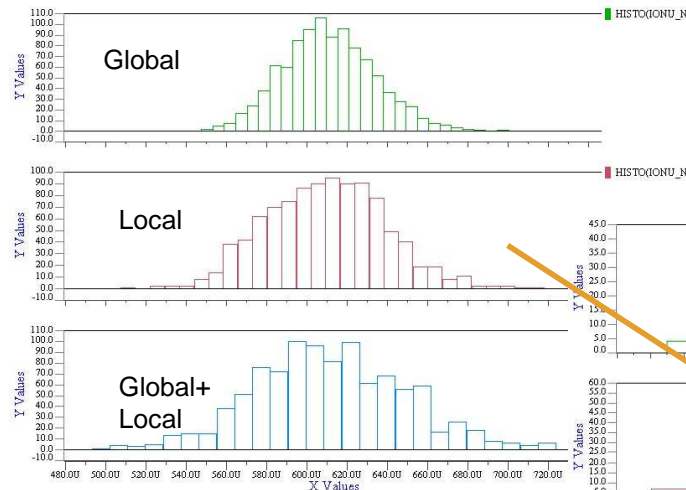
W ref tdsat

Inverter ring: Trise

Inverter ring: Period

σ	Idsat	Trise	Period
Global	1	1	1
Local	1	1	0.16
All	1.4	1.4	1.02
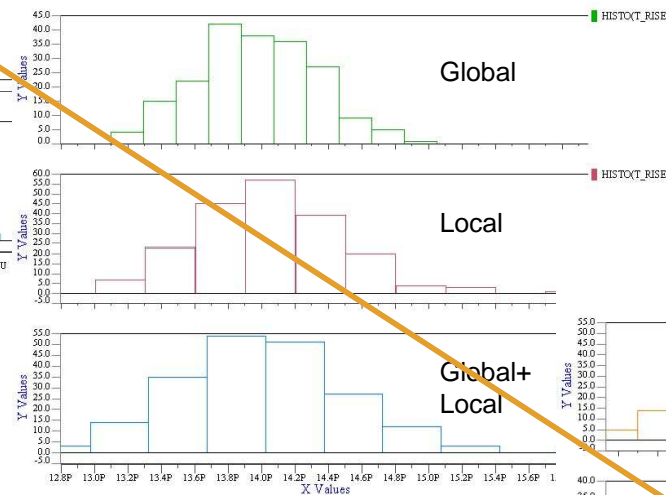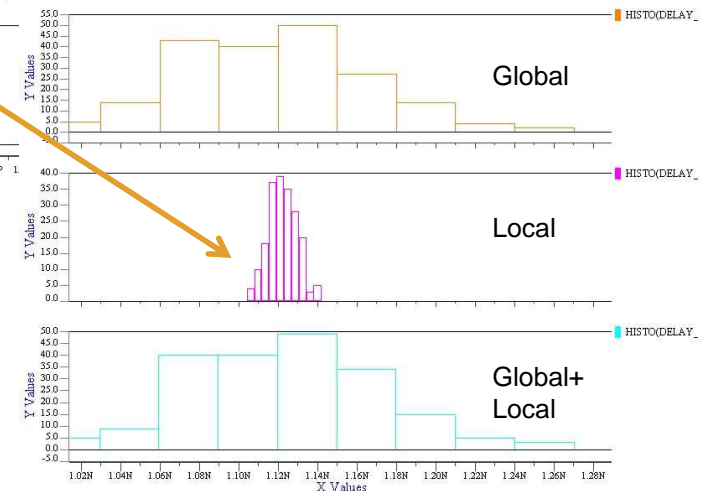
❑ Variations impact :
  ➢ Transistor: Local ~ Global
  ➢ Inverter Rise time : Local ~ Global
  ➢ Inverter Period: Local << Global

❑ Circuit design needs:
  ➢ Accurate compact statistical models
  ➢ Accurate/efficient simulation methods

Outline

- Variations and Impact

- <u>Statistical Compact Models</u>
    - Goal
    - Accuracy components
    - Extraction methods: PCA, NPM (SISPAD 2010) , BPV
    - Corner models vs Statistical models
    - Implementation: within compact model structure / within circuit netlist

- Statistical Circuit Simulation

- European project: Modern

- Conclusion

Statistical models for circuit simulation : goal
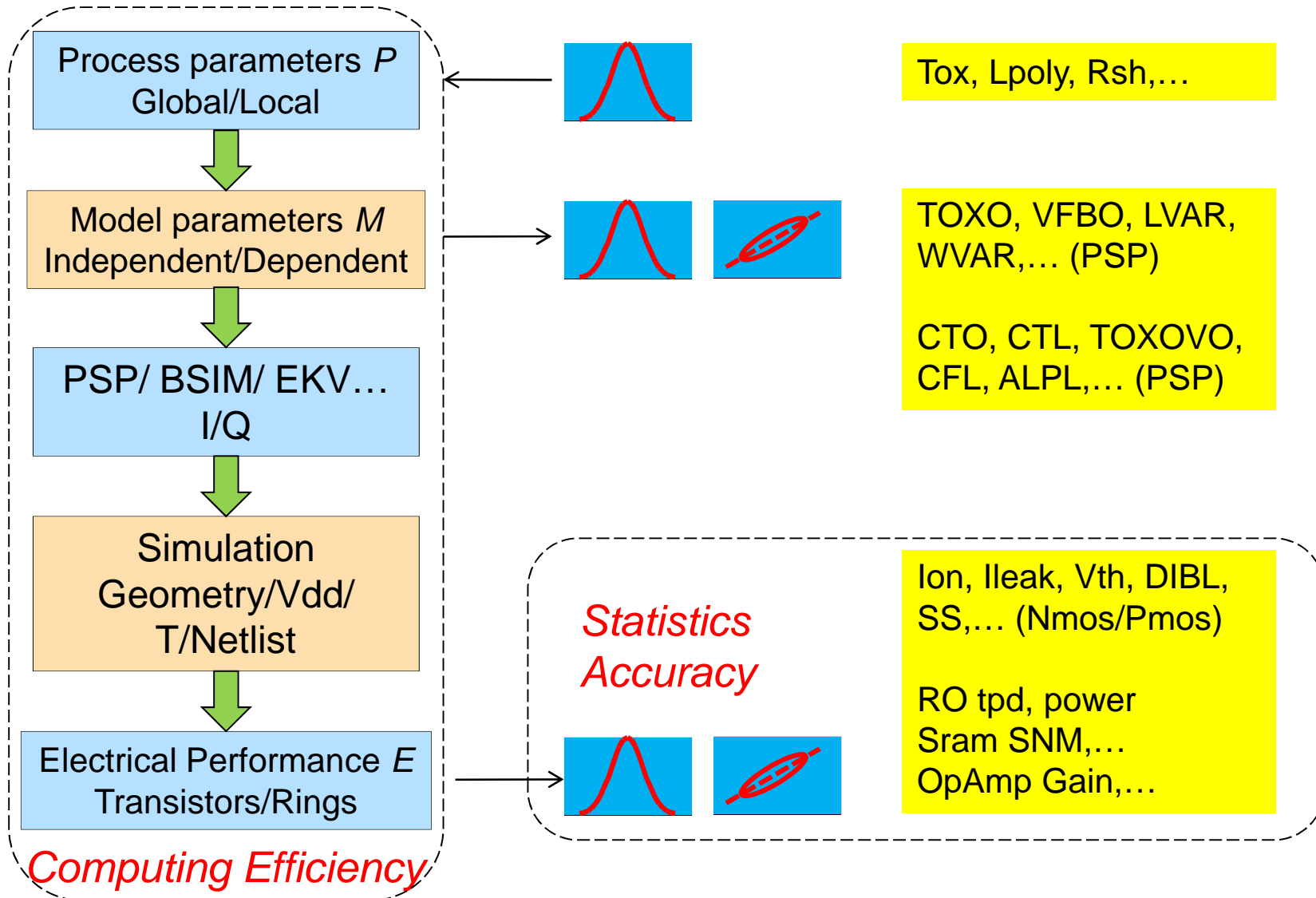
Principal Component Analysis Method (PCA)
statistical model extraction from electrical performance

Process parameters *P*
Global/Local

PCA

Model parameters *M*
Independent/Dependent

BSIM/ PSP/ EKV…
I/Q

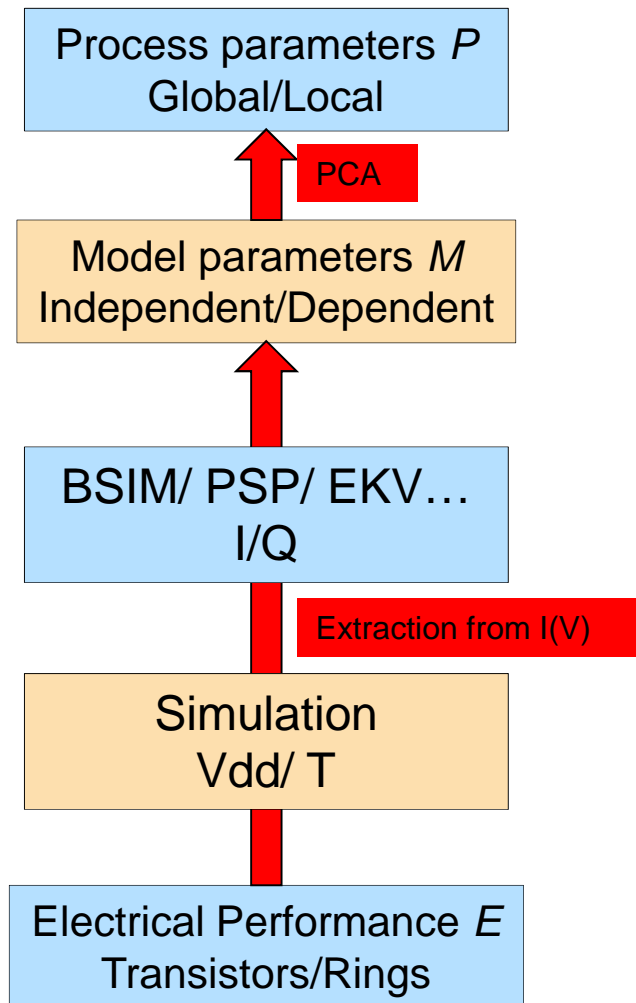**Extraction from I(V)**
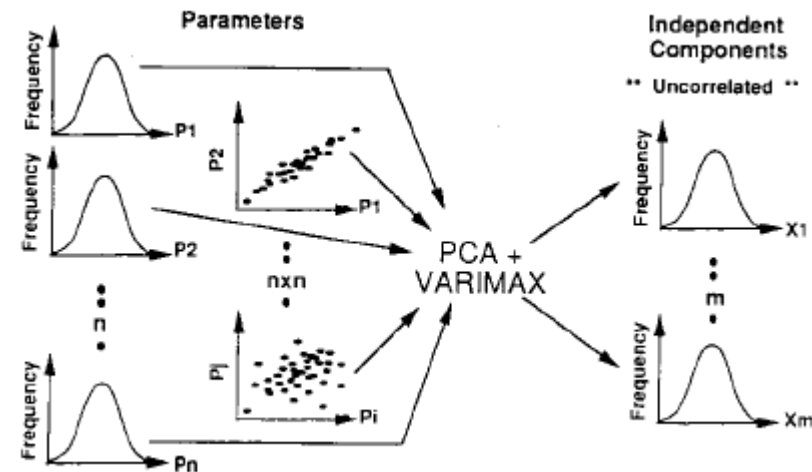
Simulation
Vdd/ T

Electrical Performance *E*
Transistors/Rings

❑*M* sets extracted from full I(V) sets

❑A correlated set of model parameters *M* (Vth, KB,..) is reduced to a limited set of *X* independent random normal dimensionless factors.

❑Careful implementation allows *X* to be related to *P* *(statistical independent)*
Mi = ai1.X1 + ai2.X2 + ...

JA.Power, ICMTS 1993

Nonlinear Power Method (NPM, SISPAD 2010)
statistical model extraction from electrical performance

Process parameters P
Global/Local

NPM

Model parameters M
Independent/Dependent

BSIM/ PSP/ EKV…
I/Q

Extraction from I(V)

Simulation
Vdd/ T

Electrical Performance E
Transistors/Rings
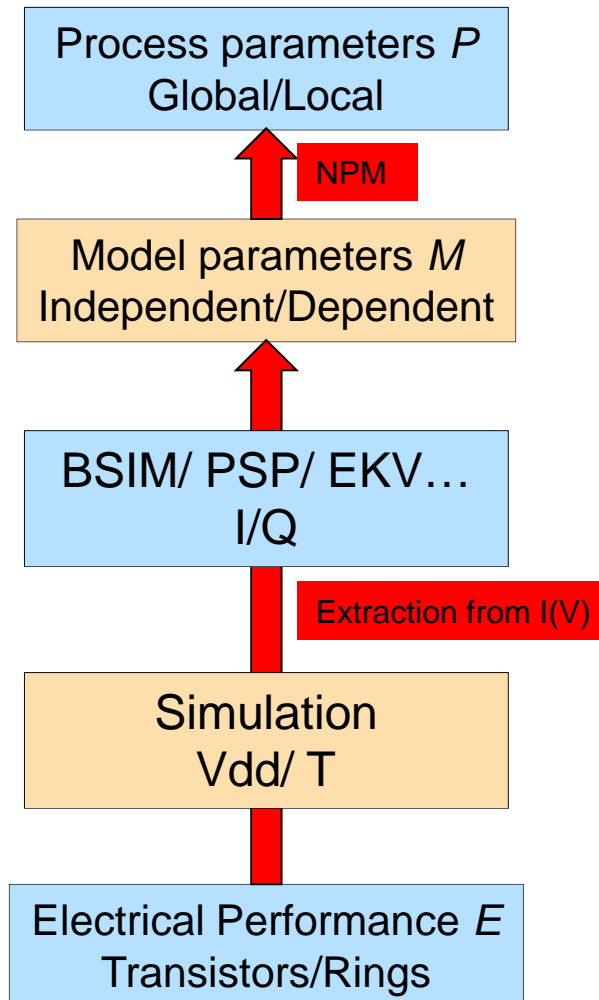
❑ M sets are directly extracted from full I(V) sets

❑ 4 moments of each M parameters and correlations between them are preserved

❑ Significant improvements for M and E distributions (shape and tails) demonstrated
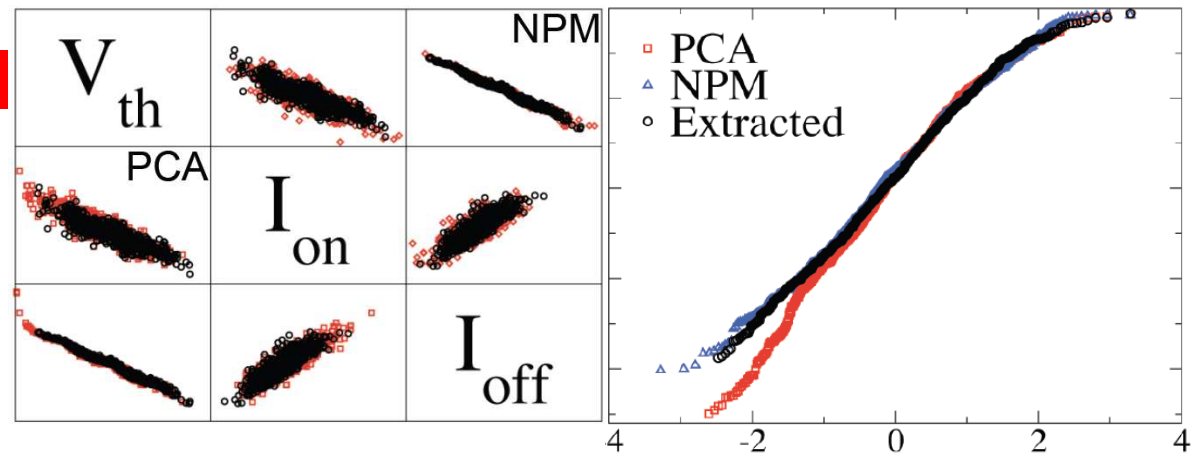
U.Kovac, SISPAD 2010, correlations between Transistor FOM (left),
RO delay QQ plot (right)

Backward Propagation of Variance(BPV)
statistical model extraction from electrical performance

Process parameters P
Global/Local

Model parameters
(M, including P)
Independent/Dependent

BSIM/ PSP/ EKV…
I/Q

M moments computation

Simulation
Vdd/ T
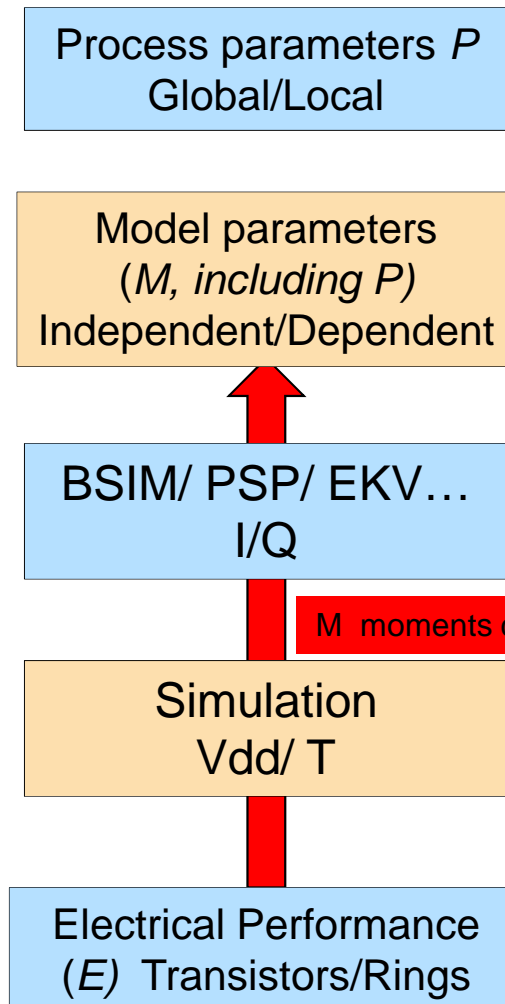
Electrical Performance
(E) Transistors/Rings

❑A subset P of independent process related model parameters selected from M.

❑ $\sigma^2_{P_i}$ computed from $\sigma^2_{E_i}$. Inter-device correlations between E_i considered

$$\sigma^2_E \cong \sum_{i=1}^{Np}\left(\frac{\partial E}{\partial P_i}\right)\times\sigma^2_{P_i}$$
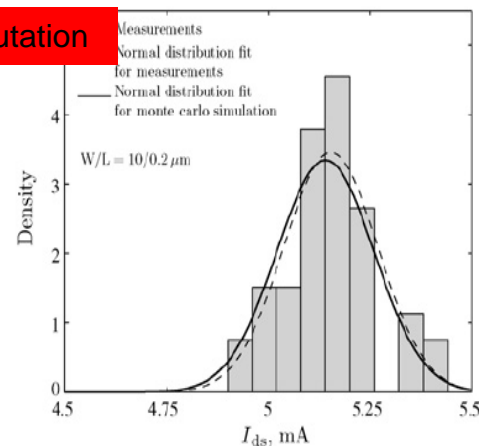
X.Li &al, IEEECAD, 2010

Stevanovic &al, SSE, 2010

Implementation aspects: comparison from paper work

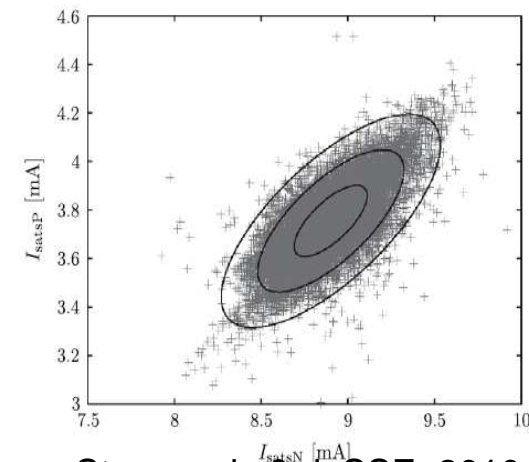|	Features	FPV	PCA	NPM (SISPAD 2010)	BPV
E test	Samples	200-1000	200-1000	200-1000	200-1000
	Type	Cg, Cj	Full I(V)	Full I(V)	ET param
Model statistics	M extraction	All samples	All samples	All samples	Nominal
	Moments	1,2	1,2	1, 2, 3, 4	1, 2,3 (2010)
	Correlations	✓	✓	✓	✓
E perf simulated accuracy	Moments	1,2	1,2	1, 2, 3, 4	1, 2, 3
	Correlations	✓	✓	✓	✓ (2010)

❑ Silicon test time remains limiting factor, except for BPV
❑ BPV : for mature technologies (as reported, down to 0.18um)

Statistical model: Common practice

- Circuit Design development often preceeds technology maturity, therefore Variability estimates need to be performed.

- Intradie variations: relies on advanced TCAD calibrated on previous node for local random effects, and OCV experiments on Silicon

- Interdie variations: TCAD/ Si DOEs help => Main factors, Sensitivities

- Electrical Characterization effort is key to progress, and focused on ET data (Transistor and RO figures) for all variability sources

- Physics based Compact model extensions are applied timely when needed (e.g. observation of unexpected L scaling for pocket implant Mosfet AVT figure, see presentation from G.Ghibaudo)

- Impact analysis of *electrical performance* simulated and comparison with measurements (QA approach)

Corners models vs Statistical models

- Principle: simulate circuit tolerance with combinations of pre-defined +/- nσ deviations of model independent parameters to minimize computational effort

- Example (PSP inputs, Speed criteria):

M	SS	SF	TT	FS	FF
dLvar	+nσ	0	0	0	-nσ
dWvar	-nσ	0	0	0	+nσ
dtox	+nσ	0	0	0	-nσ
dnsub_n	+nσ	+nσ	0	-nσ	-nσ
dnsub_p	+n	-nσ	0	+nσ	-nσ
dphibl_n	+nσ	+nσ	0	-nσ	-nσ
dphibl_p	+nσ	-nσ	0	+nσ	-nσ
dmu_n	0	-nσ	0	+nσ	0
dmu_p	0	+nσ	0	-nσ	0

- Method *simple* and *computationally* efficient, but …
- Performance specific (Ion deviation, Speed, N/P ratio,…)
- Applies under given operating conditions (Vdd, T, Layout)
- Suited to Global variations (Local deviations expected to average to 0 at circuit scale)
- Correlation between N and P model parameters difficult to handle ('0' or '1')
- Therefore requires validation against Statistical simulation

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Corner Models limitation: Inverter RO example

Ion

tpd
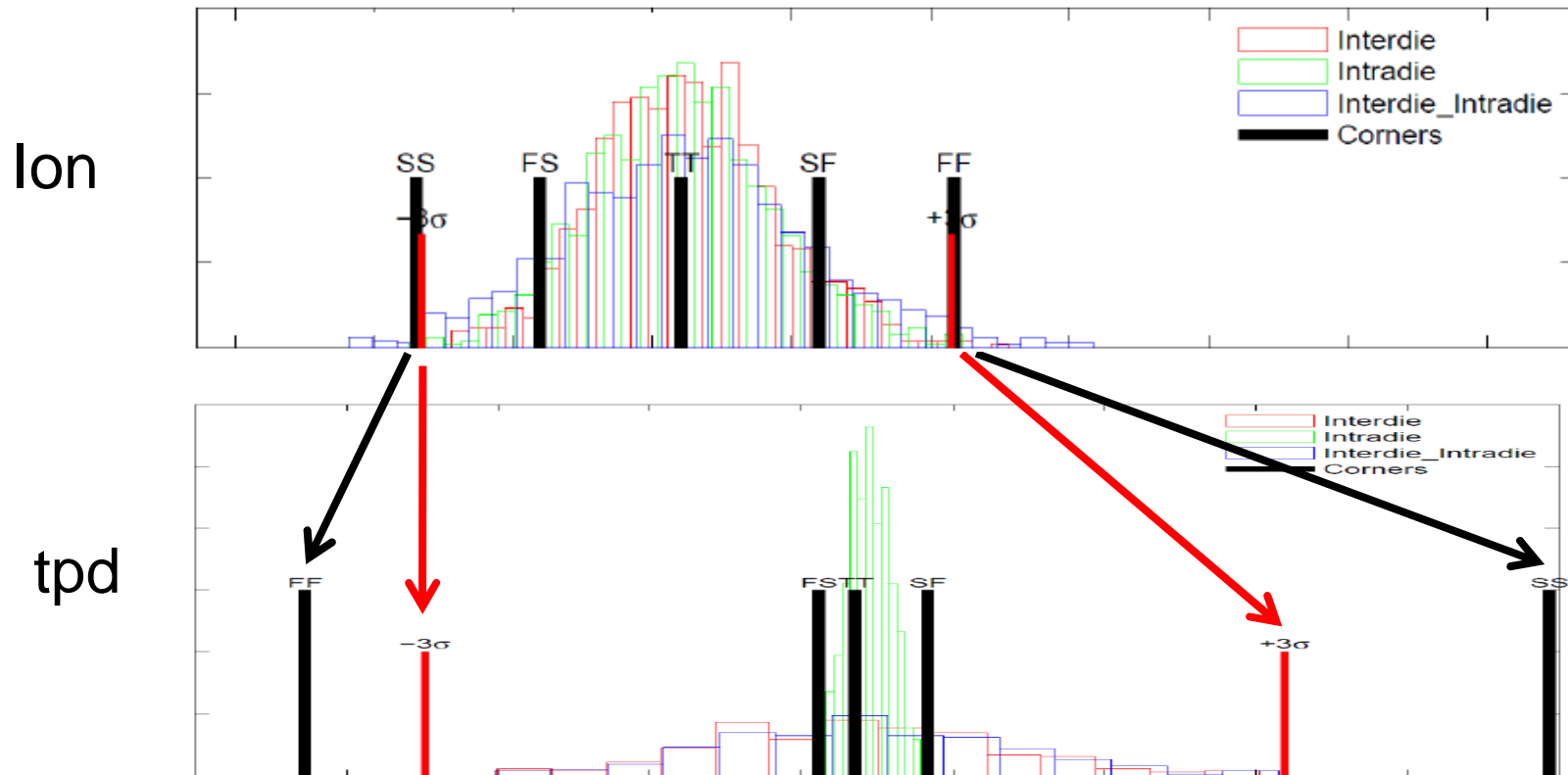
❑ Corners with 2σ model inputs, ΔIon ~ +/- 3σ, Δtpd > +/- 3σ
❑ *Ion* corners overestimate of Δtpd (N/P Ion correlation overestimated)

Corner Models limitation: Op. Amp.example
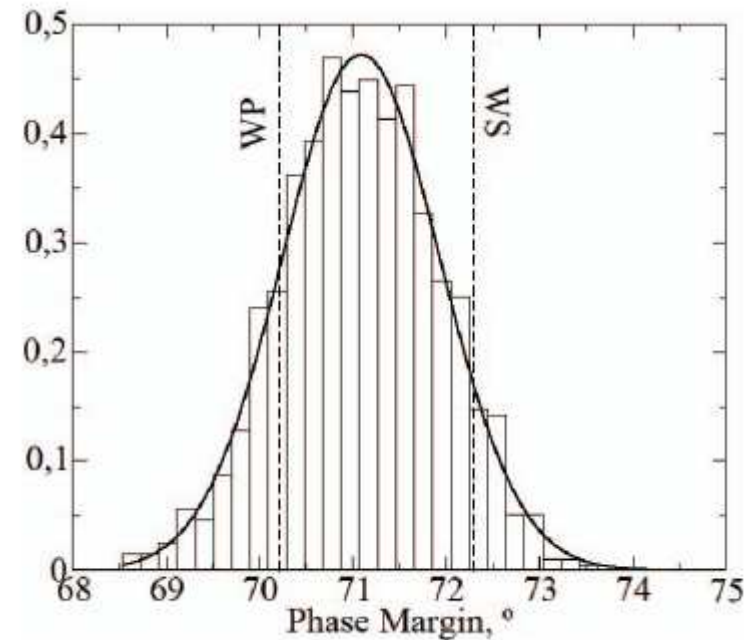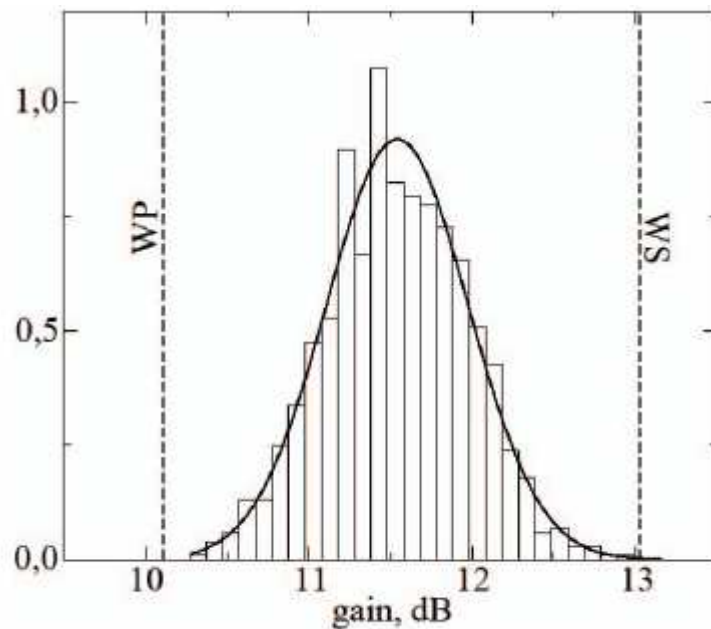
Source: M.Yakupov, MEXDES 2010

❑Worst Power (WP) Worst Speed(WS) Corners
❑Underestimation of Phase Margin variation by Corners on Gain

Corner models:

- Approach 1: Pre-defined Performance specific corners
  - *Performance aware* corners: (CH.Lin, IEEE TED, April 2009)
    - Ion, Ioff, …
    - Logic: Speed, Power
    - Analog: Voltage gain,…
    - SRAM: SNM,…
  - *Arbitrary range*: +/-nσ range (not only +/-3σ)
  - MC simulation mandatory for Pre-defined Corner model validation; can be done on a limited but representative set of circuit configurations

- Approach 2 (Analog)
  - Step 1: Generate RSM Polynomial models of Performance figures (DOE)
  - Step 2 MC simulation, then Corner analysis from MC simulated distributions

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    - Accuracy components
    - Extraction methods: PCA, NPM (SISPAD 2010) , BPV
    - Corner models vs Statistical models
    - *Implementation: within compact model structure / within circuit netlist*

- Statistical Circuit Simulation

- European project: Modern

- Challenges/ Conclusion

Statistical Model implementation: within core model

VARIABILITY INJECTORS: CONCEPT

Variability is modeled at circuit level using a compact model card independent

Original (nominal) device   Transformed (variable) device
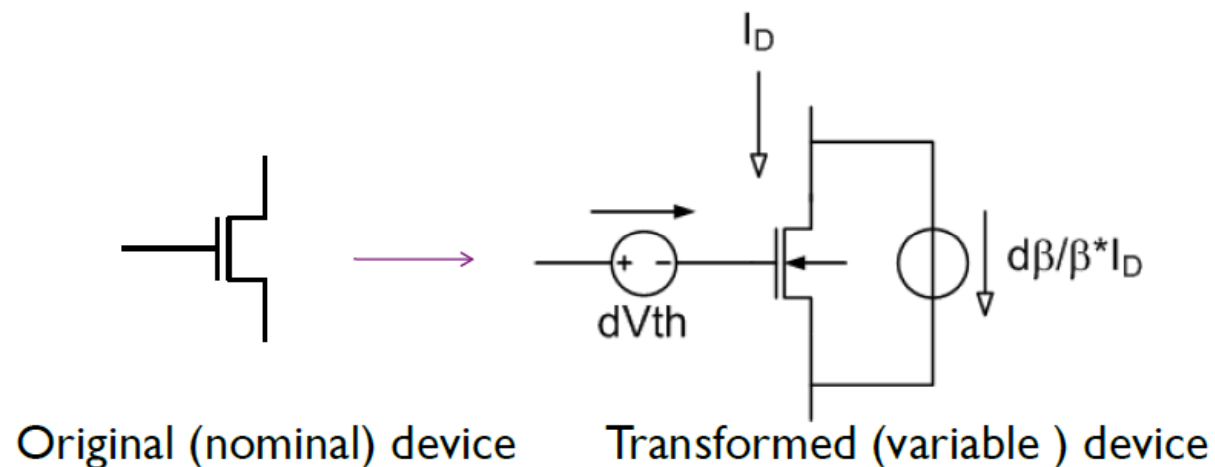
The two sources "fit" the nominal Id-Vgs curve to the variable Ids-Vgs curve (see next slide)

Courtesy of M.Miranda (IMEC, 2010). Patents pending
European Union support through REALITY FP7-2008-IST-1-216537

MODELING VARIABILITY IN A COMPACT MODEL CARD INDEPENDENT FASHION

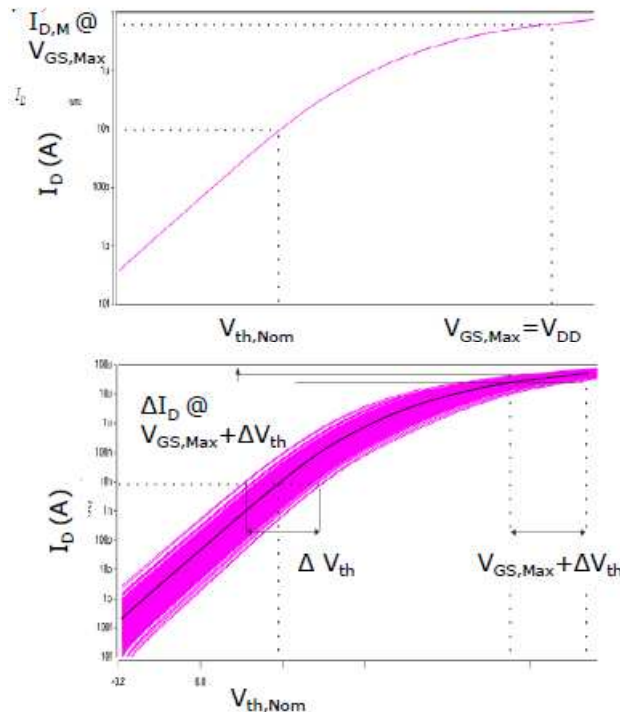Given a sample of $I_D(V_{GS})$ curves from any source

- – TCAD
- – Measurements
- – Statistical Spice
- – What-if analysis

Extract samples of

- – ΔV_{th} by 'cutting' horizontally along $I_{D,Ref}$
- – $\Delta I_D/I_D = \Delta \beta/\beta$ by 'cutting' vertically along $V_{GS,Max} + \Delta V_{th}$
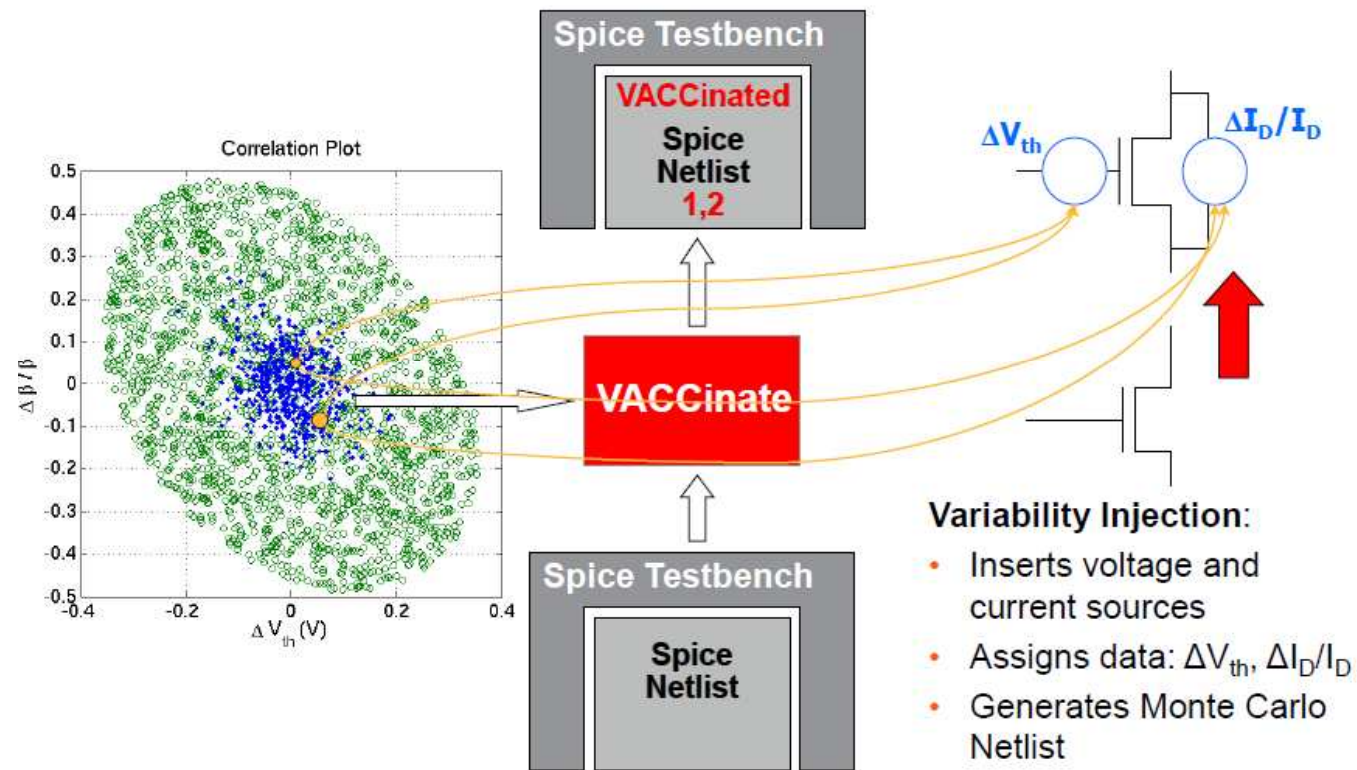
ΔV_{th} and $\Delta \beta/\beta$ samples remain correlated

Same procedure for local and non-local

Courtesy of M.Miranda (IMEC, 2010).

Courtesy of M.Miranda (IMEC, 2010)

BENCHMARKING VARIABILITY INJECTORS AT CIRCUIT LEVEL
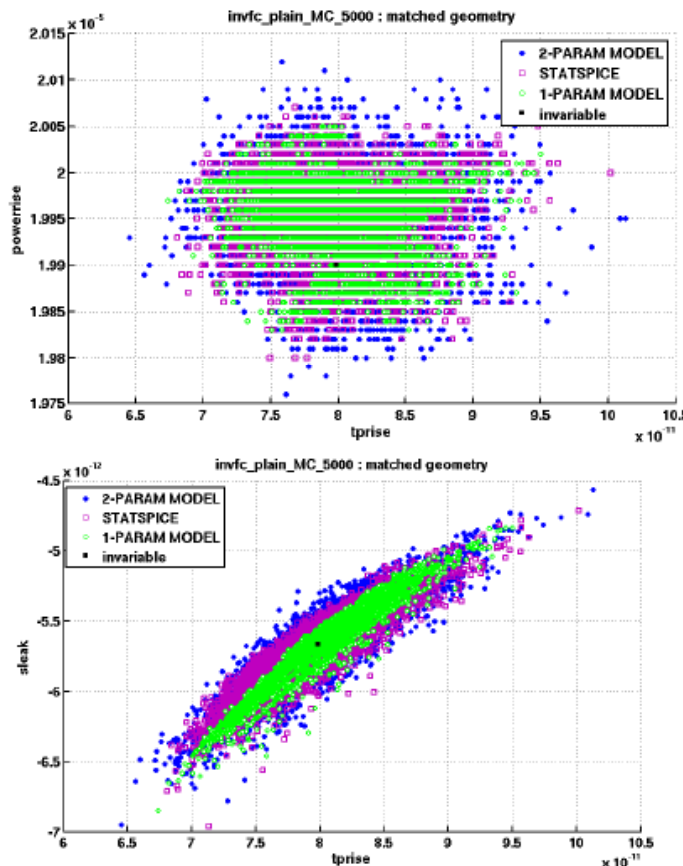
Reference is statistical device foundry model (purple)
Test vehicle is an inverter gate with drive

We benchmark:
  Single source: voltage source model (green)
  Dual source: voltage and current source model (blue)

Conclusions:
  Agreement between the dual-source model with reference
  Single source model underperforms dual-source

In summary:
  Timing can be handled by ΔV_{th} (not fully though)
  Leakage is largely handled by $\Delta\beta/\Delta\beta$
  Dynamic power by the two injectors

Courtesy of M.Miranda (IMEC, 2010)

Outline

- Variations and Impact

- Statistical Compact Models

- *Statistical Circuit Simulation*
    - *Analog DOE*
    - *Timing Analysis: STA, SSTA*

- European project: Modern

- Challenges/ Conclusion

Circuit simulation workload: some numbers

Level		90nm	65nm	45nm
SOC	Chip area (cm2)	1	1	1
	N_Cells	2.0M	5M	10M
	N_Transistors	10M	25M	40M
Critical paths	N_Cells	100-200	100-200	100-200
	N_Transistors	500-1000	500-1000	500-1000
Compact Model	Subckt/Model parameters	280	330	400

❑ Simulation tools:
  ✓ Analog Spice: ~1K transistors
  ✓ Fast Spice: > ~10K
  ✓ Timing Analysis: SOC

❑ Statistical compact models usage is limited by memory and computation cost
  ✓ Analog Spice: direct usage
  ✓ Timing Analysis methods: to assess STA accuracy, to enable SSTA

DOE Analysis Flow

- DOE analysis can be used to study the impact of process variation for analog designs

- Flow overview

Local and/or Global Variations

Polynomial models selection: Linear or quadratic models with/without interactions →

DOE Generation

DOE Execution

Sensitivity Analysis

Performance Specifications

Models Extraction

Yield and Robustness Analysis

Worst-Case Analysis

yes **Goodness of Fit ?** no
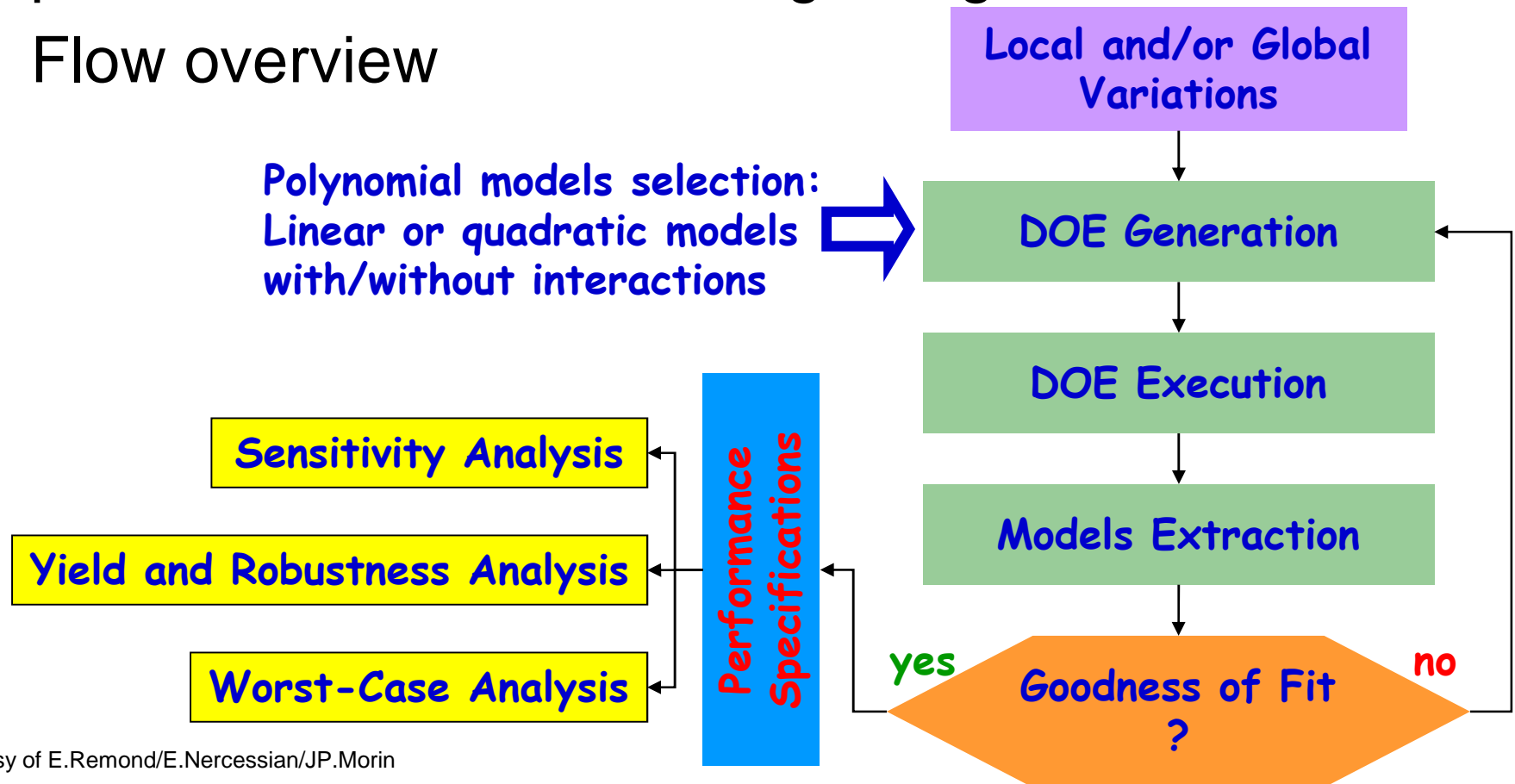
Courtesy of E.Remond/E.Nercessian/JP.Morin

DOE Analysis Flow

- Circuit Performances Analysis based on polynomial expression:

Sensitivity Analysis

- Weight of each process parameter on Performance Y

$$w_i = sign(a_i) \times 100 \times \frac{a_i^2}{\sum_j a_j^2}$$

Ex. : poly_cd (-53.47%), nsvtlp(26.99%)…

Yield and Robustness Analysis

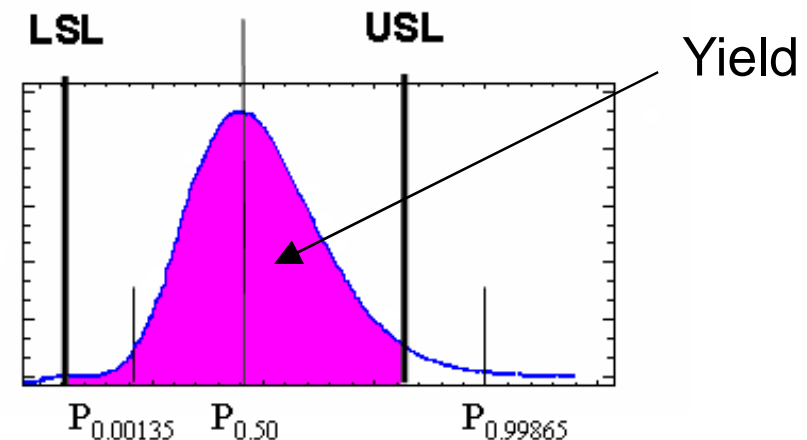$$Cpk = \min\left(\frac{USL - P_{0.50}}{P_{0.99865} - P_{0.5}}, \frac{P_{0.5} - LSL}{P_{0.50} - P_{0.00135}}\right)$$

LSL   USL

Yield

$P_{0.00135}$ $P_{0.50}$ $P_{0.99865}$

Worst-Case Analysis

- Find the sets of Process Parameters leading to Ymin and Ymax

Ex. : Ymin➔ poly_cd=3 nsvtlp=3 psvtlp=-3…

Ymax➔ poly_cd=-3 nsvtlp=-3 psvtlp=3…

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Statistical Static Timing Analysis (SSTA)

3σ parameter total variation relative to nominal value
[Source: S. Nassif, IBM]

Lot-to-Lot

Wafer-to-Wafer

Within-Die Variation

Die-to-Die

source

sink

Within-Die

Design Slack

Time

Design Yield

F*   20%

Frequency

Die-to-Die Variation
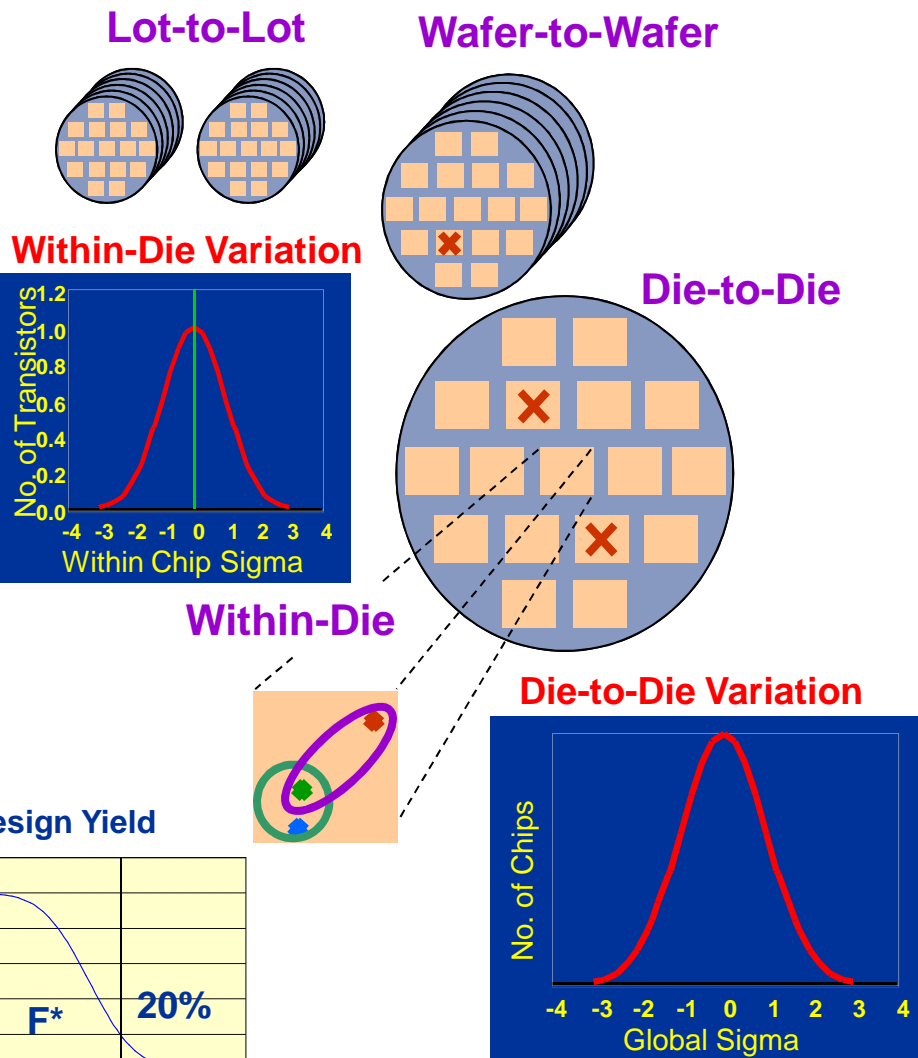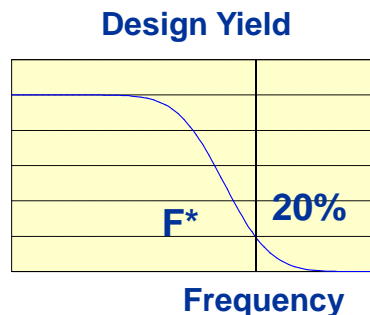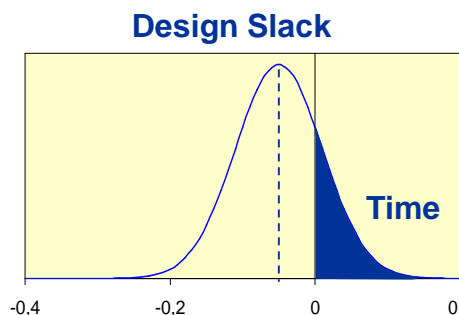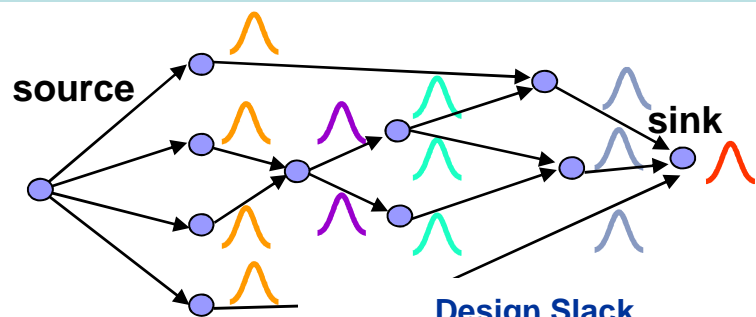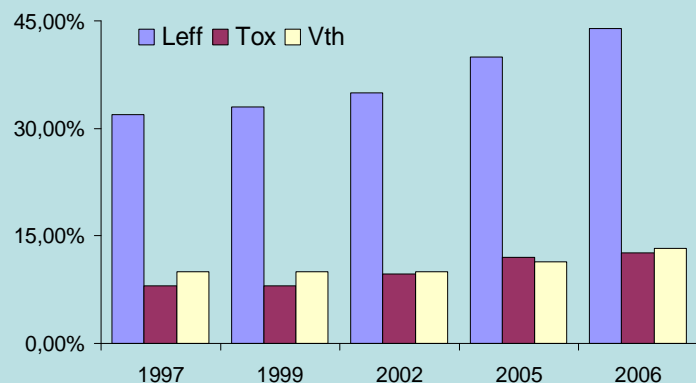
Courtesy of D.Pandini/C.Forzan

Why Statistical Static Timing Analysis?

- Statistical Static Timing Analysis (SSTA) has been proposed:
    - To deal with circuit timing uncertainty
    - As an alternative to *corner*-case analysis
- SSTA basic concept:
    - Propagate delay distributions, instead of deterministic delays, along the timing graph
    - Compute node and path delay distributions
    - Estimate the distribution of circuit delay as the joint distribution of path delays
    - Find the chip timing yield from circuit delay distribution
- What is different?
    - Critical paths are not well defined
    - Every path can be critical under some probability
    - there is a general agreement on the fact that traditional derating is not going to work to model the on-chip random variations

Courtesy of D.Pandini/C.Forzan

Path Length

- For different path lengths we simulate D2D variations (=Global), mismatch (=Local random) variations, and the *rms* sum
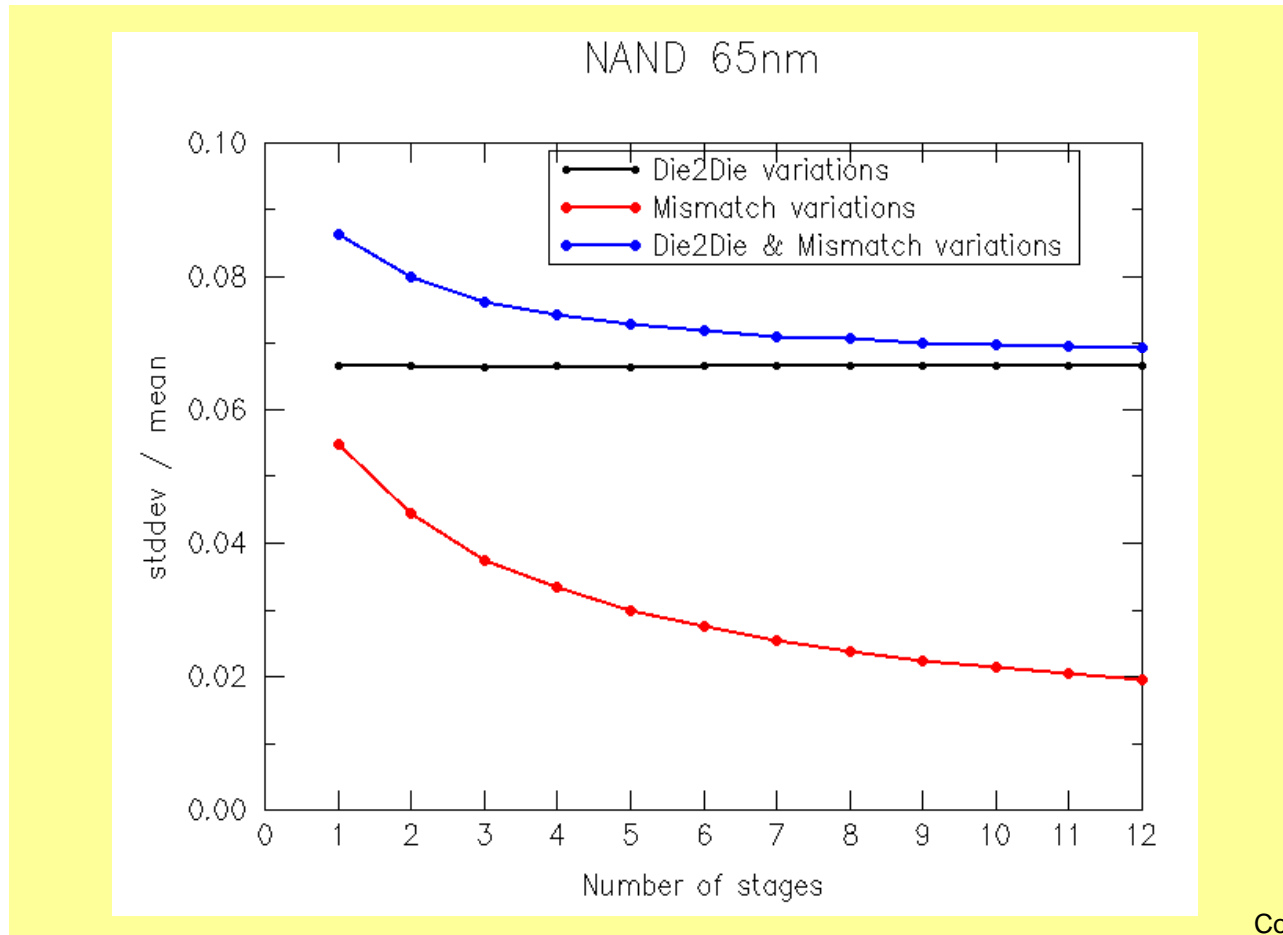
Courtesy of D.Pandini/C.Forzan

Path Length

- Derating cannot correctly model local random variations (mismatch)

Optimistic for short paths

Pessimistic for long paths

NAND 65nm

Derating

Legend:
- Die2Die variations
- Mismatch variations
- Die2Die & Mismatch variations

y-axis: stddev / mean (0.00, 0.02, 0.04, 0.06, 0.08)
x-axis: Number of stages (0 through 12)
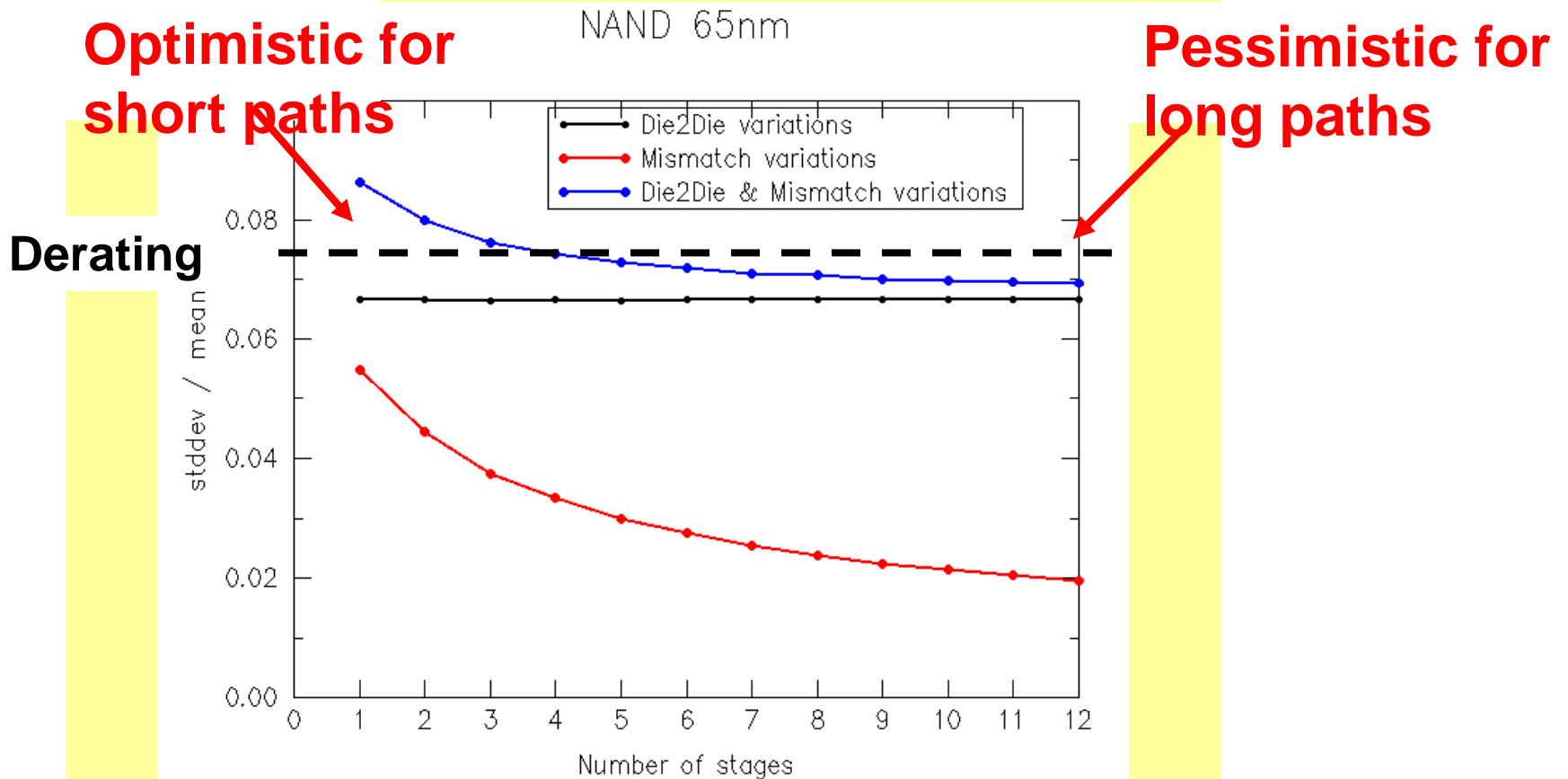
Courtesy of D.Pandini/C.Forzan

Challenges for SSTA

- Modeling data for SSTA
  - Which process parameters are most critical?
  - L_{eff}, V_T, T_{ox}, doping, ILD thickness, metal thickness, metal width
  - Obtaining inter-die (W2W and D2D) variations, intra-die variations (WID) and spatial information from raw data
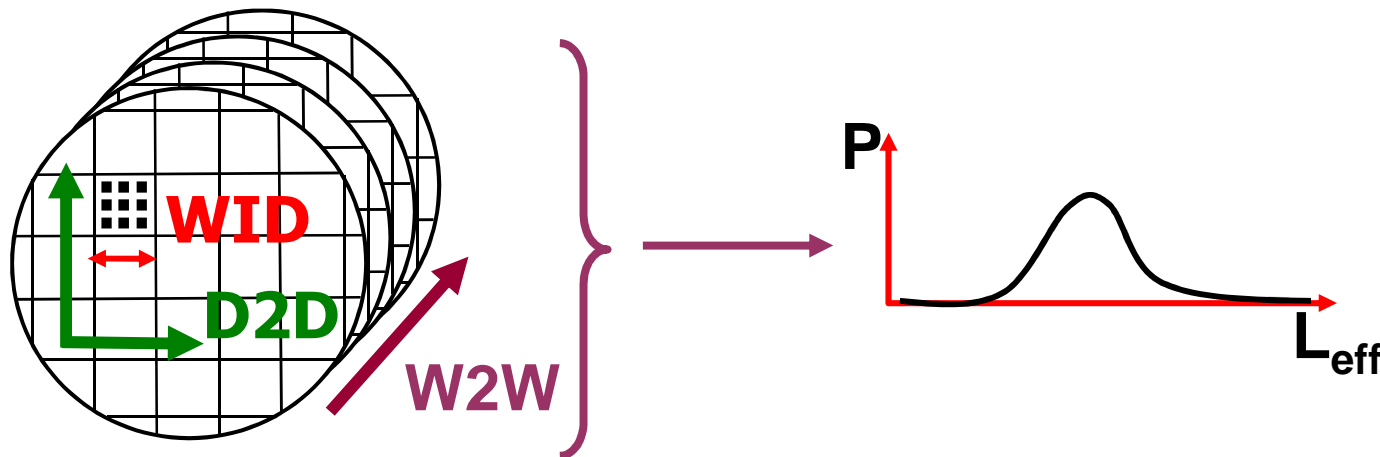
- Tracking process as it matures
- Representing process variations in the cell library

Courtesy of D.Pandini/C.Forzan

Outline

- Variations and Impact

- Statistical Compact Models

- Statistical Circuit Simulation
    - Analog DOE
    - Timing Analysis: STA, SSTA

- European project: Modern

- Conclusion

Modern EU project

- The objective of the MODERN project is to develop new paradigms in integrated circuit design that will enable the manufacturing of reliable, low cost, low EMI, high-yield complex products using unreliable and variable devices.

Specifically, the main goals of the project are:

➢ Advanced, yet accurate, models of process variations for nanometre devices, circuits and complex architectures.

➢ Effective methods for evaluating the impact of process variations on manufacturability, design reliability and circuit performance.
  o Reliability, noise, EMC/EMI.
  o Timing, power and yield.

➢ Design methods and tools to mitigate or tolerate the effects of process variations on those quantities applicable at the device, circuit and architectural levels.

➢ Validation of the modelling and design methods and tools on a variety of silicon demonstrators.
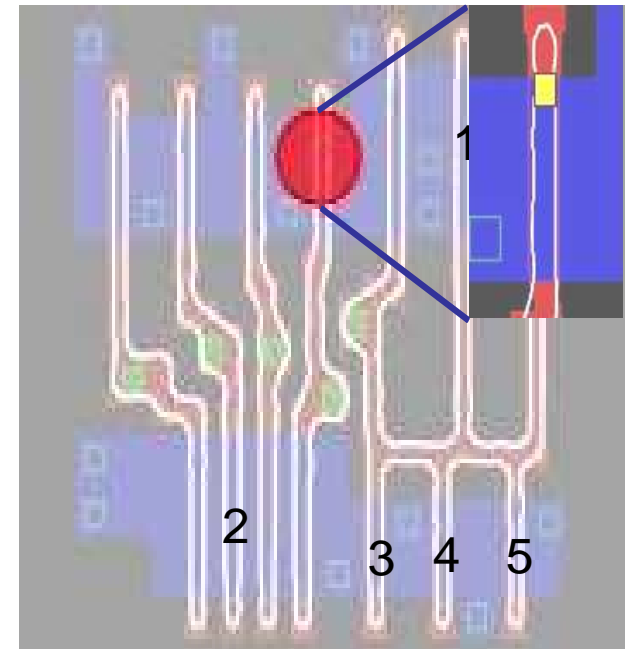
Layout and strain induced variability (Synopsys)

More information on MODERN can be found at http://www.eniac-modern.org/

- The MODERN **Consortium** features strong *competence* and *expertise* in the field of *advanced technologies*, with a well-balanced participation between *Large Industries, SMEs, Research Centres* and *Universities* from all over Europe.
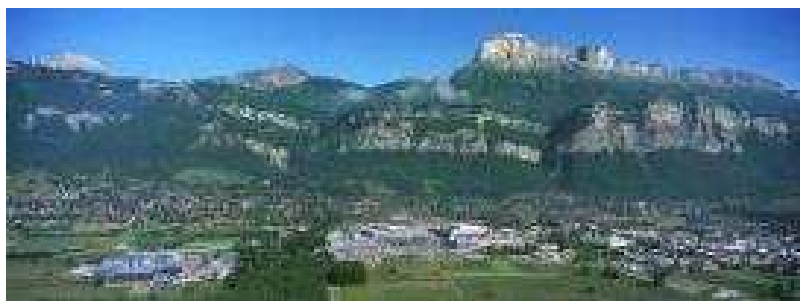
28 Partners

9 Countries
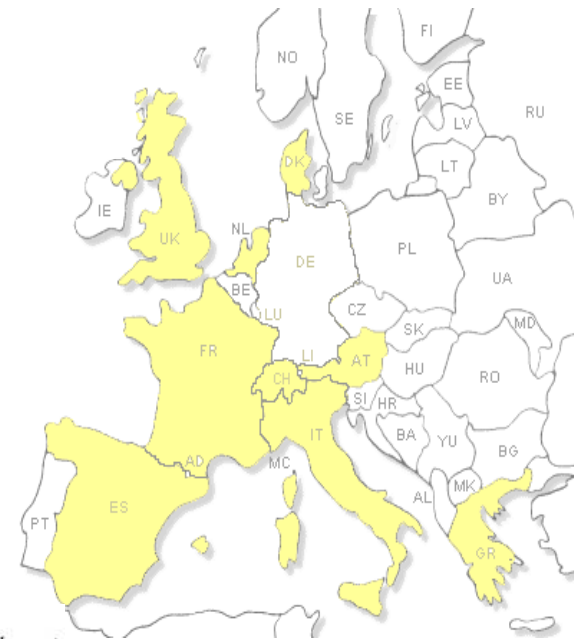
Conclusion

- Joint effort is needed in TCAD, Characterization, Compact Modeling, and Circuit simulation methods, concurently with tremendous effort for technology development

- TCAD :
    - Comprehensive analysis of *local random* variability and *reliability statist*ics.
    - Validation on existing materials and devices
    - Estimation of impact on new materials and devices for coming technology nodes

- Statistical Compact Modeling:
    - Physics based and Accurate compact models over Process Voltage Temperature
    - Method for extracting Statistical models: BPV? NPM? Just for mature technologies?

- Statistical Circuit simulation
    - MC methods are proven efficient/accurate when applied to DOE-RSM Polynomial models
    - Performance aware Corner simulation still help when MC is not applicable
    - Timing analysis: SSTA?

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Thank you!