SYNOPSYS®
Predictable Success

# Modeling Random Variability of 16nm Bulk FinFETs

Victor Moroz, Qiang Lu,
and Munkang Choi

September 9, 2010

**SISPAD 2010 Variability Workshop**

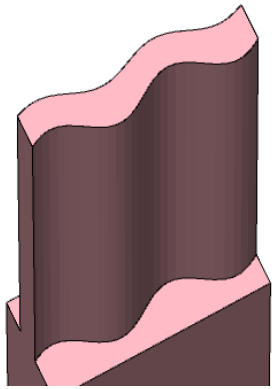
# Outline

- LER effects for litho and spacer litho
- Random dopant fluctuations
- Stress engineering
- Conclusions

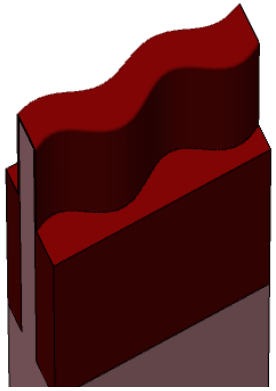
# Outline

- **LER effects for litho and spacer litho**
- Random dopant fluctuations
- Stress engineering
- Conclusions

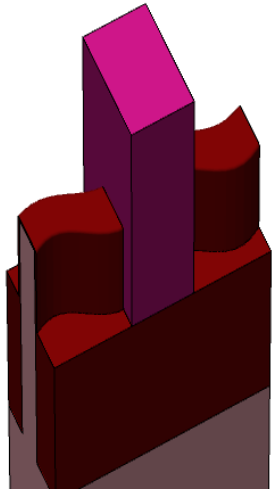
# 16nm Bulk FinFETs for 16nm Node



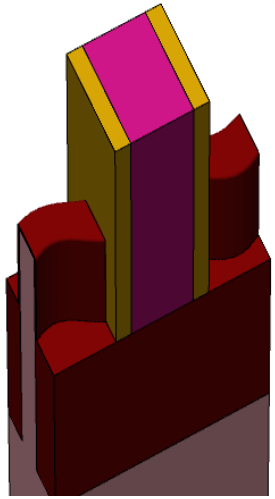
Define fin
(spacer litho shown)



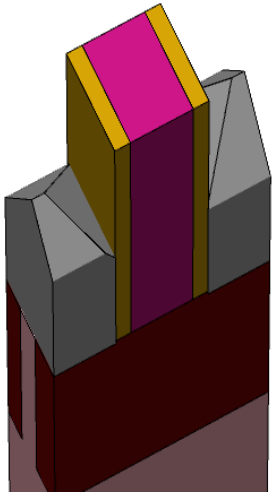
STI



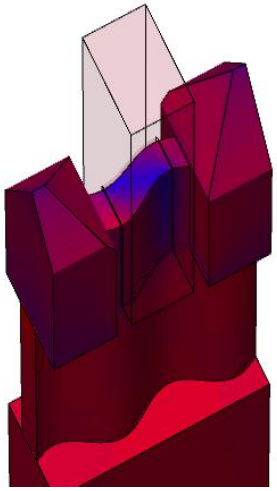
Poly gate



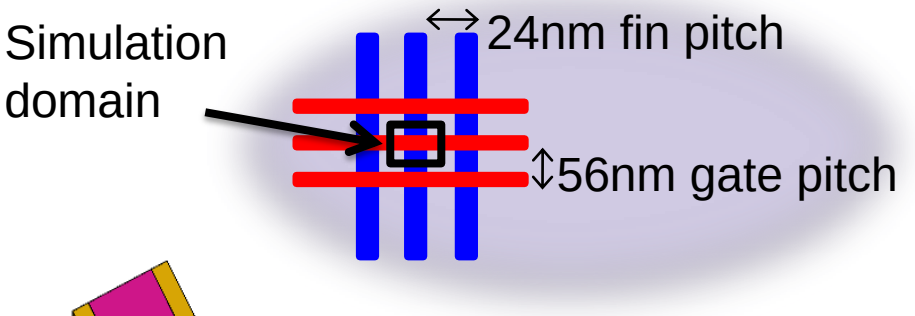
Spacers



S/D epitaxy

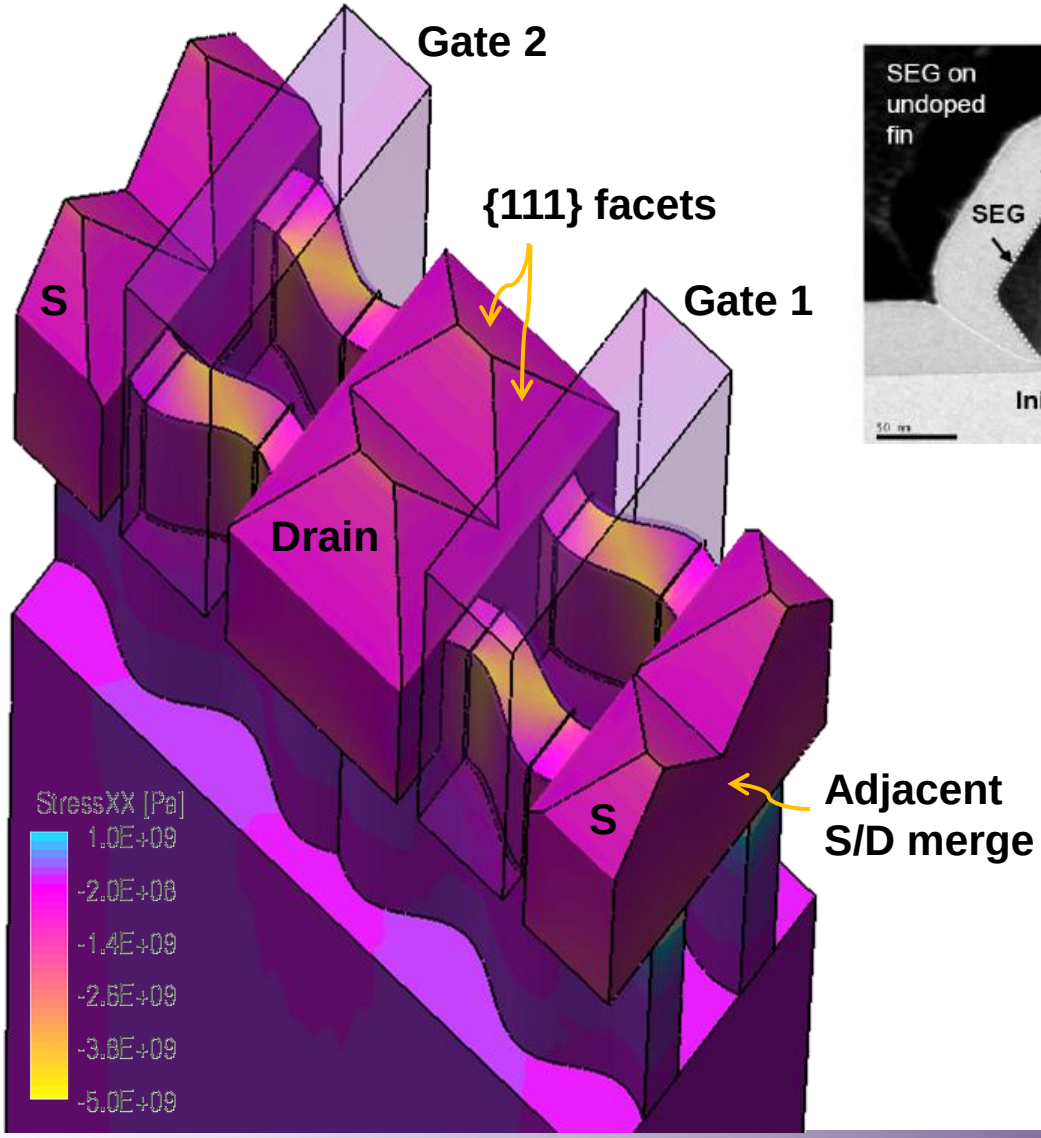


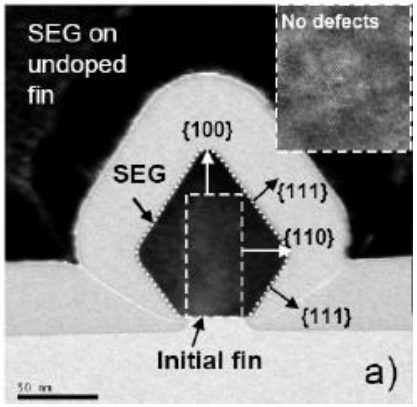
HKMG

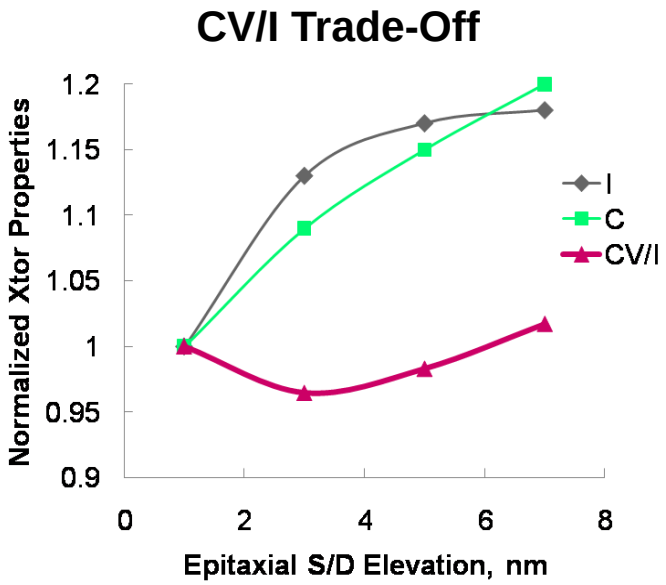



- 0.8 V Vdd
- 0.8 nm EOT
- 32 nm tall fins
- 8 nm wide fins
- Undoped channel
- In-situ doped S/D epi
- 33% Ge SiGe PMOS S/D

# S/D Shape Affects Stress, $R_{cont}$, and $C_{par}$

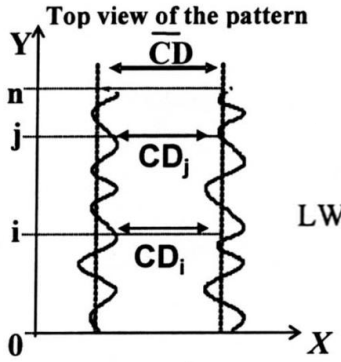


# LER Analysis

**LWR definition:**




$$LWR(3\sigma) = 3\sqrt{\frac{\sum_{i=0}^{n}(CD_i - \overline{CD})^2}{n}}$$

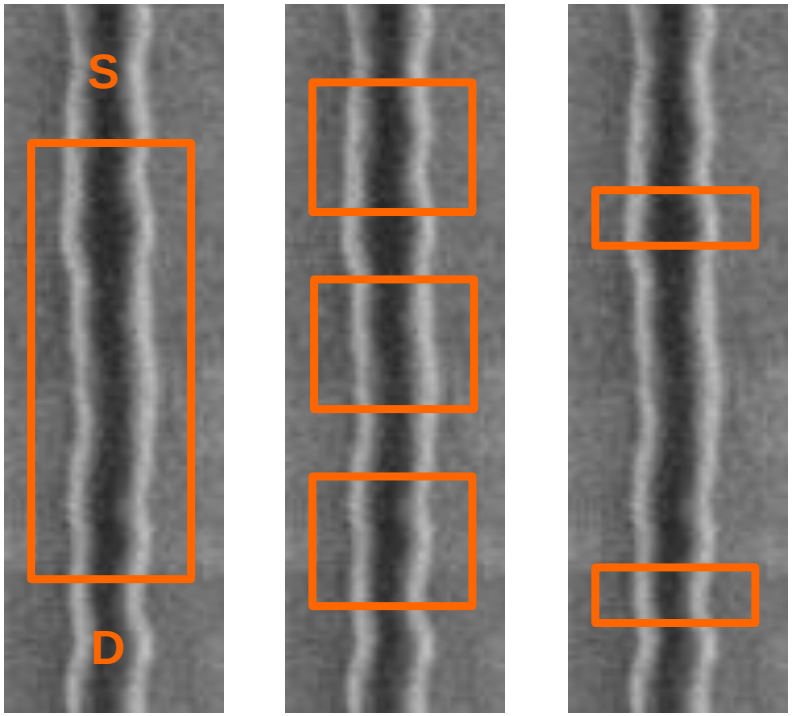
**Typical LWR is ~9nm:**

| Technological steps | Resist LWR (nm) | BARC LWR (nm) | poly-Si LWR (nm) | ΔLWR (nm) |
|---|---|---|---|---|
| Lithography | 13.2 | ··· | ··· | |
| Ar plasma treatment | 10.2 | ··· | ··· | −3 |
| $CF_4$ BARC open | 9.2 | ··· | ··· | −4 |
| Gate etching | 9 | 8.1 | ··· | −5.1 |
| Stripping and HF | | | 9.1 | −4.1 |

**L > λ averages LER; no issues**

**L ~ λ requires random sampling**

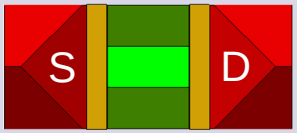
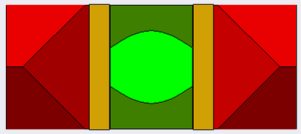
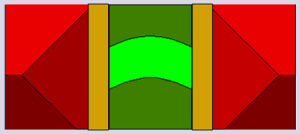
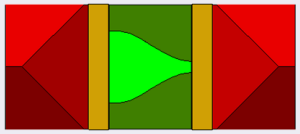
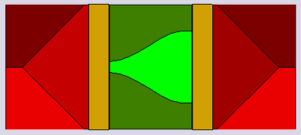
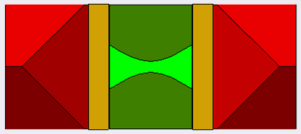
**L < λ: few extreme cases**



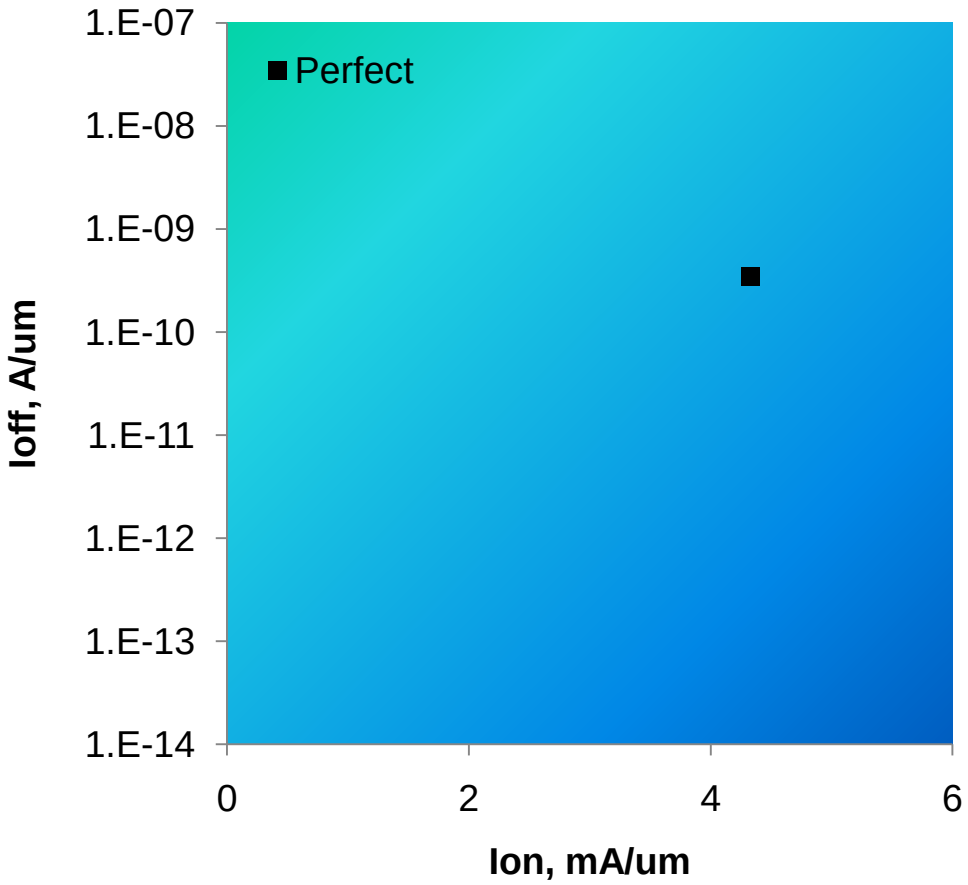

**>=65nm** **45nm - 22nm** **<=16nm**

- **Due to the LER wavelength λ~30nm >> fin size:**
- **Use a small set of deterministic extreme cases instead of massive random analysis**
- **A popular claim that etching is a "low pass filter" requires significant amount of under-etching that can not be used for tight fin pitches**

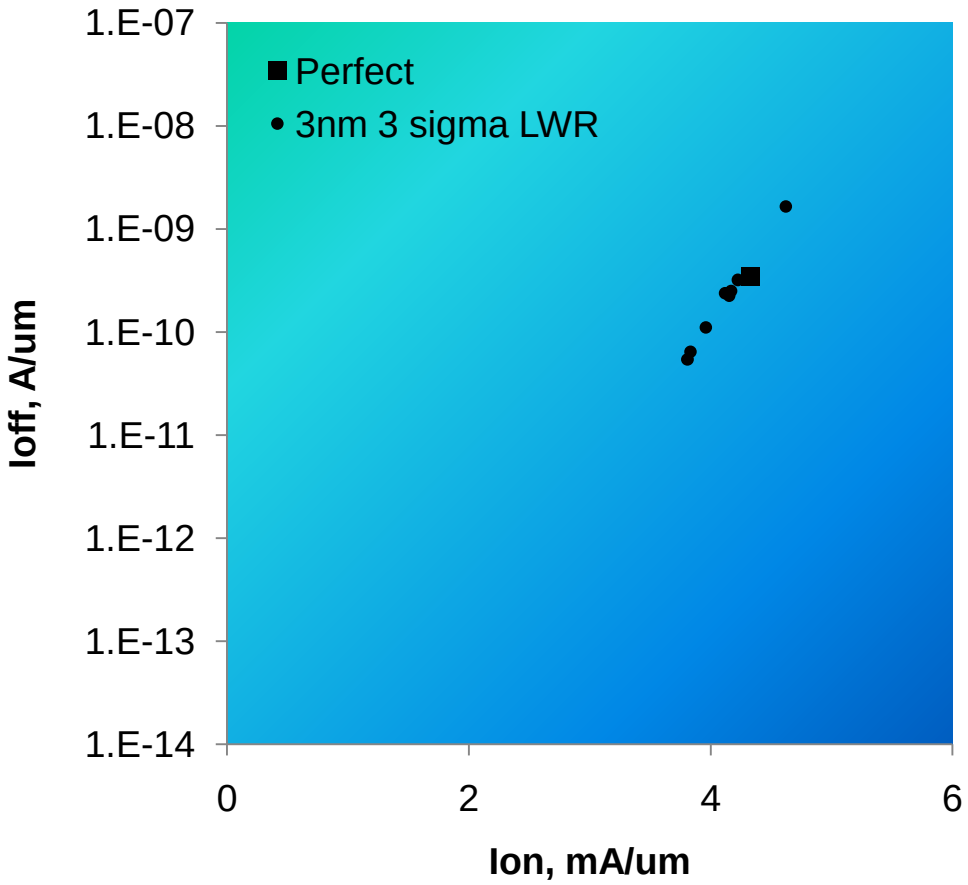
# Extreme FinFET Shapes for LER Analysis

| Fin shape | Edge #1 phase shift | Edge #2 phase shift | Comment |
|---|---|---|---|
|   | - | - | Perfect |
|  | 0 | $\pi$ | Fat |
|  | 0 | 0 | Bent |
|  | $\pi/2$ | $-\pi/2$ | Big source |
|  | $-\pi/2$ | $\pi$ | Big drain |
|  | $\pi$ | 0 | Thin |

# Perfect Rectangular 16nm FinFET

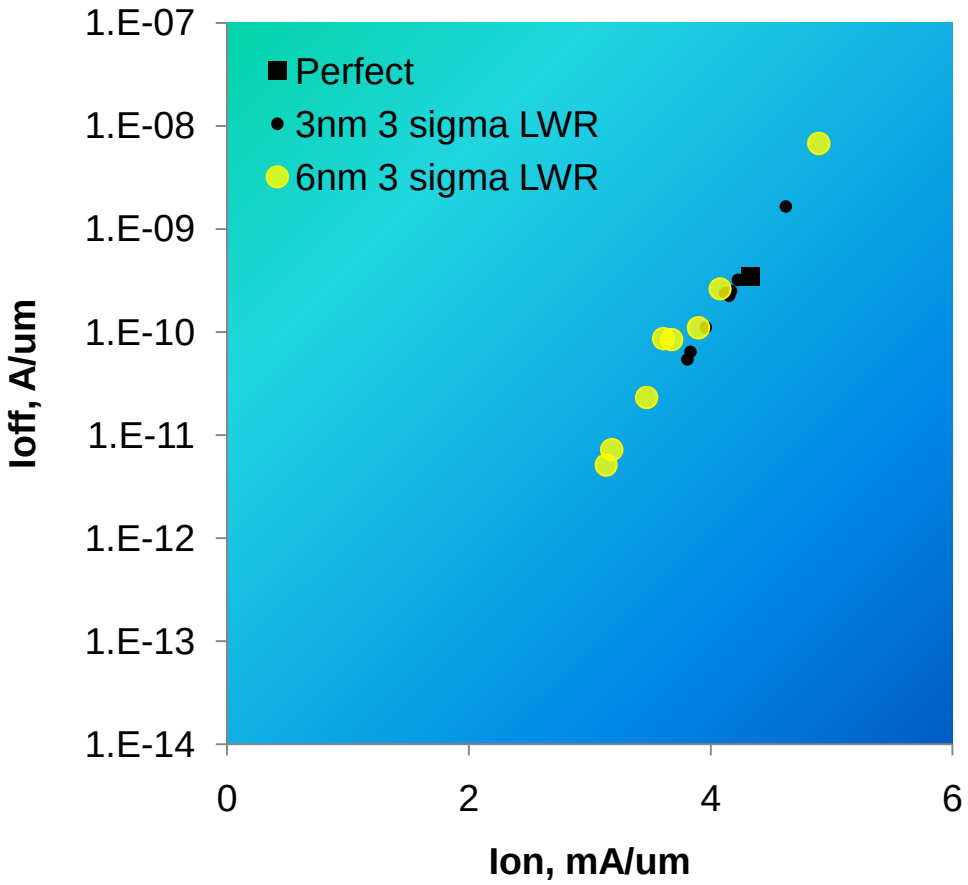


# LWR: 3 Sigma = 3 nm



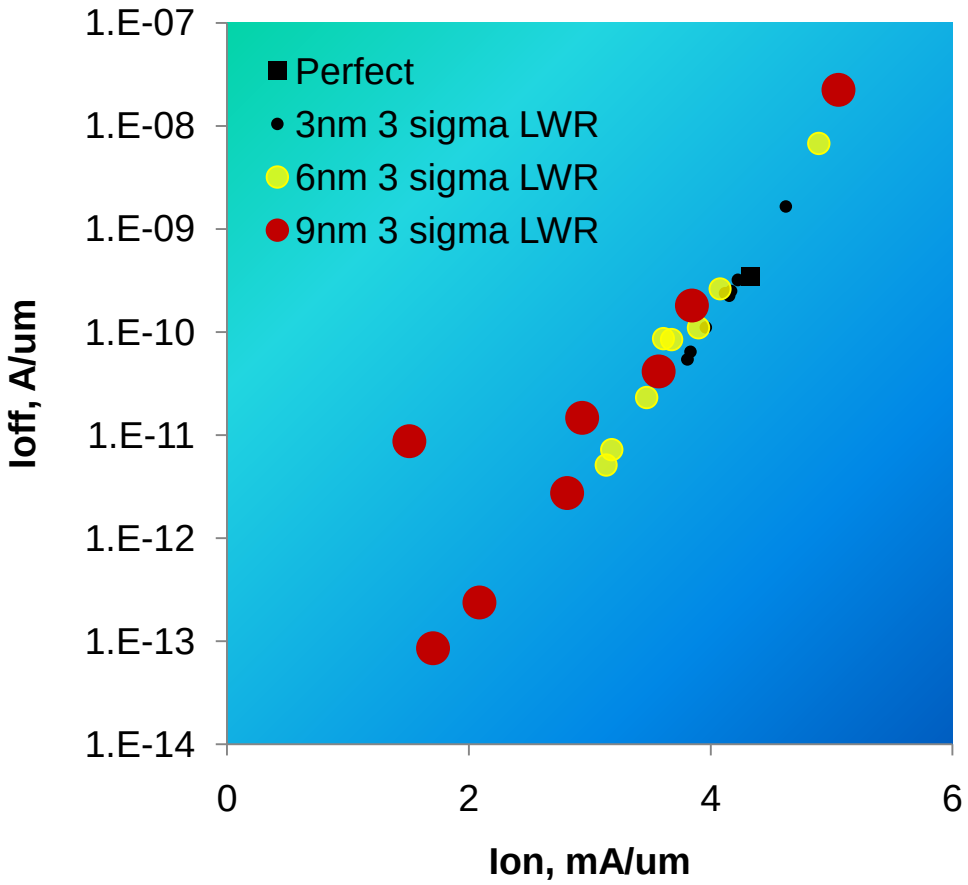

- 20% $I_{on}$ range
- 30x $I_{off}$ range

# LWR: 3 Sigma = 6 nm



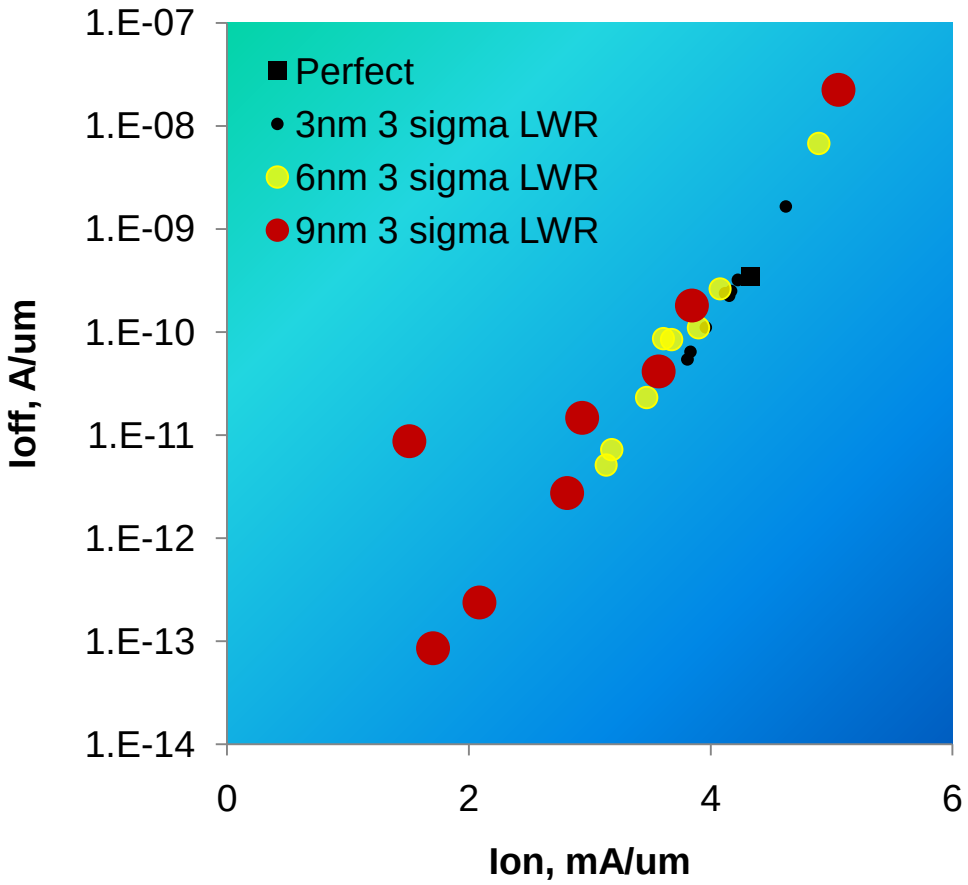

- 40% $I_{on}$ range
- 1300x $I_{off}$ range

# LWR: 3 Sigma = 9 nm



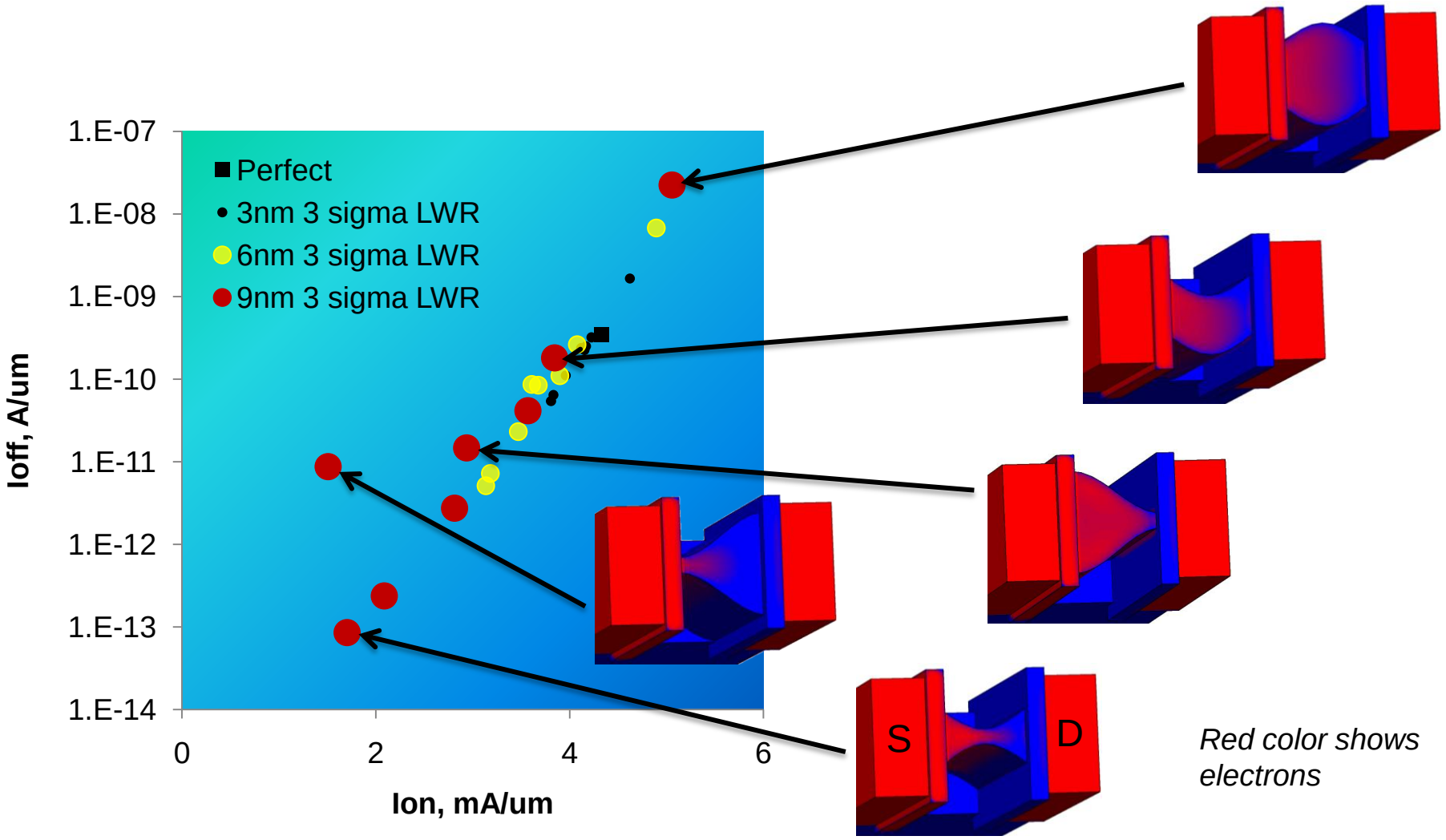

- 80% $I_{on}$ range
- 260,000x $I_{off}$ range
- ~400 mV $V_{tsat}$ variation

# LER: Unacceptable State-of-the-Art Litho

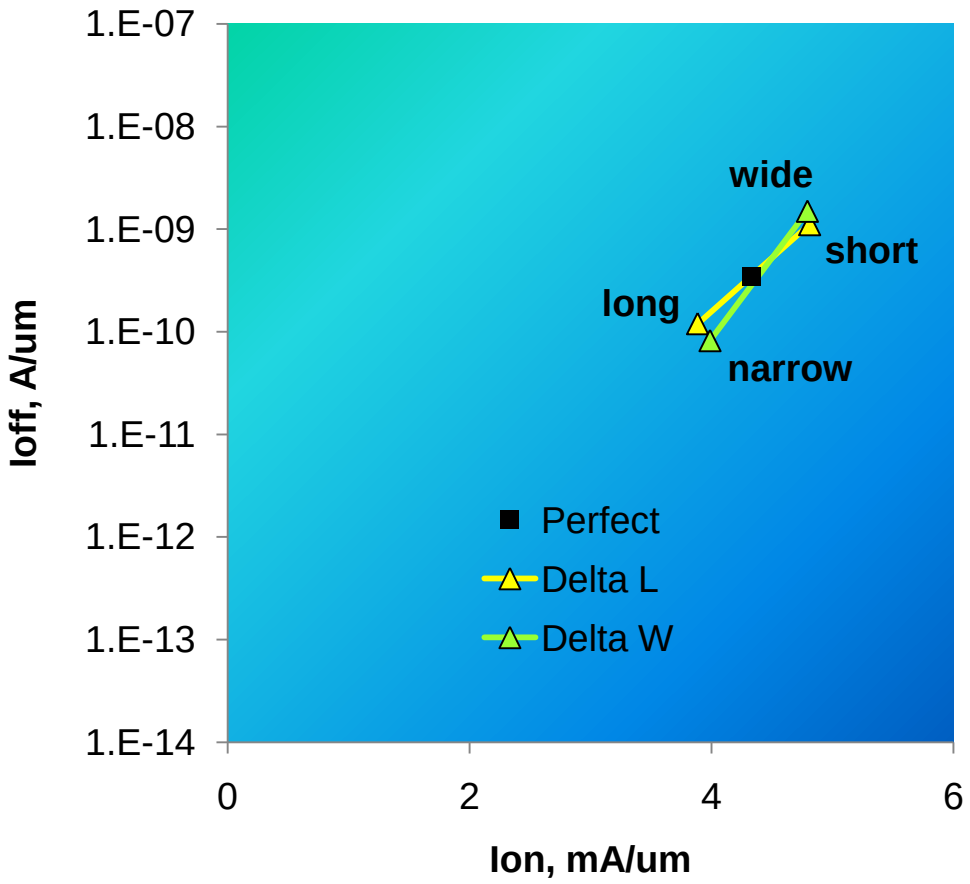



- All LER cases line up along the same Ion/Ioff trade-off curve
- No performance gap with the perfect rectangular fin
- Variability dramatically increases with LER amplitude
- Unacceptable variability above 3nm 3*Sigma LER

# LER: Particular Configurations



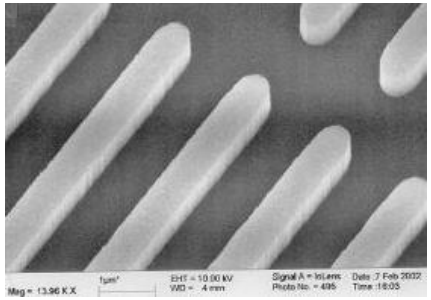
# ΔL and ΔW Sensitivities: Quite High



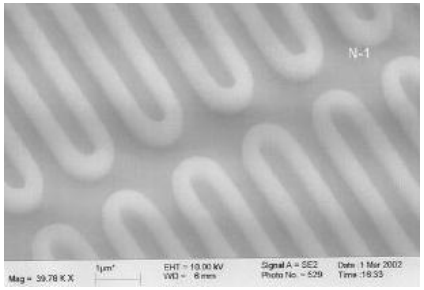

- 1nm change in L or W changes:
  - Ion by ~10% and
  - Ioff by ~4x
- No performance degradation, you move along the same Ion/Ioff trade-off curve
- Very similar ΔL and ΔW sensitivities, despite L~2W
- +/- 1nm L and W control is only possible with spacer litho

# Spacer Lithography Definition

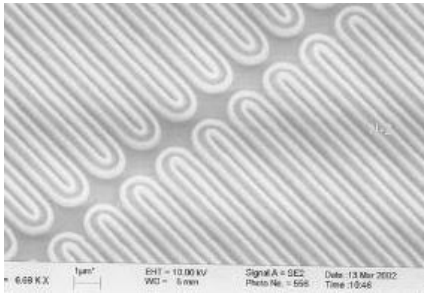
**Photo-lithographically defined sacrificial structures**



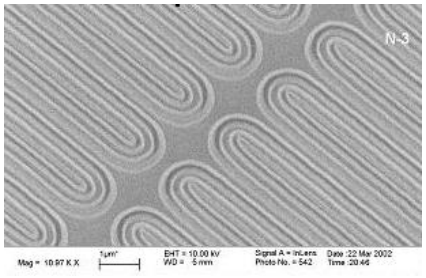
**1st Spacers**




**2nd Spacers**



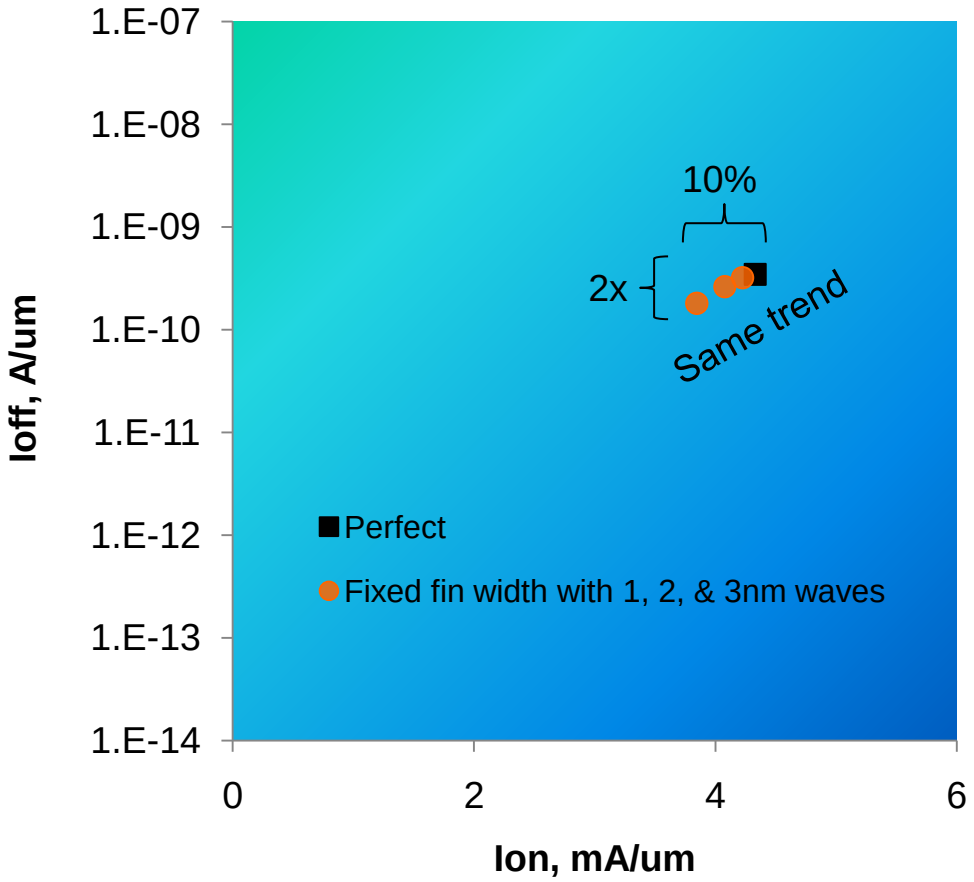
**3rd Spacers**

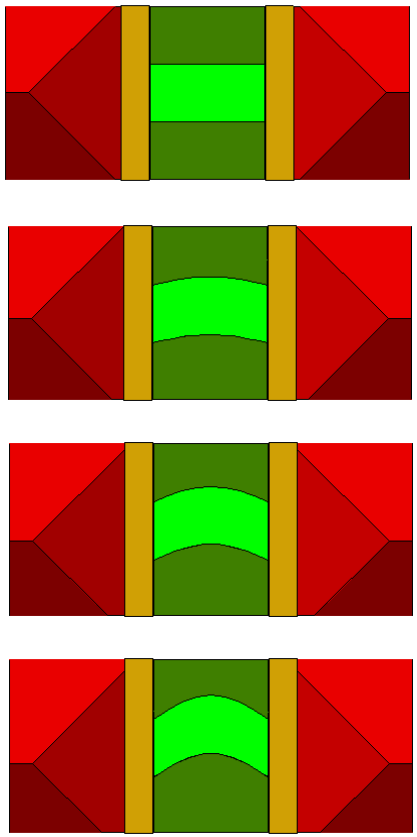



**$2^n$ lines after n iterations of spacer lithography!**

# Spacer Lithography: Small Impact

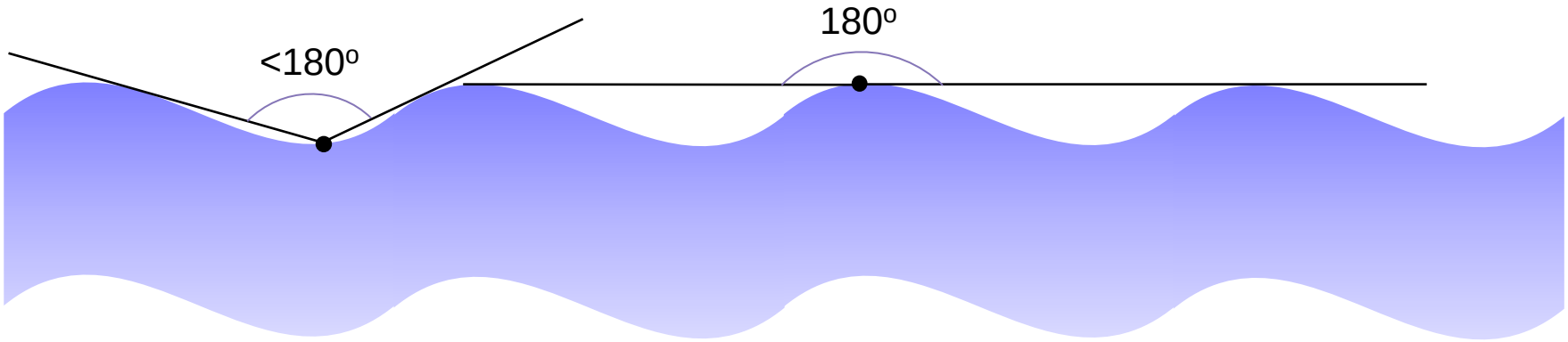
- **For the spacer lithography, the two fin edges are always in-sync**



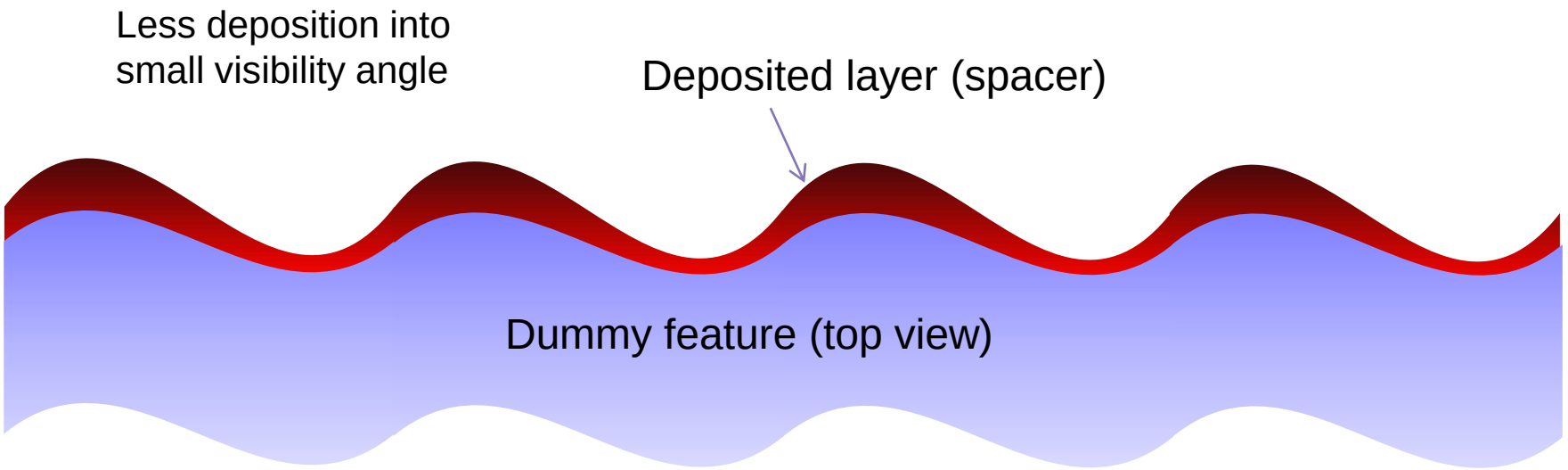



# Spacer Lithography Imperfections

Less deposition into
small visibility angle

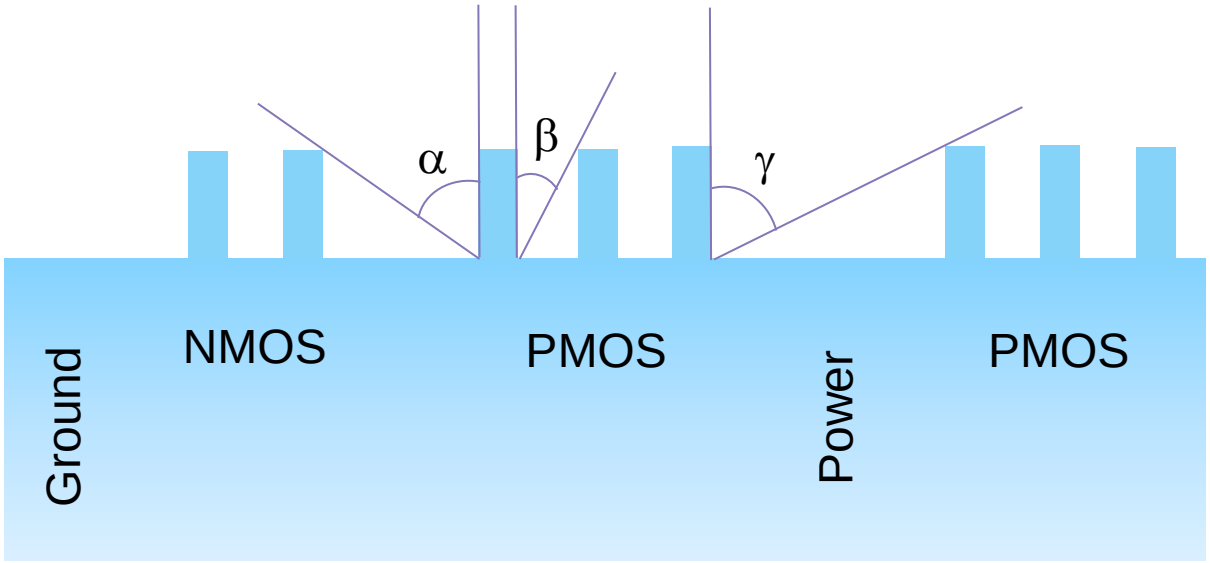


# Spacer Lithography Imperfections




- Deposition creates positive feedback, amplifying LER
- This gives you two edges that are in-sync (same phase), but different amplitudes
- Etching has the opposite, negative feedback, smoothing LER
- It might be possible to balance the deposition and etching effects, but
- Generally, spacer-litho-defined features will have some width variation

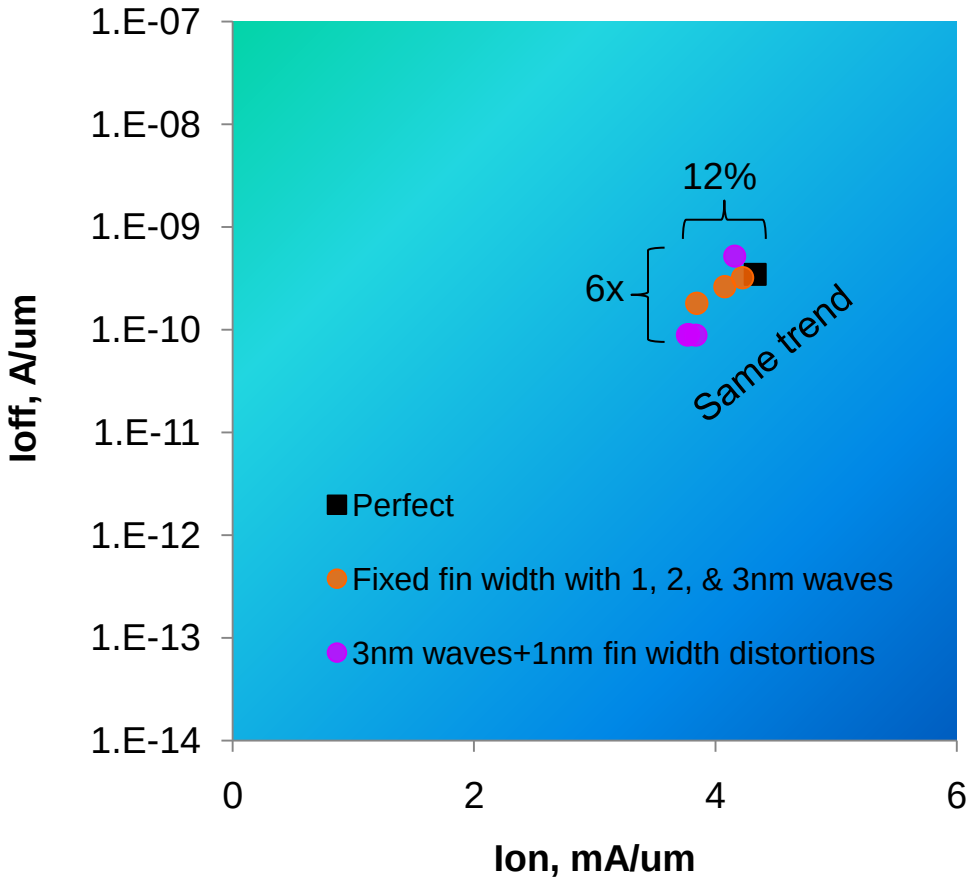
# Etch/Depo Micro-Loading Effects

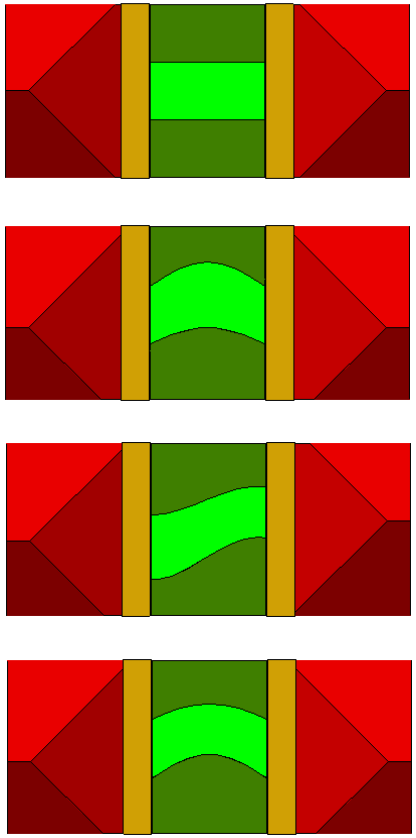



- Different fins experience different etch/deposition conditions
- Due to local visibility angles and pattern density
- This leads to variability in fin width and layer thicknesses

# Imperfect Spacer Litho: Still OK

- **For the spacer lithography, the two fin edges are always in-sync**



**Perfect**

**Mid-thick**

**Drain-thick**

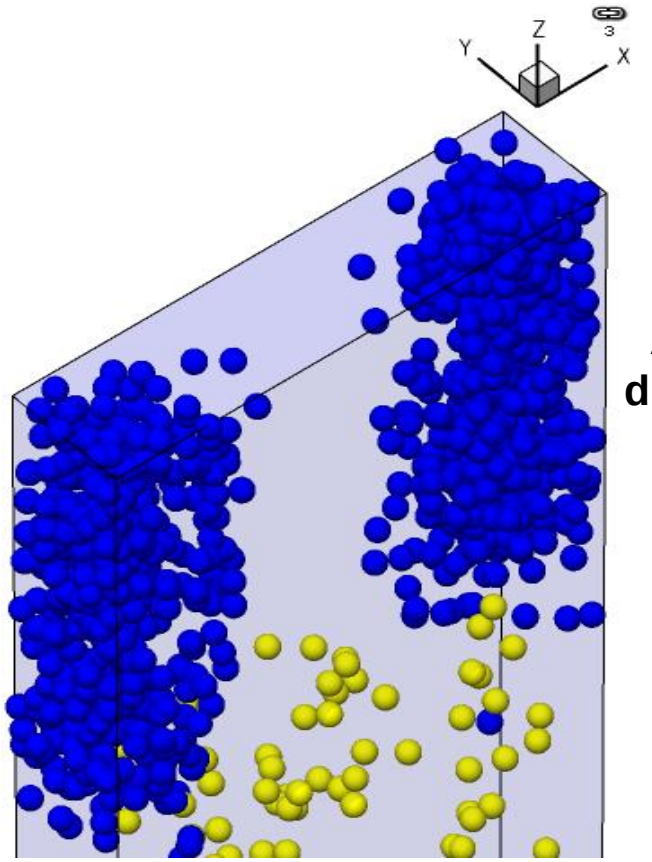
**Mid-thin**

*Spacer litho is "green": always reduces leakage!*

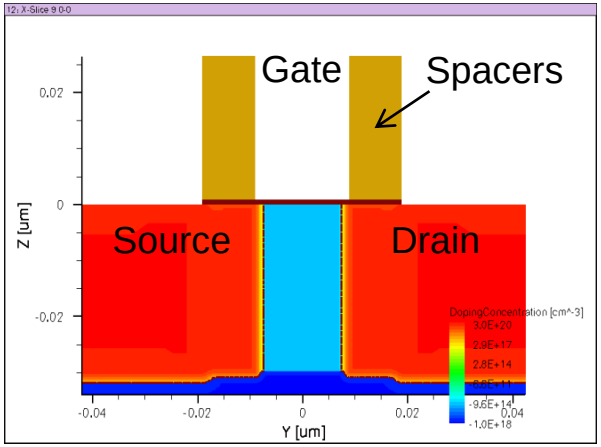
# Outline

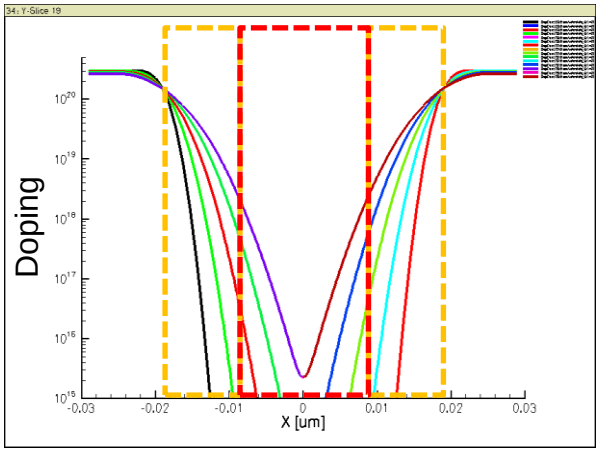
- LER effects for litho and spacer litho
- **Random dopant fluctuations**
- Stress engineering
- Conclusions

# Random Dopant Fluctuations



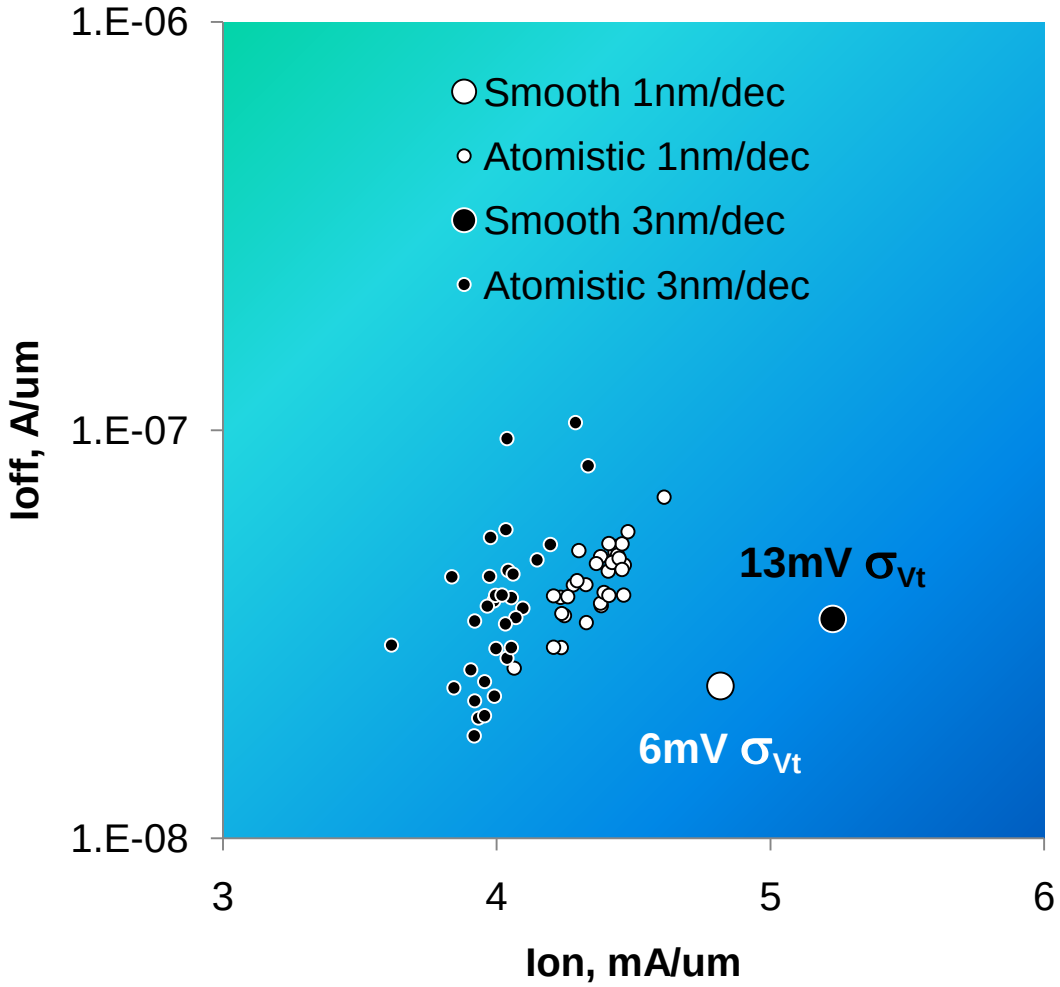

## Different junction abruptness



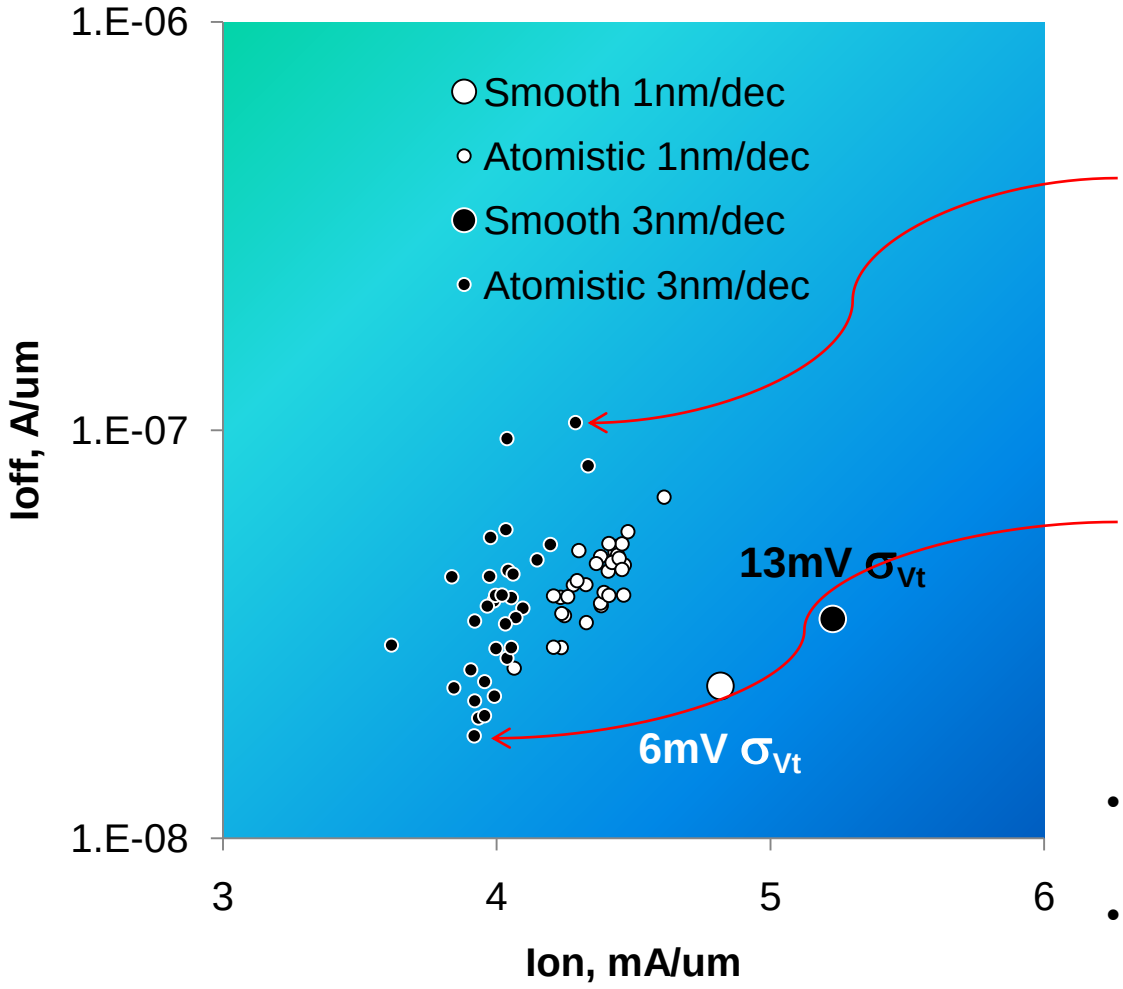

Source Spacer Gate Spacer Drain

# RDF: Insensitive to Junction Abruptness

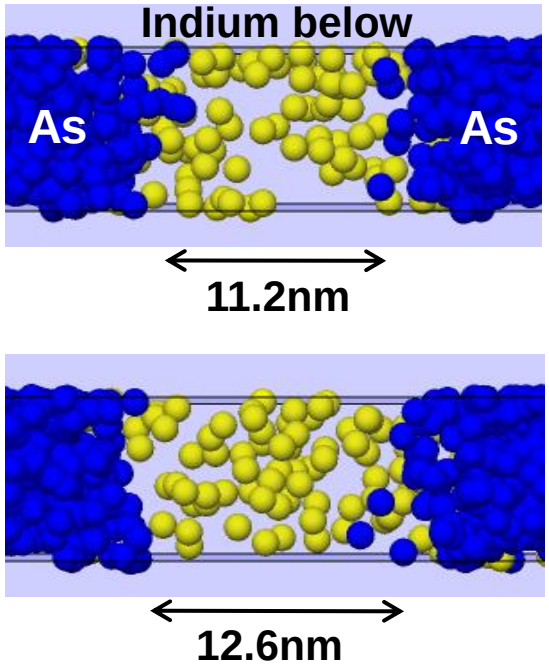



- Smooth junctions give similar performance for different amounts of abruptness
- The amount of RDF variability is quite moderate
- With junction abruptness degrading from 1nm/dec to 3nm/dec, $\sigma_{Vt}$ only doubles
- Surprisingly low RDF sensitivity to junction abruptness
- Indium channel-stop RDF contribution is negligible

# S/D RDF: Consistent with ΔL Variation

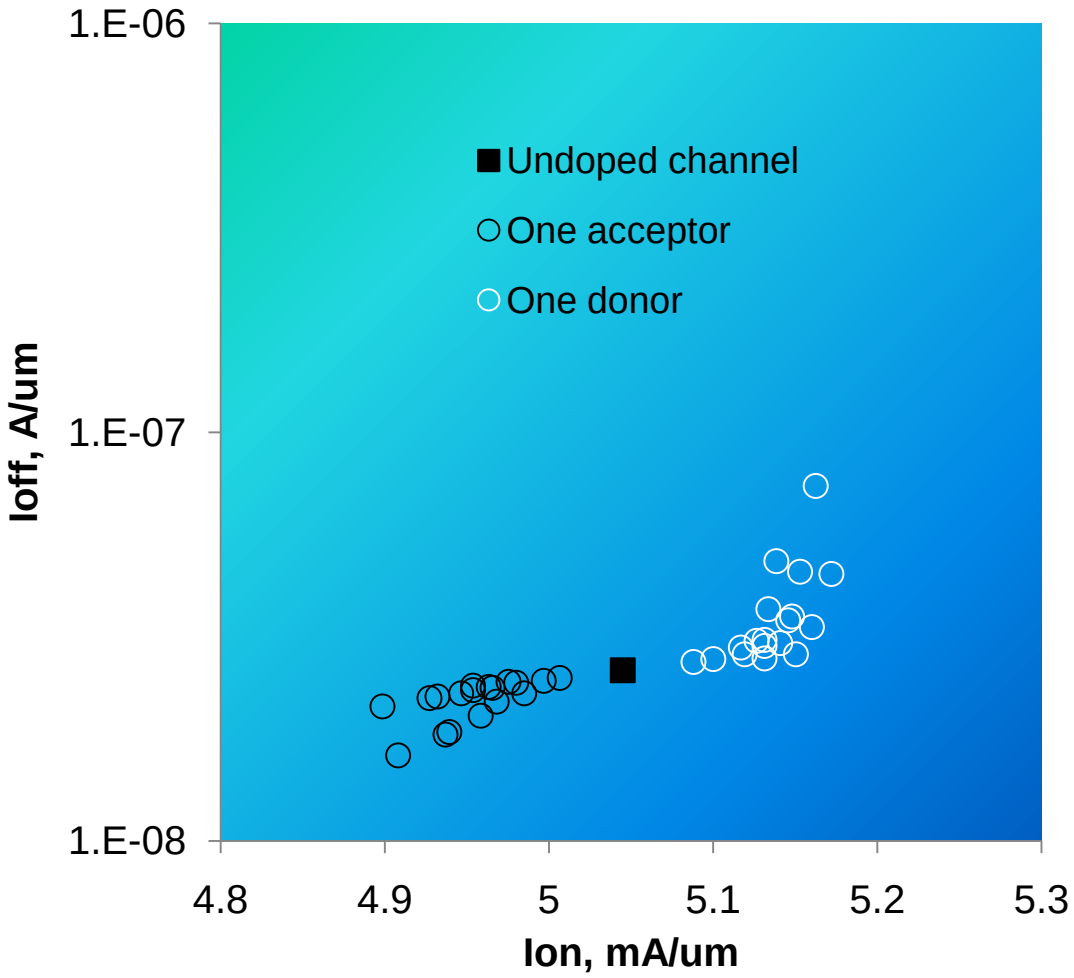



**Top view of the fin:**



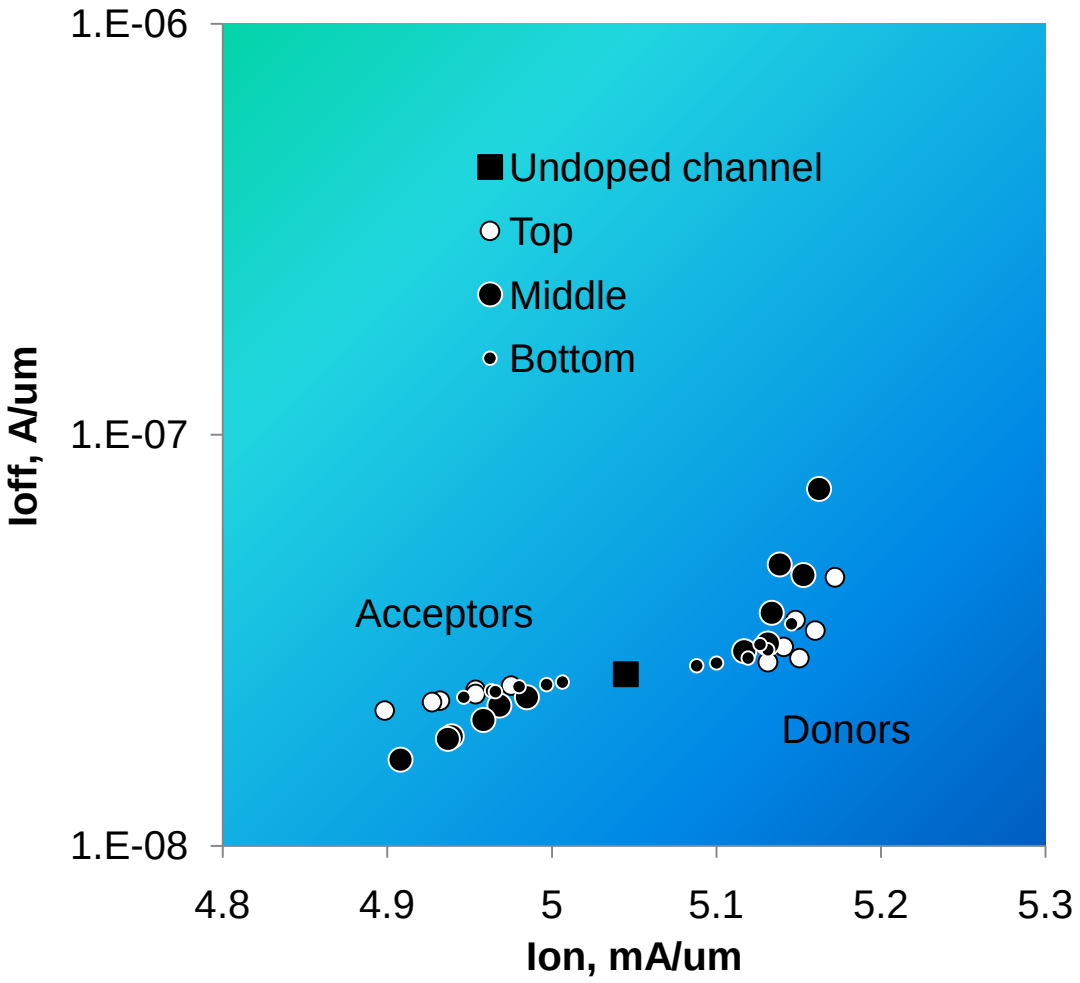

- **Apparent channel length difference is ~1.4nm**
- **S/D RDF are consistent with the ΔL sensitivity of 4x $I_{off}$ per 1nm**

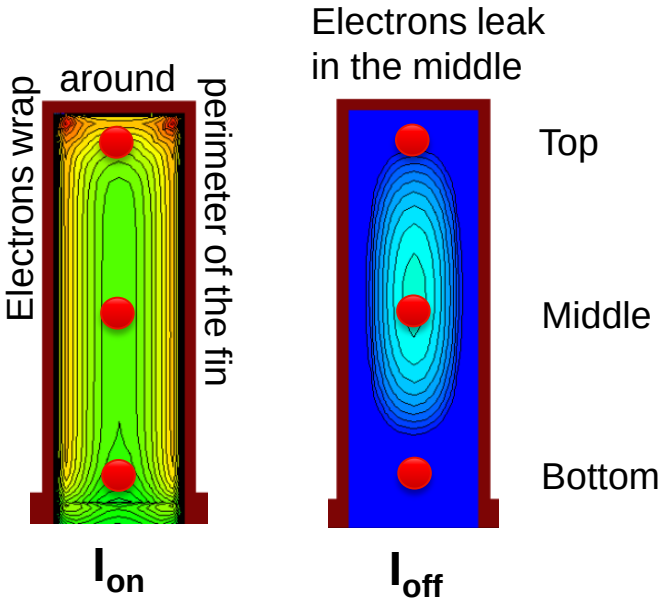
# Single Dopant in the Channel: ~3e17 cm$^{-3}$




- Donor “opens” the channel for $I_{off}$ (3x), but not $I_{on}$ (3%)
- Acceptor “blocks” the channel
- The impact is not catastrophic

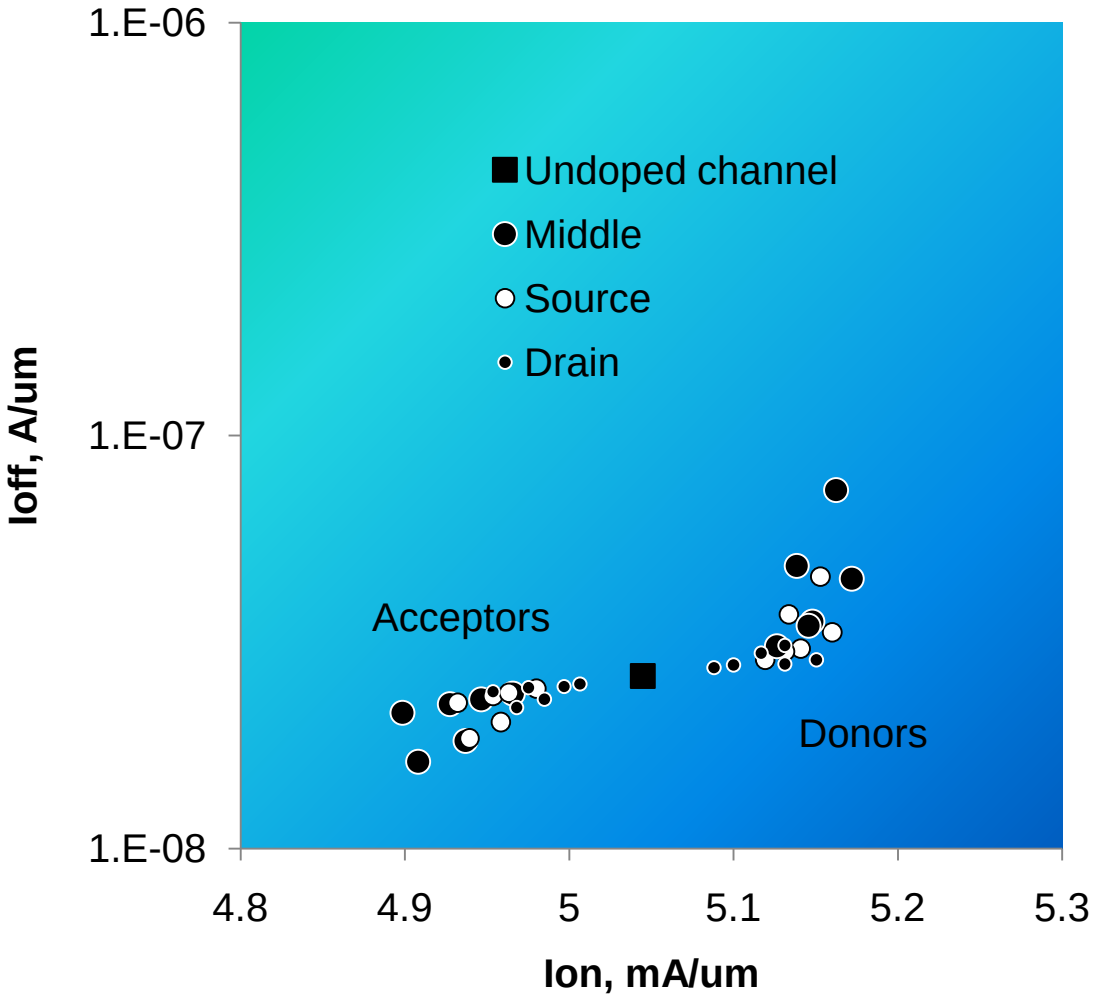
# Single Dopant: Worst at Mid-Height

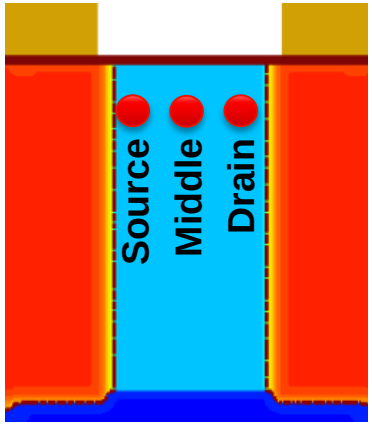



- Ions in the middle of the fin height affect $I_{off}$ the most
- Ions at the top of the fin affect $I_{on}$ the most
- Ions at the bottom of the fin have the least impact

# Single Dopant: Worst at Mid-Length



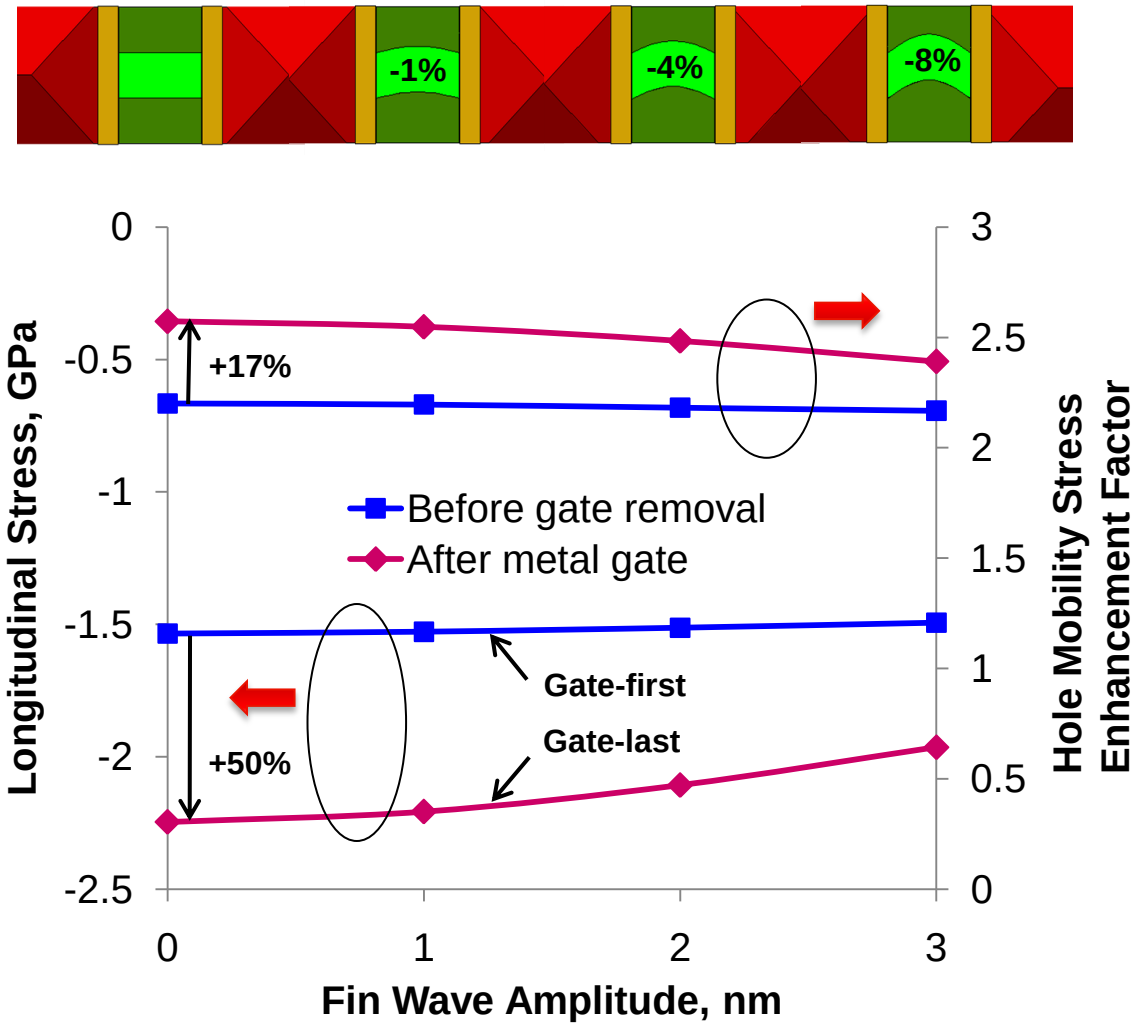




- Ions in the middle of the fin length have the most impact
- Ions at the source side have less impact
- Ions at the drain side have the least impact

# Outline

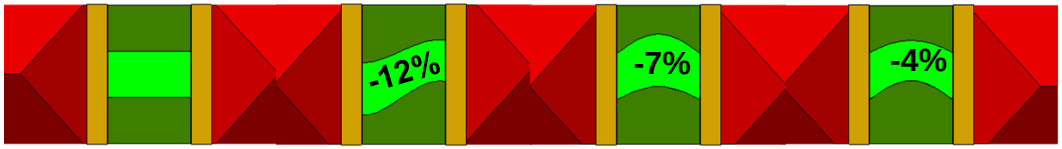
- LER effects for litho and spacer litho
- Random dopant fluctuations
- **Stress engineering**
- Conclusions

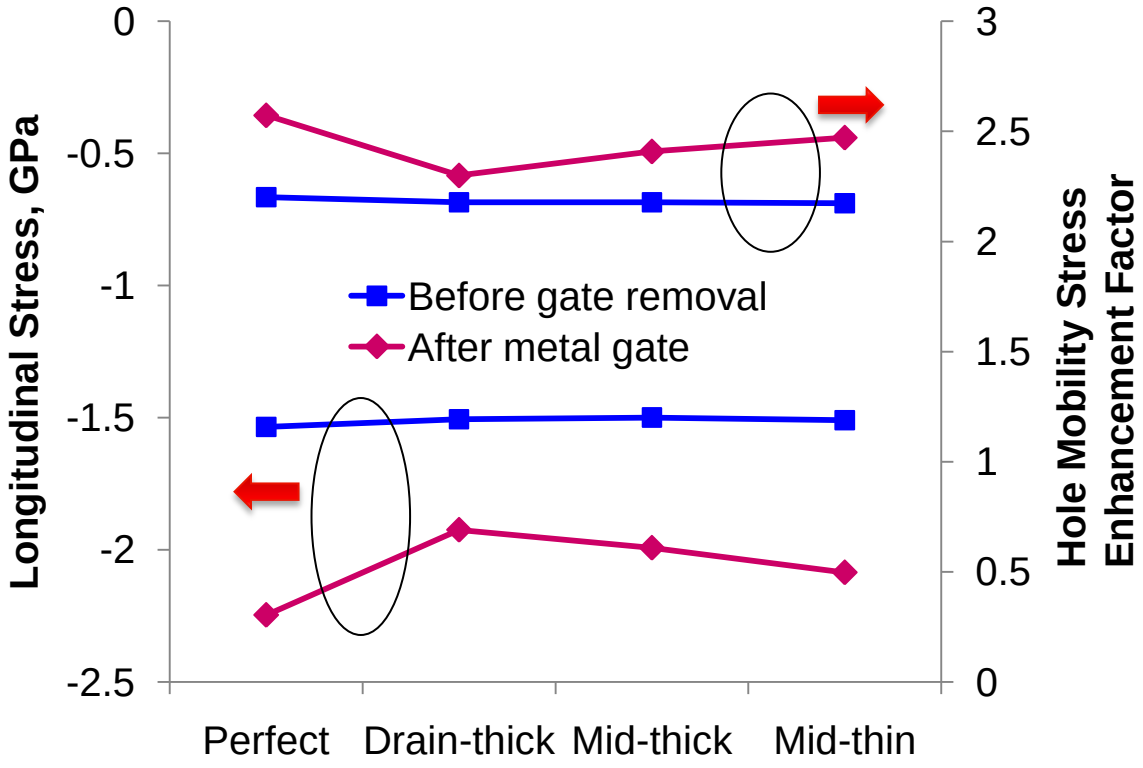
# Stress Variation for Spacer Litho




- Stress and mobility values are averaged over the entire fin channel volume
- Both the stress and the mobility increase upon poly removal
- Mobility enhancement degrades with fin curvature
- This adds (i.e. positive feedback) to the longer L with fin curvature

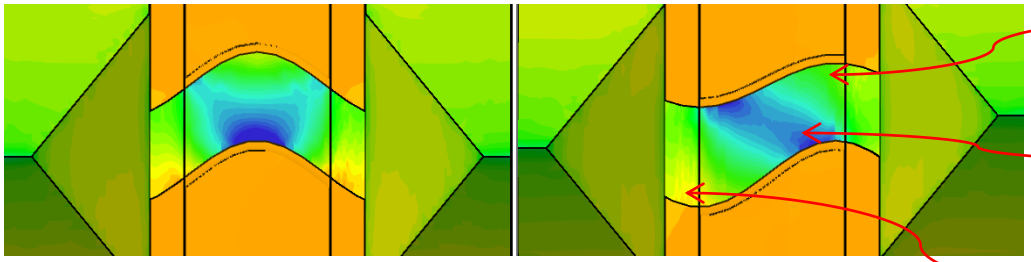
# Stress Variation for Distorted Spacer Litho

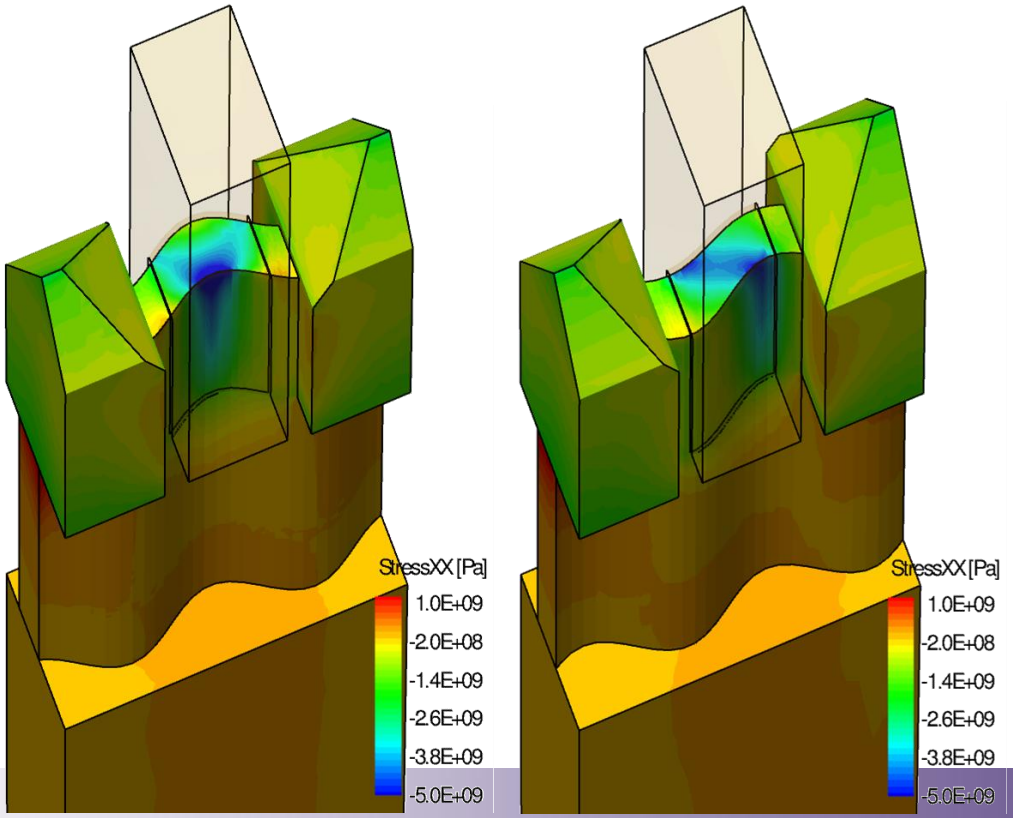



- Before poly gate removal for the gate-last HKMG, stress levels are very similar
- However, after the poly removal, stress increases, but the amount is geometry-specific
- All non-rectangular shapes reduce mobility despite using the best patterning option: spacer lithography
- Gate-first HKMG has remarkably lower stress but remarkably lower stress variation

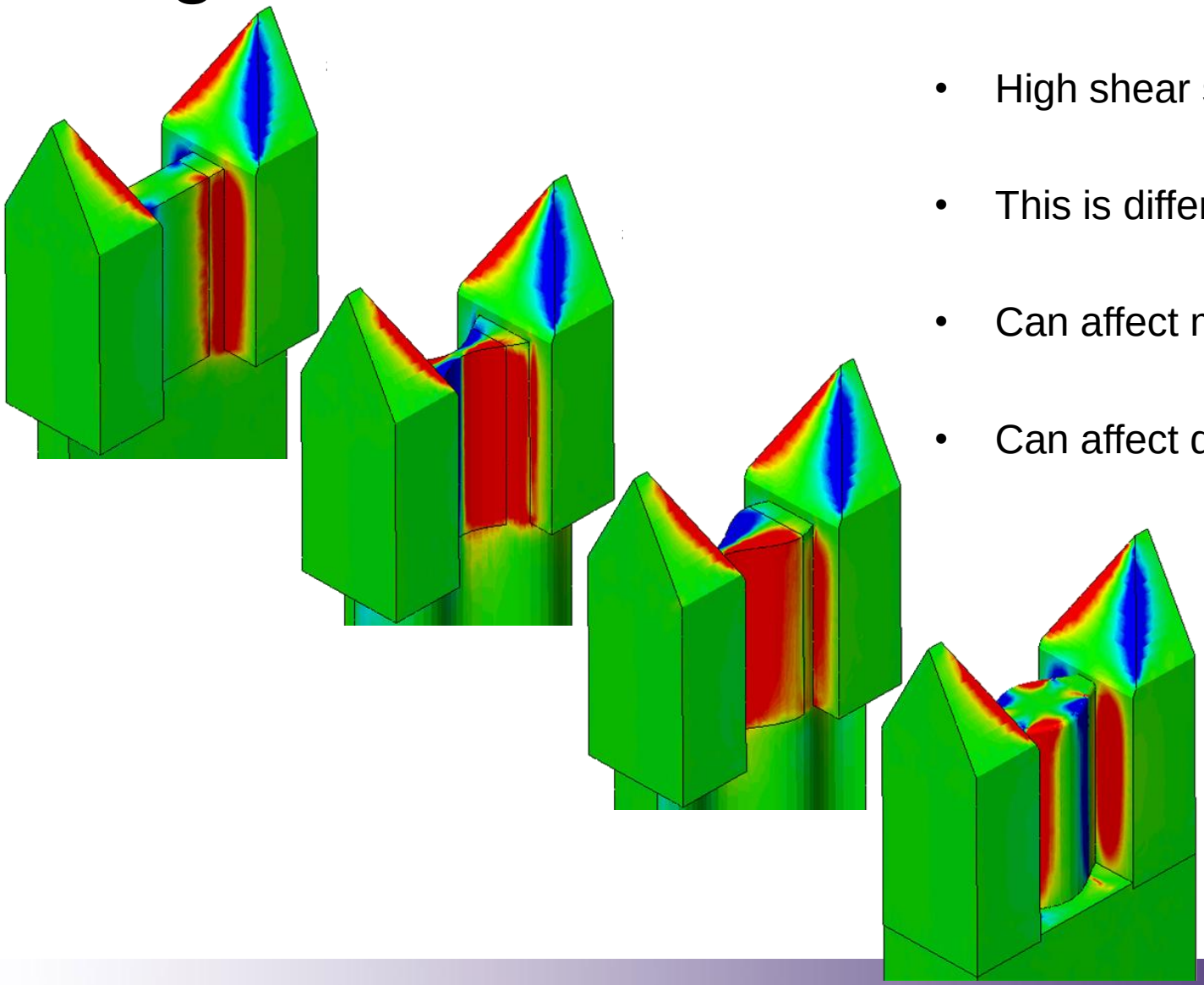
# Non-Uniform Fin Stress Patterns





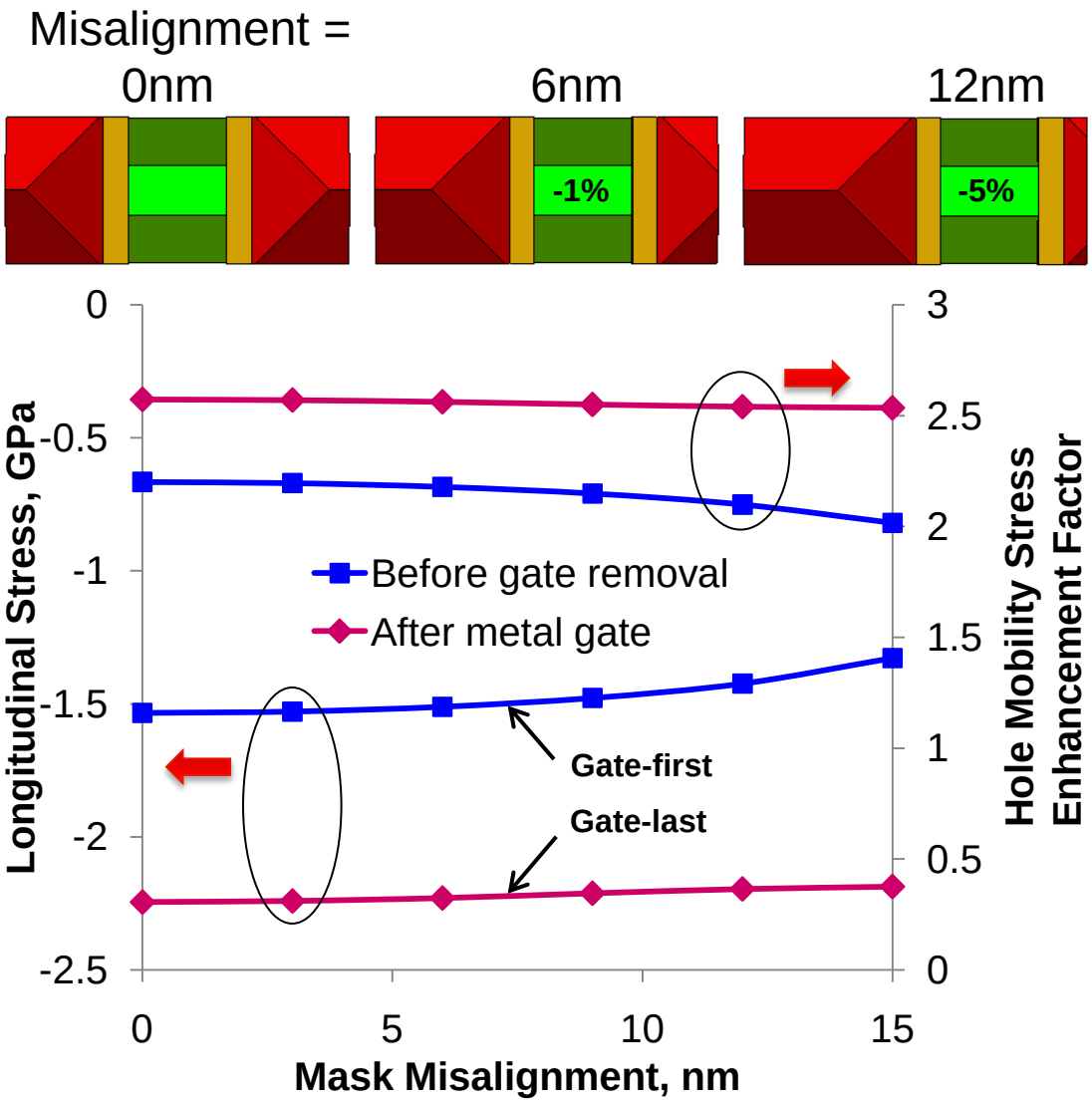

- -1 GPa
- -5 GPa
- Zero stress
- Huge stress variations, especially at the S/D junctions
- To get average fin stress of ~2 GPa, peak stress in the fin exceeds dangerous 5 GPa

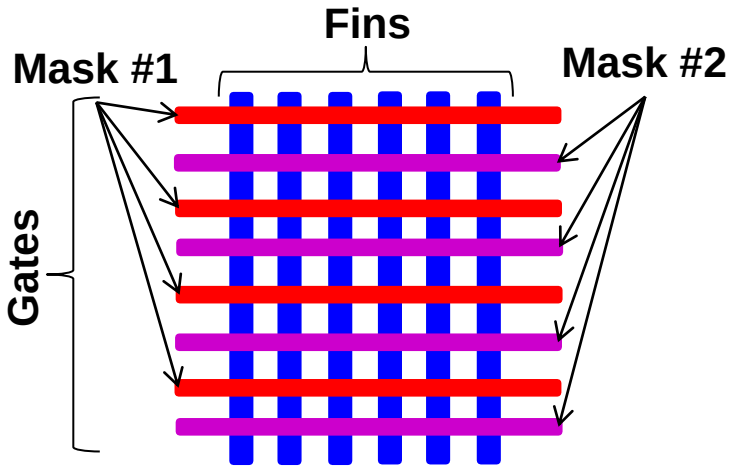
# High Shear Stress Levels



- High shear stress of ~1 GPa
- This is different from planar FETs
- Can affect mobility enhancement
- Can affect defect formation

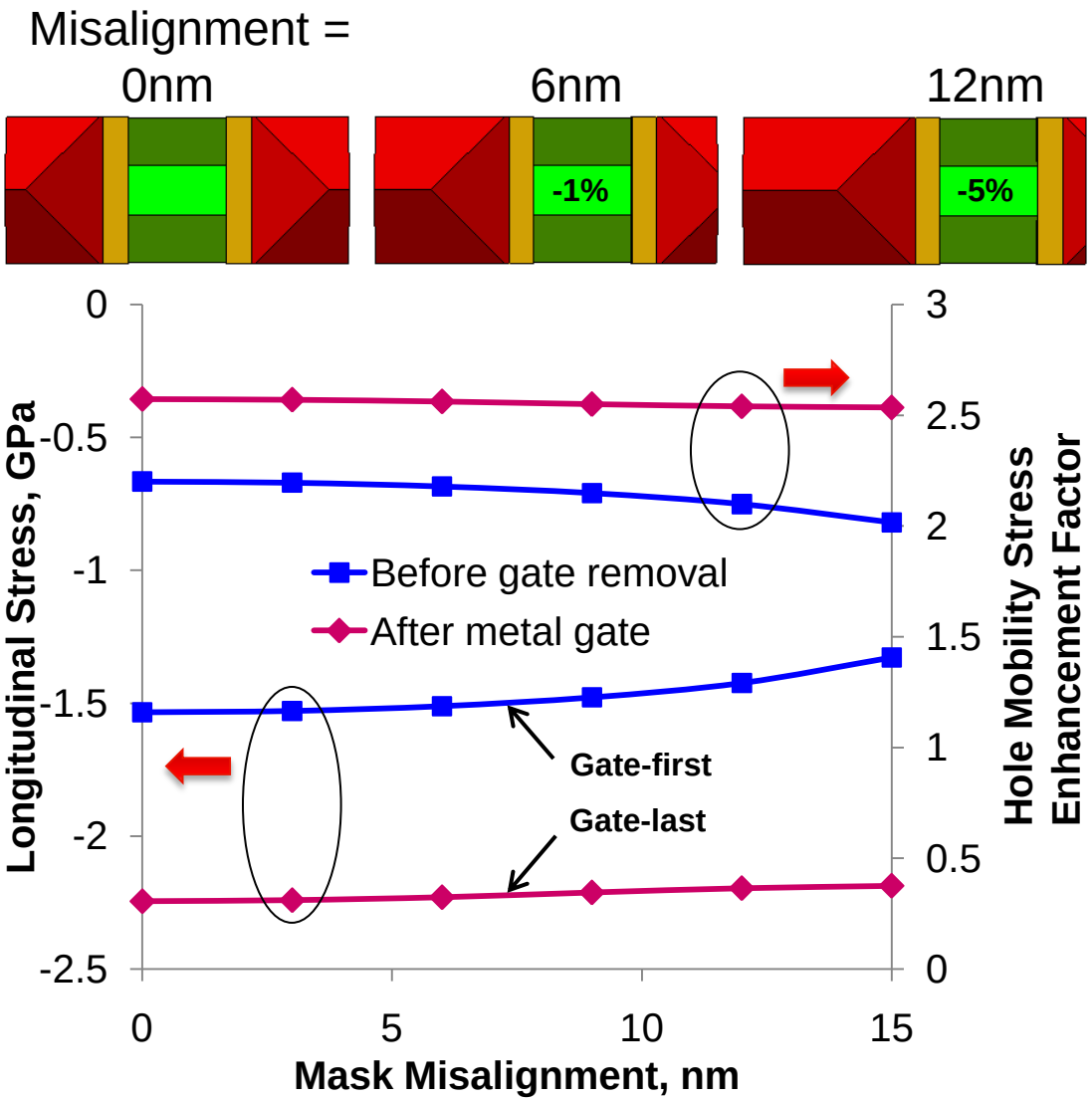
# DPT Mask Misalignment Impact on Stress

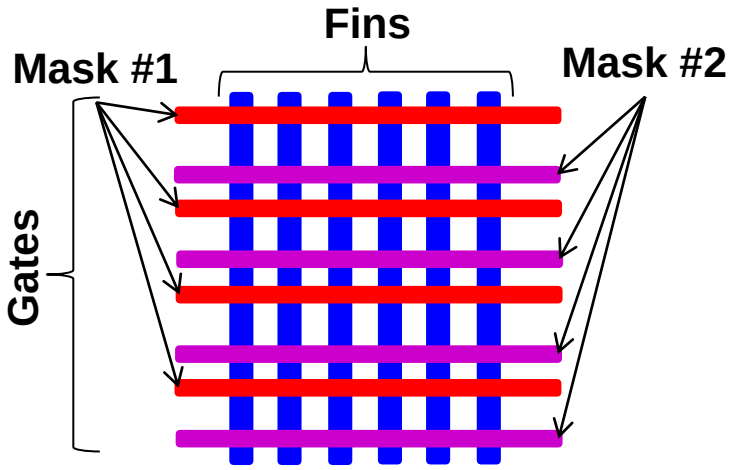



- Remarkably little stress loss even for major misalignment for gate-last HKMG
- Stronger effect for gate-first HKMG
- Again, perfect case performs the best
- Contact resistance will degrade much faster

# DPT Mask Misalignment Impact on Stress




- Remarkably little stress loss even for major misalignment for gate-last HKMG
- Stronger effect for gate-first HKMG
- Again, perfect case performs the best
- Contact resistance will degrade much faster

# Outline

- LER effects for litho and spacer litho
- Random dopant fluctuations
- Stress engineering
- **Conclusions**

# Conclusions

- **FinFET variability mechanisms are analyzed for 16nm node**
- **LER effects analyzed as a set of extreme cases:**
  - State-of-the-art litho is not good enough for fin and gate patterning
  - Spacer lithography provides manageable amount of variations
  - Geometry variation of +/- 1nm dominates variability over RDF & $\sigma$
- **Random dopant fluctuations are suppressed due to undoped channel and full depletion**
  - S/D junction abruptness is not critical for performance & variability
  - Single stray donor/acceptor dopant does not disturb performance significantly
- **Stress engineering is very efficient in FinFETs, but brings several new issues**
  - Remarkable stress gradients, from 5 GPa to 0 across the fin
  - High shear stress levels, ~1 GPa
- **3D simulation methodology demonstrated for several major FinFET variability mechanisms**
- **Metal grains for gate-last HKMG are too small to matter**