

# Modeling of IC Variability

**Simulation and Characterization of Statistical CMOS Variability  
and Reliability**

**SISPAD 2010 Workshop**

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# Introduction

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- IC variability originates from interacting layout components, manufacturing imperfections, and randomness at the atomistic scale.
- IC variability has a hierarchical & hybrid character
  - Its hierarchy reflects the nature of production (*device, chip, field, wafer, and wafer-lot*)
  - It is *hybrid*, because at each levels variability consists of *systematic (deterministic)* and *random* components.
- A complete, yet *parsimonious* statistical model is needed to capture and describe variability.



# Outline

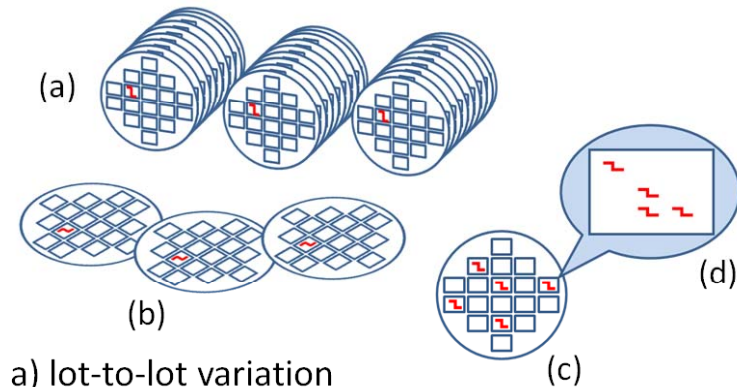
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- Introduction
- Modeling and Case Studies
  - Random Variability
  - Systematic (Deterministic) Variability
  - Global Hierarchical Variability Model
- Future

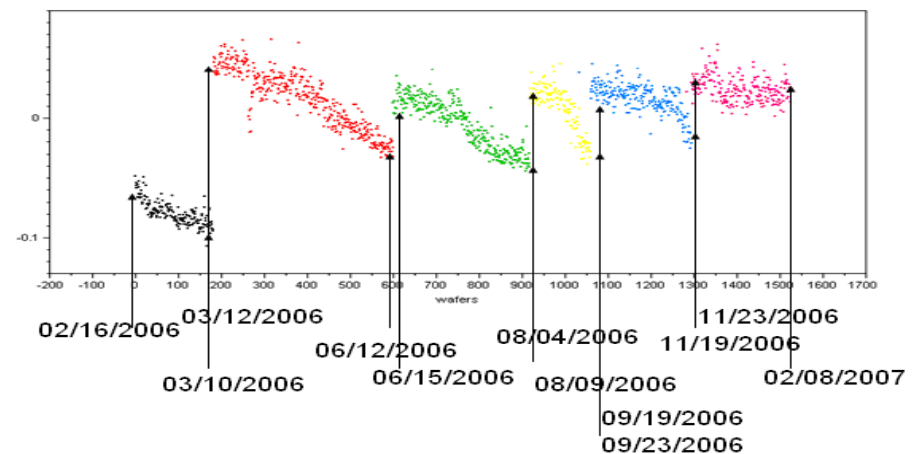


# Why is it such a hard problem?

- Dual Nature: Random vs. Systematic
- Various levels of *Hierarchy*
  - die, field, wafer, lot
- Various *consumers* of variability information
  - device, process, circuit engineers
- A large portion of variability is not stationary



a) lot-to-lot variation  
b) wafer-to-wafer variation  
c) die-to-die or across-wafer variation  
d) within-die variation



# Model Hierarchy (lot, wafer, within wafer, within die)

$$p_{ijkl} = \eta + \lambda_i + \sigma_j + \alpha_{ij} + \beta_k + \omega_{ijk} + \gamma_l + \tau_{kl} + \epsilon_{ijkl}$$

Model Estimator	Description
$\hat{\eta} = \bar{p}_{....}$	Global Mean
$\hat{\lambda}_i = \bar{p}_{i...} - \bar{p}_{....}$	Lot Factor
$\hat{\sigma}_j = \bar{p}_{.j..} - \bar{p}_{....}$	Wafer or Slot Factor
$\hat{\alpha}_{ij} = \bar{p}_{ij..} - \bar{p}_{i...} - \bar{p}_{.j..} + \bar{p}_{....}$	Lot-Wafer Interaction Factor
$\hat{\beta}_k = \bar{p}_{..k.} - \bar{p}_{....}$	Average Wafer
$\hat{\omega}_{ijk} = \bar{p}_{ijk.} - \bar{p}_{ij..} - \bar{p}_{..k.} + \bar{p}_{....}$	Deviation from Average Wafer
$\hat{\gamma}_l = \bar{p}_{...l} - \bar{p}_{....}$	Average Die
$\hat{\tau}_{kl} = \bar{p}_{..kl} - \bar{p}_{..k.} - \bar{p}_{...l} + \bar{p}_{....}$	Die-Site Interaction
$\hat{\epsilon}_{ijkl} = p_{ijkl} - \bar{p}_{ijk.} + \bar{p}_{..k.} - \bar{p}_{..kl}$	Residual



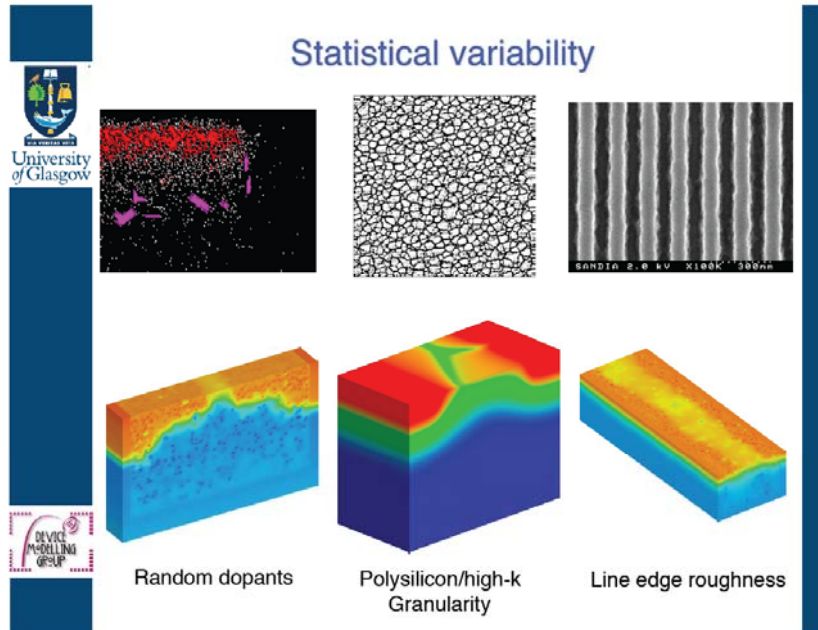
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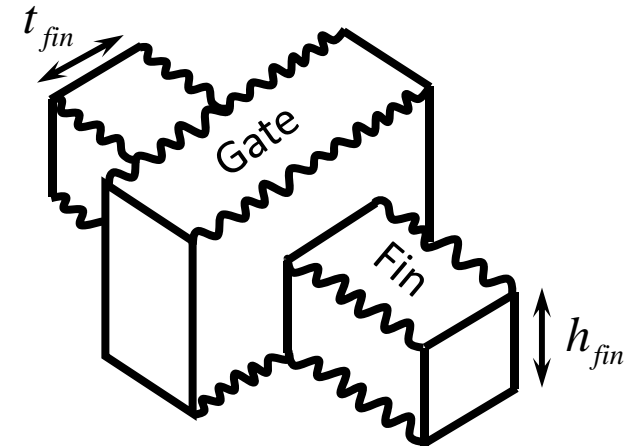
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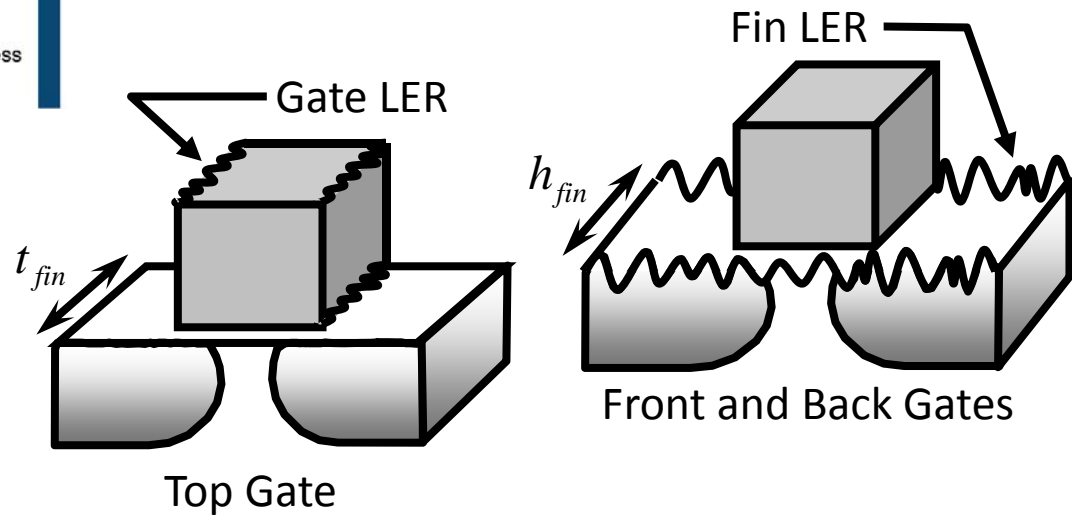
# Intrinsic (Random) Variability



IEEE/ACM Workshop on Variability Modeling and Characterization  
 ICCAD 2009  
 Scott Roy (Univ. of Glasgow): Atomistic Simulation of Variability

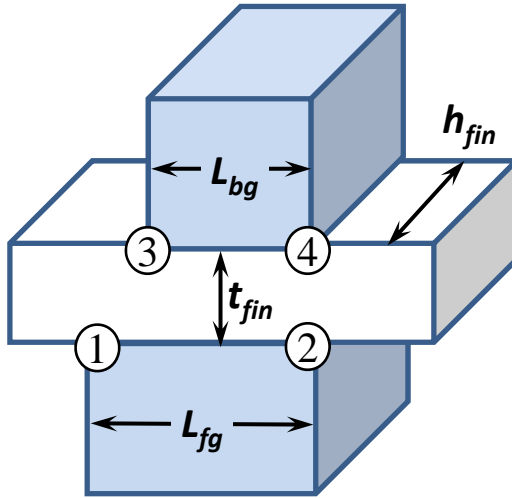


(Patel, Spanos and King-Liu, TED 2009)



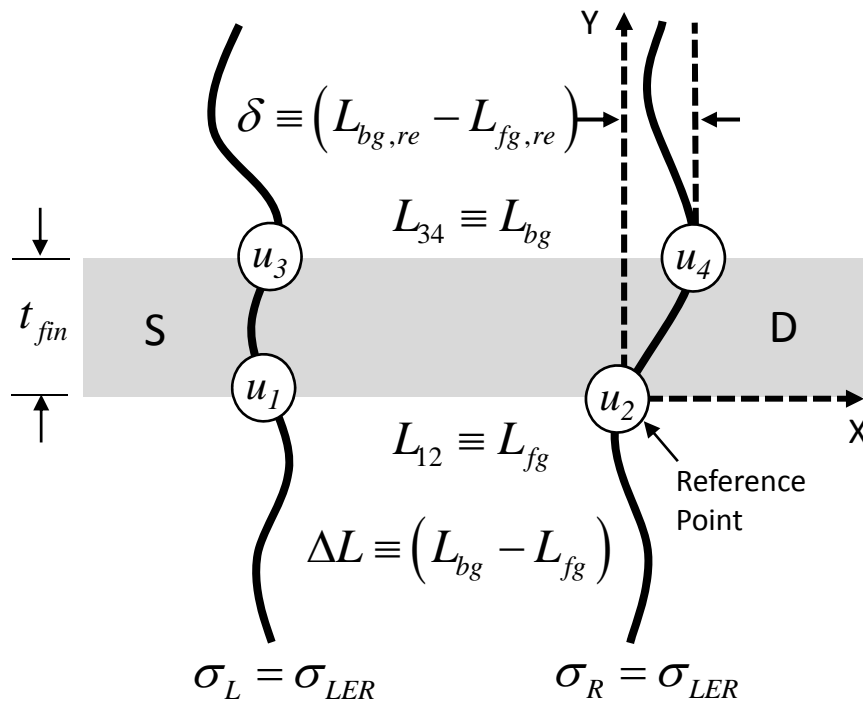
# LER Model Description

(Patel, Spanos and King-Liu, TED 2009)



$$\sigma_{\delta}^2 = 2\sigma_{LER}^2 \left(1 - \rho_A(t_{fin})\right)$$

$$\rho(y) = e^{-\left(\frac{|y|}{\xi}\right)^{2\alpha}} \quad \text{Auto-correlation function}$$



For a resist-defined gate electrode,

$$\sigma_{\Delta L}^2 = 4\sigma_{LER}^2 \left[1 - \rho_A(t_{fin})\right].$$

For a spacer-defined gate electrode ,

$$\sigma_{\Delta L}^2 = 0$$





# LER Simulation Details

**TABLE 1: 2-D DEVICE SIMULATION PARAMETERS**

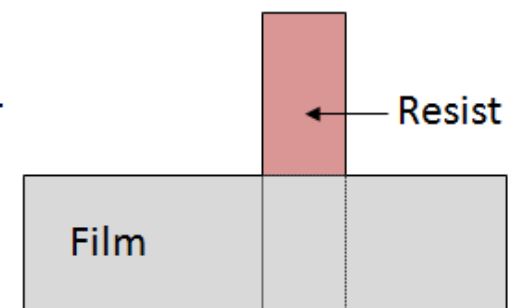
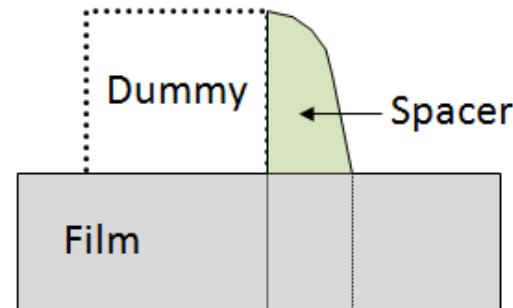
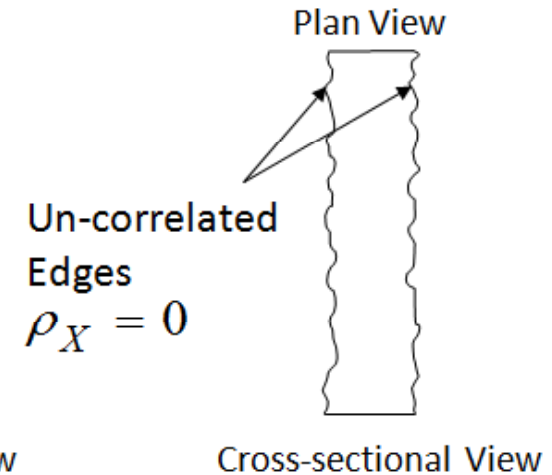
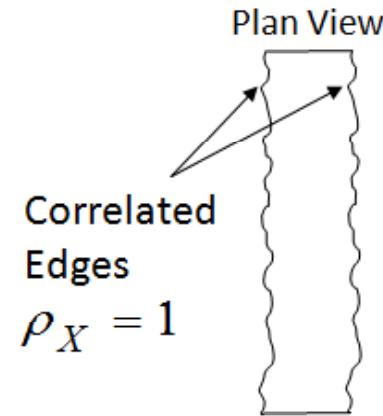
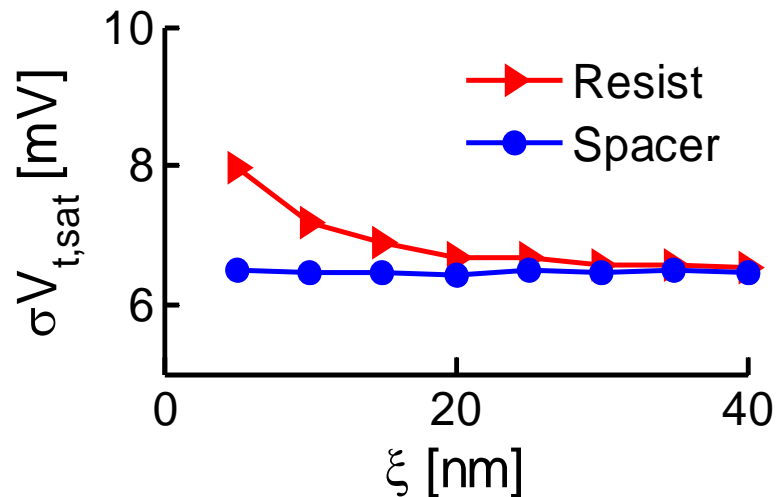
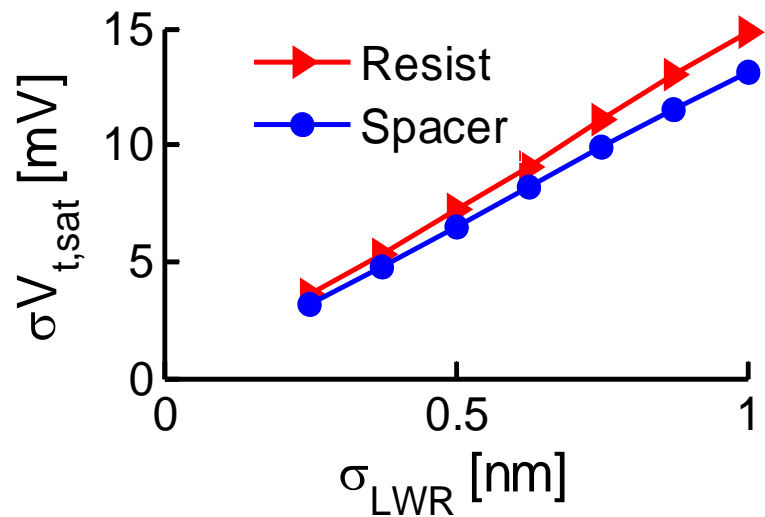
Electrical/Doping	Structural
$V_{dd}=0.9V$	$L_g=13nm$
$\phi_m=4.62eV$	$t_{ox}=6A$
$N_B=1e15\text{ cm}^{-3}$	$L_{sp}=7.2nm$
$N_{s/d}=1e20\text{ cm}^{-3}$	$t_{fin}=7.5nm$
$\sigma_{s/d}=4nm/dec$	$t_{poly}=13nm$

**TABLE 2: 2-D NOMINAL DEVICE PERFORMANCE PARAMETERS.**

Parameter	Units	Value
$V_{t,sat}$	mV	210
SS	mV/dec	69
DIBL	mV/V	30
$g_{m,sat}$	mA/V	6.75
$I_{d,sat}$	mA/ $\mu m$	2.48
$I_{off}$	pA/ $\mu m$	94.4



# Spacer v. Resist



(a) Spacer Defined

(b) Resist Defined

$$\sigma_{LWR}^2 = 2\sigma_{LER}^2 (1 - \rho_X) \quad \sigma_L = \sigma_R \equiv \sigma_{LER}$$



# Outline

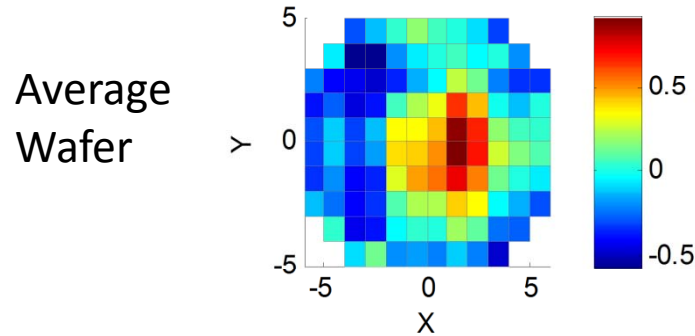
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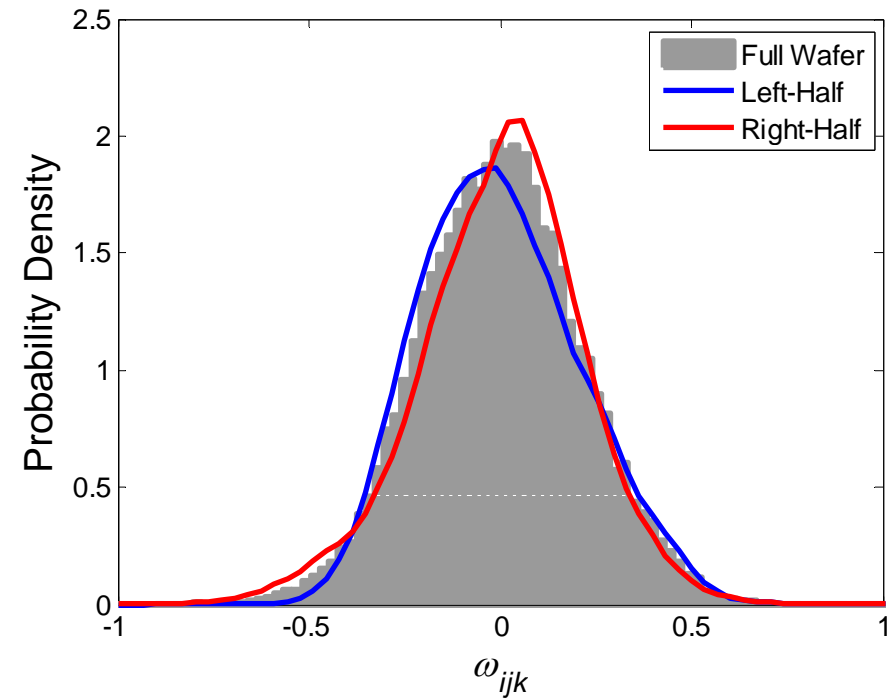
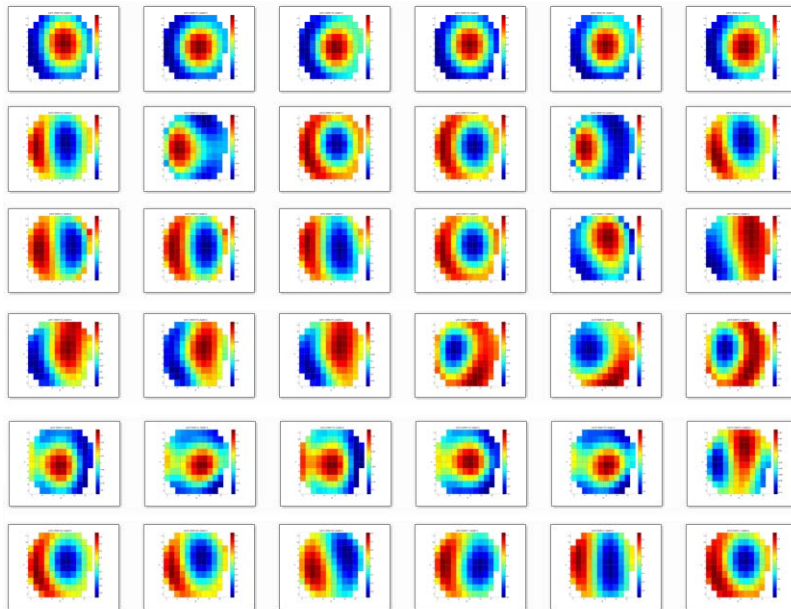


# The Statistics of Spatial Variability

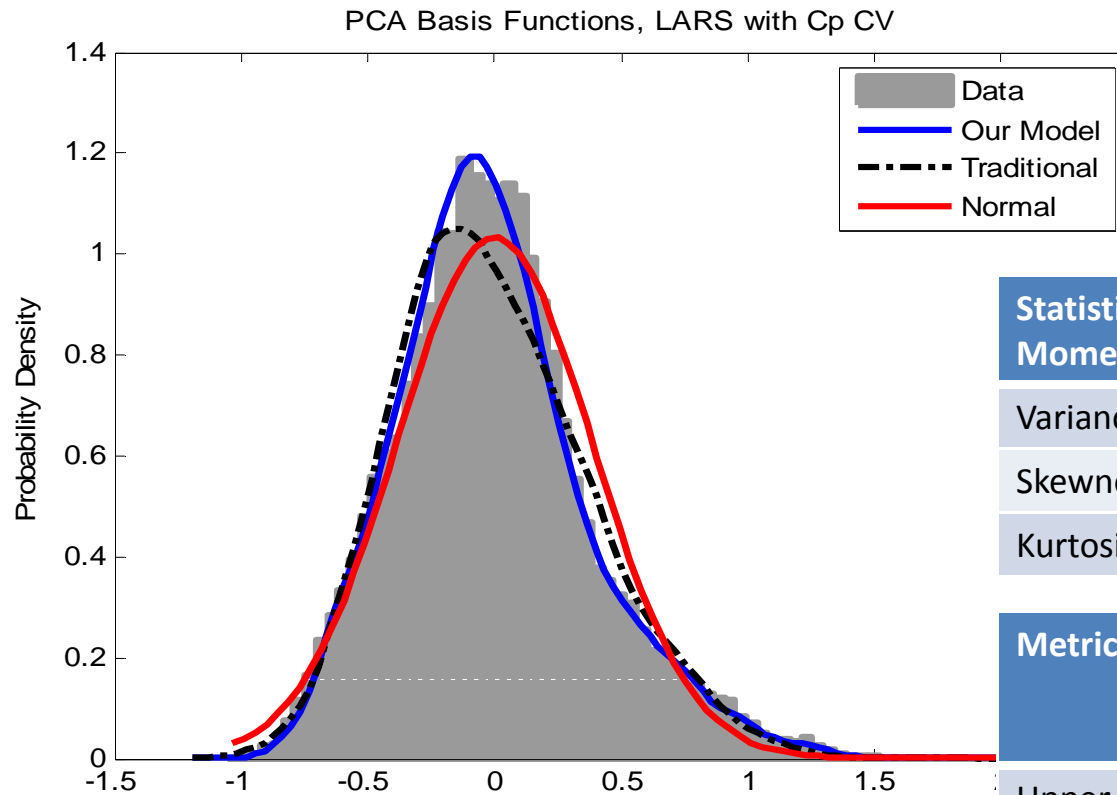
Ring Oscillator Frequency, 65nm node



Residuals



# Results using PCA Basis Functions



Statistical Moment	Data	Traditional Model	Our Model
Variance	0.149	0.147	0.142
Skewness	0.545	0.401	0.563
Kurtosis	3.555	3.002	3.544

Metric	% Actual Data [95% CI]	% Traditional Model	% Our Model
Upper Tail	1.47 [1.34, 1.61]	1.00	1.45
Lower Tail	0.02 [0.00, 0.03]	0.09	0.02
Out of Spec [-1, 1]	1.49 [1.35, 1.62]	1.00	1.45

Traditional Method:

$$\hat{\beta} + \varepsilon_{\hat{\omega}}$$

$$\varepsilon_{\hat{\omega}} \sim N(0, \text{var}(\hat{\omega}_{ijk}))$$

Proposed Method:

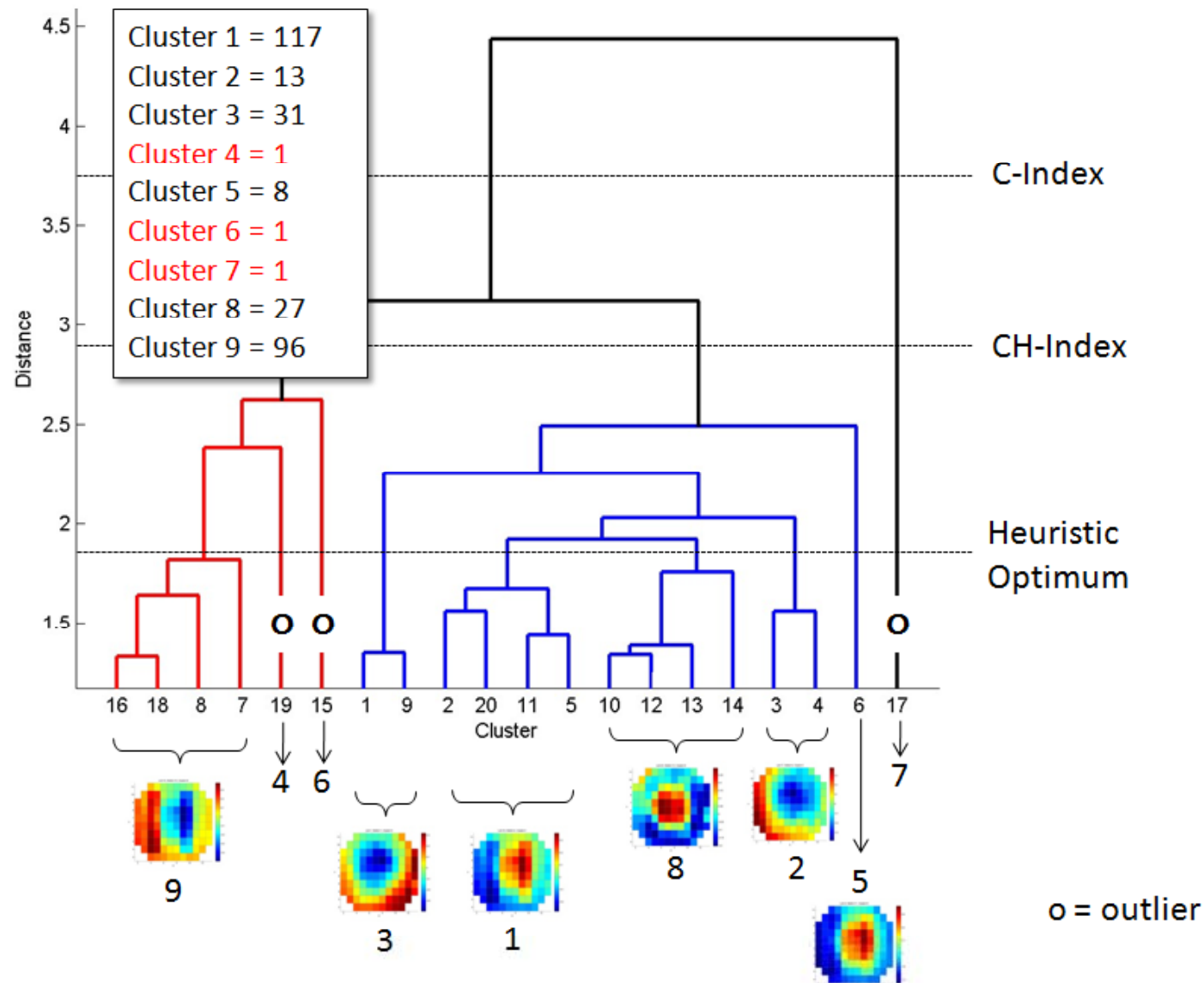
$$\hat{\beta} + \tilde{\omega} + \varepsilon_R$$

$$\varepsilon_R \sim N(0, \sigma_R^2)$$

$$R = \hat{\omega}_{ijk} - \tilde{\omega}$$



# A Bonus Application: Cluster Analysis



# Outline

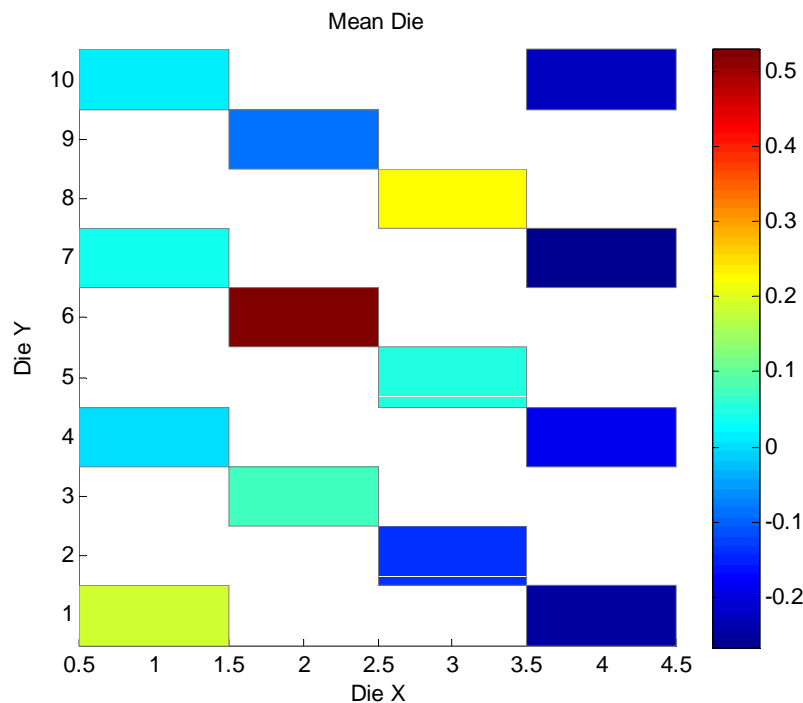
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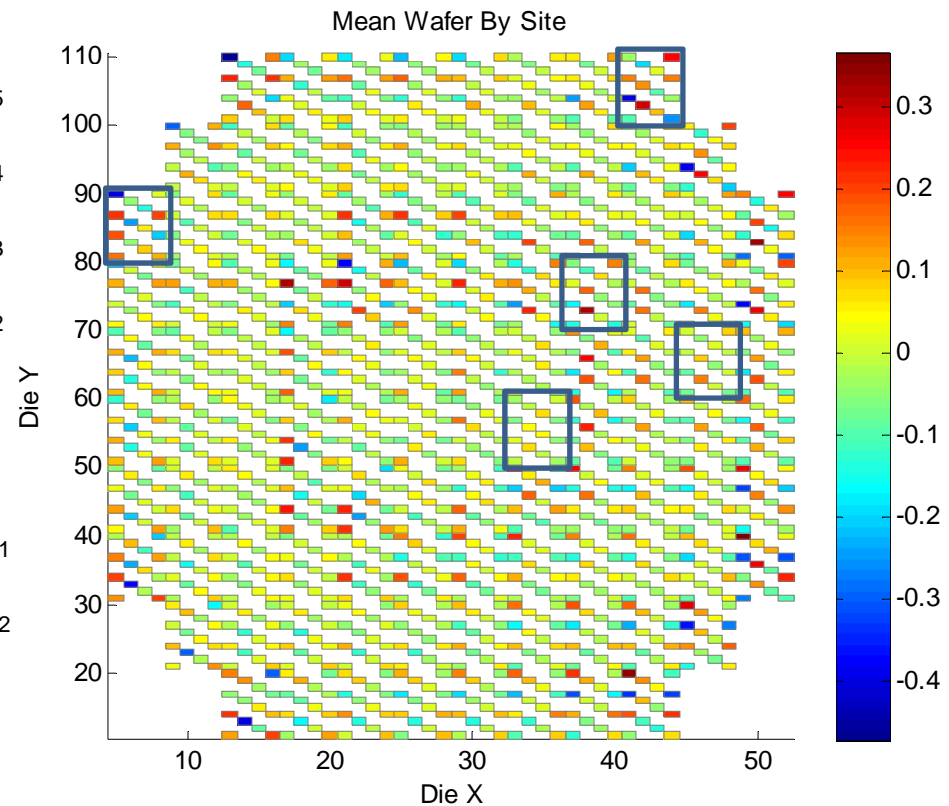


# Within-die Variation

$$p_{ijkl} = \eta + \lambda_i + \sigma_j + \rho_{ij} + \beta_k + \omega_{ijk} + \gamma_l + \tau_{kl} + \delta_{ijkl}$$

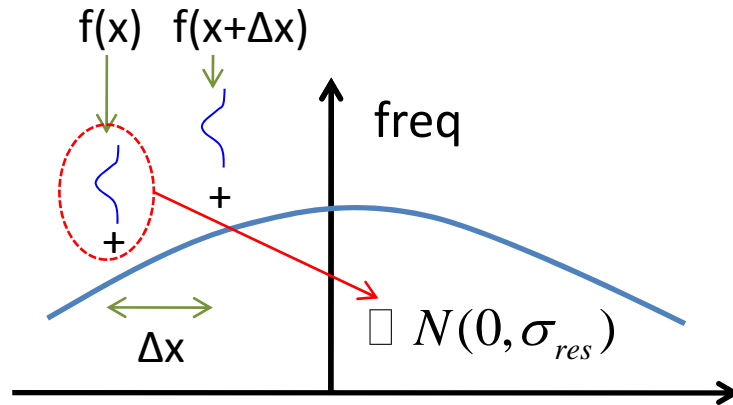


Average die





# Apparent Spatial Correlation

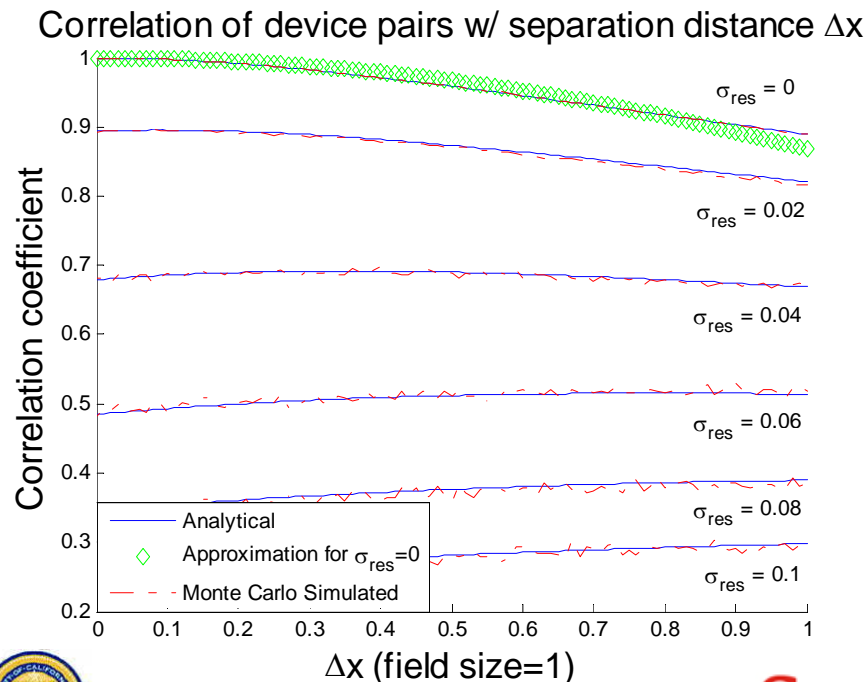


$$Z_1 = f(x, y) + e_1$$

$$Z_2 = f(x + \Delta x, y) + e_2$$

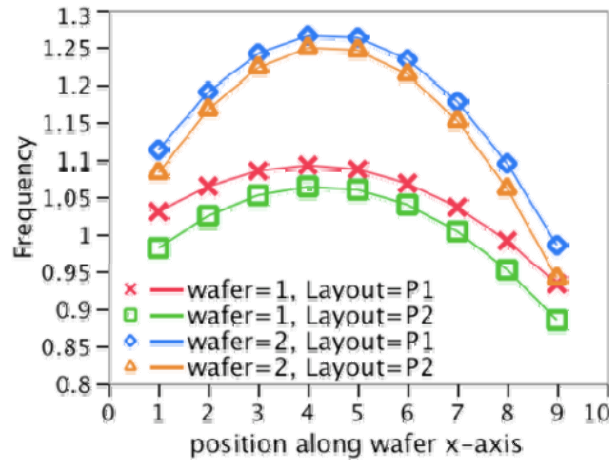
$$\approx f(x, y) + \frac{\partial f(x, y)}{\partial x} \Delta x + e_2$$

>> Unmodeled Systematic Variation Exhibits Spatial Correlation

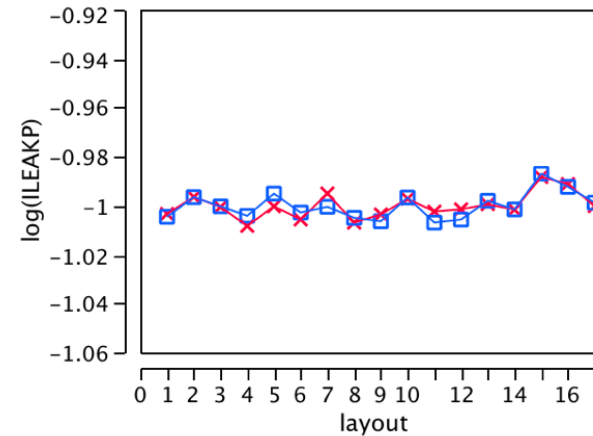


# Layout Effect Analysis

Fitted across-wafer frequency map

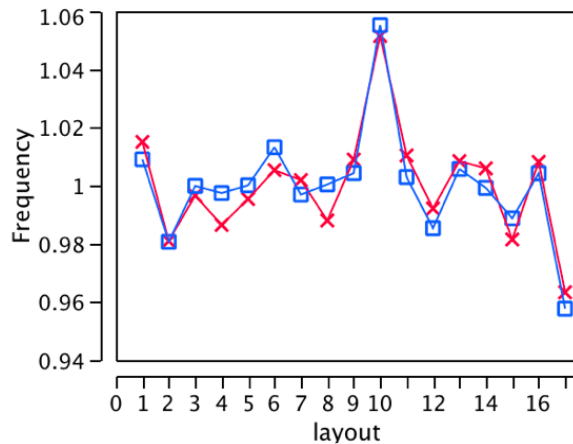


Layout-to-layout log(ILEAKP) variation



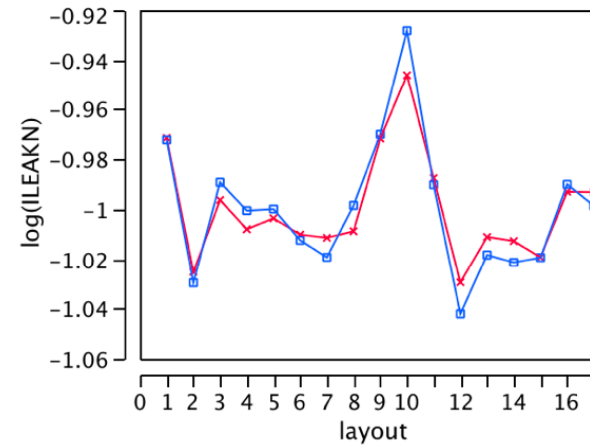
Y x — wafer1 □ — wafer2

Layout-to-layout Frequency Variation



Y x — Wafer1 □ — Wafer2

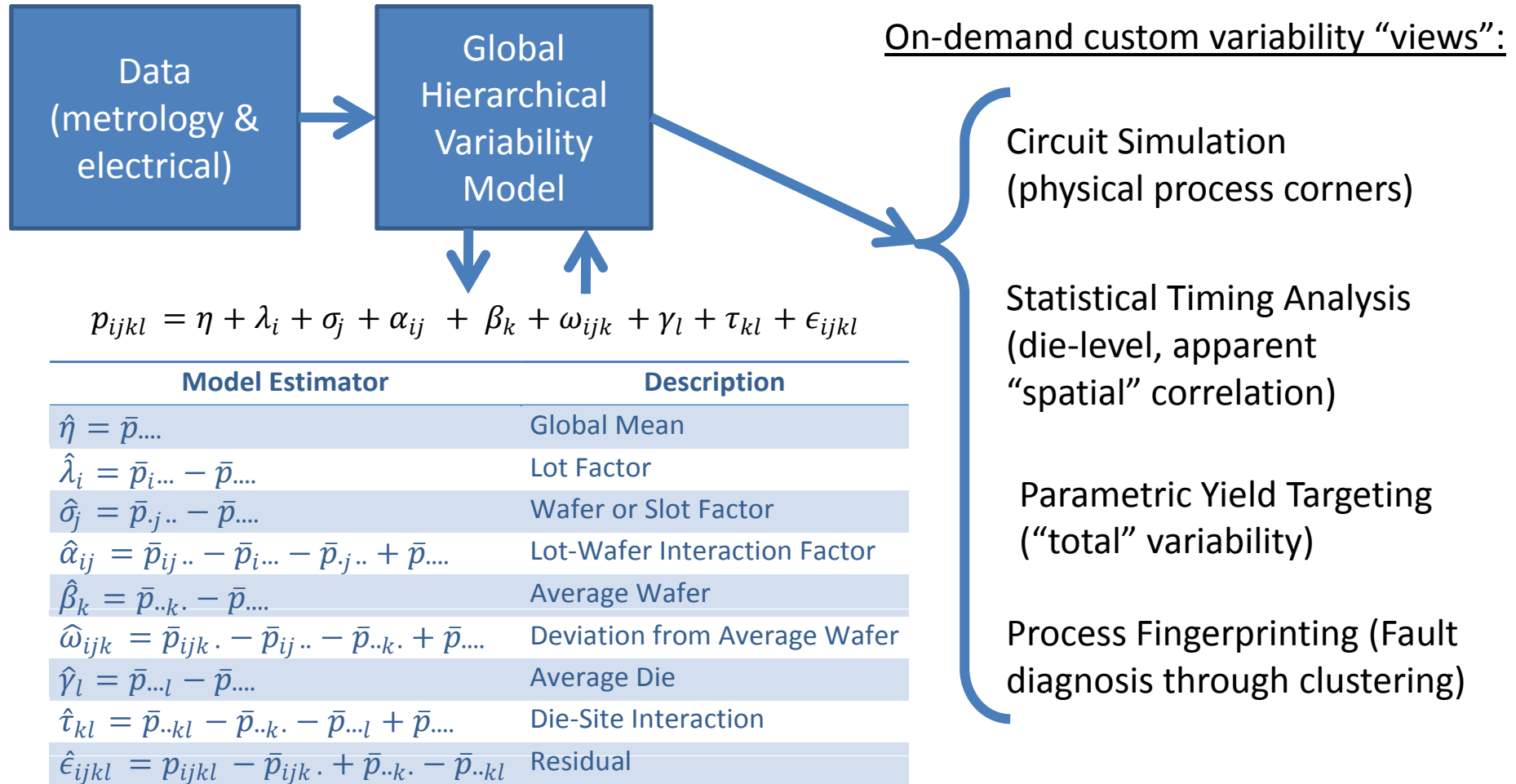
Layout-to-layout log(ILEAKN) variation



Y x — Wafer1 □ — Wafer2



# Global Hierarchical Variability Model



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# Of Further Interest

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- What about Statistical Circuit Simulation?
  - Propagating Gaussian and Mixture of Gaussian (MOG) distributions through interval representation
- What about temporal non-stationarity?
  - Can be modeled or “collapsed” depending on the needed “view”
- What about SRAM variability?
  - Nothing special other than we really must capture extreme tails of distribution extremely well (see above)



# Acknowledgements

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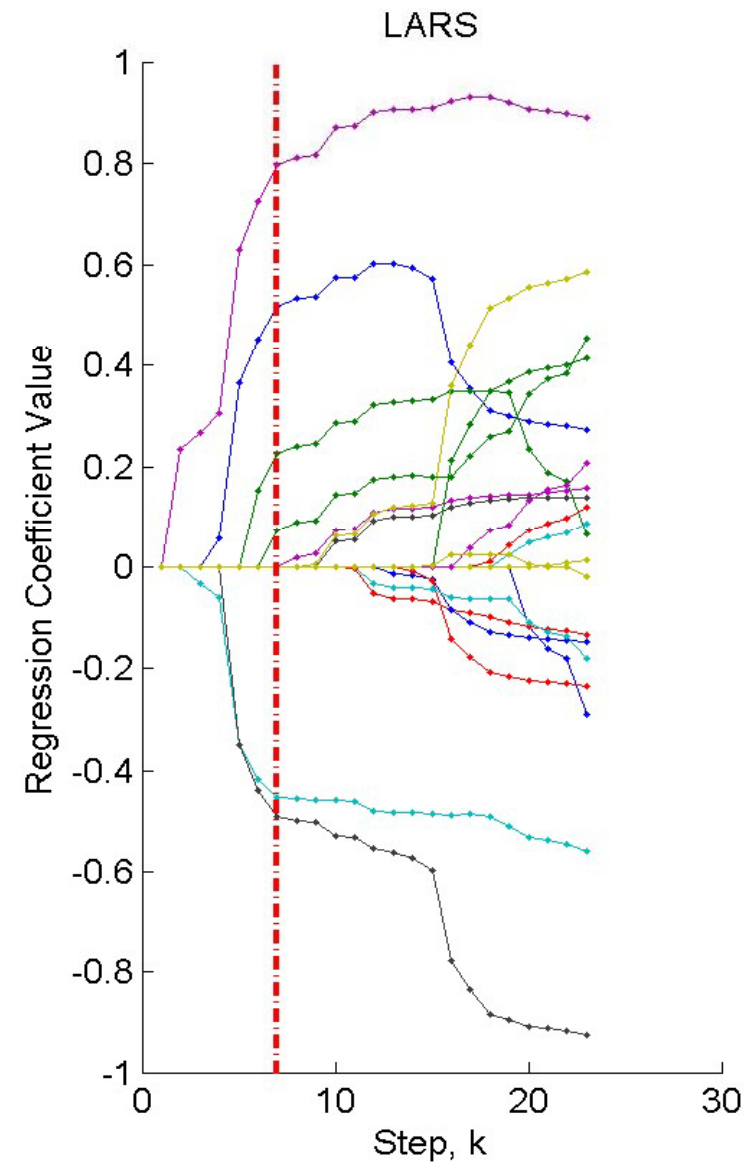
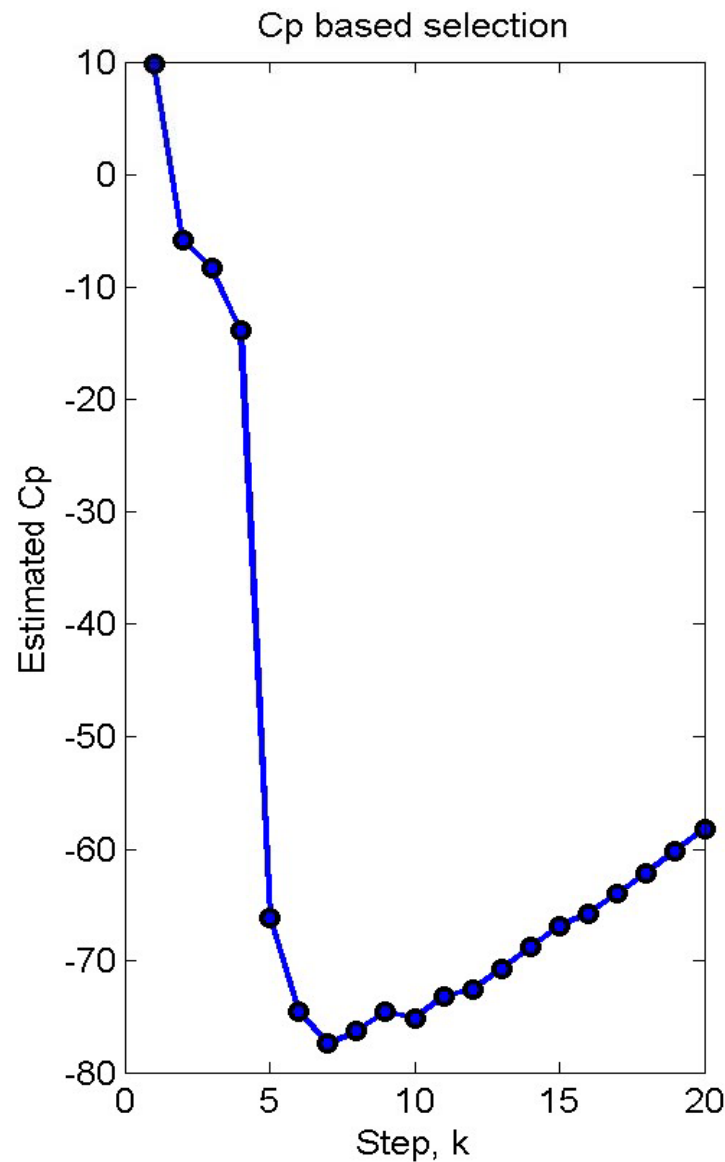


Thank you for your attention!

Questions?



# Least Angle Regression with Cp Selection



Lot 7, Wafer 9, Terms = 1, 2, 4, 7, 9, 12